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WELCOME NOTES

On behalf of the ISQED 2004 conference and technical committees, we are pleased to welcome you to the 5th IEEE International Symposium on Quality Electronic Design, ISQED 2004, the leading conference in design for manufacturability and quality. Due to the overwhelming success of the last 4 conferences and the unique value that it offers, IEEE ISQED is gaining recognition in both academia and industry. We look forward to continuing this tradition of excellence.

Siva Narendra
Technical
Program Chair

All the technical presentations, plenary sessions, panel discussions, tutorials and related events will take place on March 22-24 at the San Jose Double Tree Hotel. The hotel is located in the heart of Silicon Valley, near the San Jose International Airport, and is a very convenient location for all conference participants whether local, US or international attendees. It is clear that advances in semiconductor processing and manufacturing technologies continue to progress at an ever increasing rate giving rise to complex processes and physics, and making possible increasingly complicated designs. Due to these advances, we are in a situation of even greater dependencies between integrated circuit design, semiconductor technology development, manufacturing, and test.

Kaustav Banerjee
Conference Chair

In addition, issues of modeling, verification, validation and characterization are taking on an increasingly important and critical role due to the highly complex interaction between IC design and process.

Furthermore, evolving business models making possible the availability of IP from a variety of sources and where questions of qualification, use/reuse, and integration exacerbate this complexity. This program will attempt to address these issues by bringing together industry practitioners and academics engaged in deep sub-micron integrated circuit design and development.

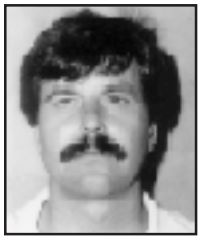
The technical sessions will span the numerous disciplines that in total define the IC industry, but whose common goal is the improvement of design quality, particularly with respect to metrics such as device robustness, yield, testability, design productivity and overall systems cost. This conference provides a unique opportunity to bring together people and ideas to whose common goal understand and discuss the key issues faced by industry in the next few years, highlight emerging areas of importance, and provide possible solutions to these challenges.

The technical program for ISQED 2004 has been assembled by the technical program committee, which includes international experts from industry and academia.

The technical program committee has selected papers for presentation from numerous excellent submissions. This year, a total of 49 papers were accepted for regular presentation from 148 papers submitted to ISQED 2004. Because of the high quality of this year's submissions, an additional 12 short papers were accepted. The technical program also includes two invited papers from leading experts in the field. Due to the high quality of submitted papers this year several additional papers were accepted for poster presentation.

The ISQED 2004 Best Paper Award ceremony will be held during the luncheon on Tuesday.

The conference will commence with our popular tutorial sessions, organized by Dennis Sylvester and Enrico Malavasi, and will be held on Monday, March 22. We will have a single but comprehensive track on compact modeling, featuring leading experts from around the world. The tutorial sessions cover a variety of exciting and timely topics such as Compact Modeling and Analysis for Nanometer-scale CMOS Design, Manufacturability, Variability/Uncertainty, Advanced Devices, Low-Power Design, and Interconnect Modeling & Analysis



Geroge Alexiou
Technical
Program Vice
Chair

The 2004 tutorials at ISQED offer a truly outstanding opportunity to catch-up with the latest areas of research and development.

In keeping with our tradition of bringing highly renowned leaders from industry and academia to discuss vital issues, we are pleased to offer again two plenary sessions, organized by Kris Verma and Lech Jozwiak. This year, we have two plenary sessions, the first on Tuesday and the second on Wednesday, with 3 speakers in each session. In the first keynote speech on Tuesday, John Chilton Sr. VP of Synopsys will address enabling Quality thru innovation in Semiconductor electronic devices by working with a new Business model between Fabless Design companies, IP Provider, EDA tools Provider, and Mega foundries by focusing on their respective core competencies to add value.

Kenneth Shepard
Conference Vice
Chair

Second Speaker, Marc Levitt, VP and GM of Cadence Design System will give his views and insight on will discuss what is needed in a new generation design-for-yield tool suite to address the quality of silicon at its source.

WELCOME NOTE

Third speaker, Larry Bock, CEO of Nanosys Inc., will take us in to new emerging world of nanoelectronics devices. Larry will point out, why nanoelectronic devices start getting attention NOW and how they will revolutionize the electronics in coming decade or decades.

Bharath Rajagopalan
General Chair

This second plenary session has three key leaders. First speaker, Prof. Yasuura Hiroto of Kyushu University of Japan, will address new Infrastructure in today's digital world and its impact on our daily life. He will mainly focus on implementation of Silicon-on-Chip technology in to bi-directional mutual authentication through personal identification device (PID), RF –ID tags and challenges associated with this.

Second Speaker, Pierre Paulin, Director of SoC Platform Automation of ST Microelectronics, Canada will address high quality scalable SoCs for heterogeneous design blocks. Pierre will discuss an approach to effectively integrate heterogeneous parallel blocks in to homogenous programming environment, which leads to high quality designs.

Final speaker of the session Prof. K. Saraswat of Stanford University will explore the ultimate in CMOS scaling (65nm-35nm regime) including some modifications in conventional FET such as adding layers of Ge and other materials . Dr. Saraswat will also provide his insight in to various forms of new devices such Silicon based quantum-effect devices, nanotube electronics. molecular and organic semiconductor devices, and optical interconnections, which may either co-exit with CMOS or carve out their own new technology path.

Ali Iranmanesh
Founding Chair

The ISQED 2004 program also includes two panels, one each on Monday and Tuesday evening. The first, organized by Pallab Chatterjee and moderated by Tets Maniwa, asks the following questions: DFM PDK's: Where do they belong? Are Process Design Kits (PDKs) the answer for modern Design For Manufacturing (DFM) issues?

The second evening panel on Tuesday night, organized by Phil Dworsky, and moderated by Ron Wilson, is titled: "IP Industry: Nordstrom or K-Mart? The trend toward tighter relationships between supplier and user".

Come and hear the opinions of the leaders in the field, and voice your opinion during the audience participation phase for these controversial topics. In summary, we have assembled an excellent program for academics, practicing engineers and managers in the IC industry to learn the latest on quality electronic design so that functional integrated circuits, with expected performance, acceptable yield and reliability, can be manufactured within the frame work of the desired cycle time. This conference provides a forum for you to learn and share and exchange insight and knowledge with your peers. We look forward to seeing you in March 2004.

Sincerely,

Siva Narendra
Technical Program Chair

George Alexiou
Technical Program Vice-Chair

Kaustav Banerjee
Conference Chair

Ken Shepard
Conference Vice-Chair

Bharath Rajagopalan
General Chair

Ali Iranmanesh
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Intel

Janet Meiling
Arizona State University

Mohammad Mortazavi
Cadence

GENERAL INFORMATION

ISQED 2004 GENERAL INFORMATION

March 22-24, 2004

DoubleTree Hotel
2050 Gateway Place
San Jose, CA
Telephone: 408-453-4000

TUTORIALS

Monday, March 22, 8:30am-5:15pm
San Carlos/San Juan
Tutorial registration includes the tutorial workbook, lunch and coffee breaks.

PLENARY SESSIONS

Plenary Session 1P

Sponsored by Synopsys

Tuesday, March 23, 8:30 am - 10:15 am
Donner Pass

Features keynote speeches by **John Chilton** (Sr. VP and General Manager, Synopsys, Inc.), **Marc Levitt** (Vice President and General Manager, Cadence Design Systems, Inc.), and **SY Wang** (Senior Scientist, Hewlett Packard Laboratory).

Plenary Session 2P

Sponsored By Magma

Wednesday, March 24, 8:30 am - 10:15 am
Donner Pass

Features keynote speeches by **Hiroto Yasuura** (System Research Center, Kyushu University, Fukuoka, Japan), **Pierre G. Paulin** (Director, SoC Platform Automation, Central R&D, STMicroelectronics, Ottawa, Canada), and **Krishna Saraswat** (Rickey/Nielsen Professor of Engineering, Stanford University).

TECHNICAL SESSION

There are a total of 18 technical sessions held on Tuesday and Wednesday. Technical sessions are held in 3 parallel tracks and are being held on **San Carlos**, **San Juan**, and **San Martin** rooms.

POSTER SESSION

Poster papers (session 1C) will be on display on Tuesday morning 10:00am-12:00pm . Authors will be available to discuss their works and to answer questions.

PANEL DISCUSSIONS

Evening Panel Discussion EP1& Dinner

Sponsored by PDF Solutions

Monday, March 22, 6:30 pm - 8:30 pm

DFM PDK's: Where do they belong?
Are Process Design Kits (PDKs) the answer for modern Design For Manufacturing (DFM) issues?

Moderator:
Tets Maniwa
Editor in Chief, Chip Design Magazine

Evening Panel Discussion EP2 & Dinner

Sponsored by Ascend Design Automation

Tuesday, March 23, 6:30 pm - 8:30 pm

IP Industry: Nordstrom or K-Mart?
The Trend Toward Tighter Relationships Between Suppliers and Users

Moderator:
Ron Wilson
Semiconductor Editor
EE Times (CMP Media Electronics Group)

Luncheon Awards & Speech

Tuesday, March 23, 12:00pm-1:00pm
Donner Pass

Committee Awards

12:00pm-12:25pm
This year ISQED honors veteran committee members for their outstanding committement and lasting contributions to the conference throughout it's 5 years history. ISQED **Sesior**, **Distinguished**, and **Fellow** members are introduced and acknowledged during the luncheon.

Best Paper Awards

Sponsored by Synopsys

The ISQED 2004 Best Paper Award Ceremony will be held prior to the ISQED luncheon speech on Tueday. List of best papers is shown in Page 2 of this document.

Luncheon Speech

12:25pm-1:00pm

Luncheon speaker is **Michael Keating** of Synopsys. The title of his talk is "**The IP Quality Revolution**"

GENERAL INFORMATION

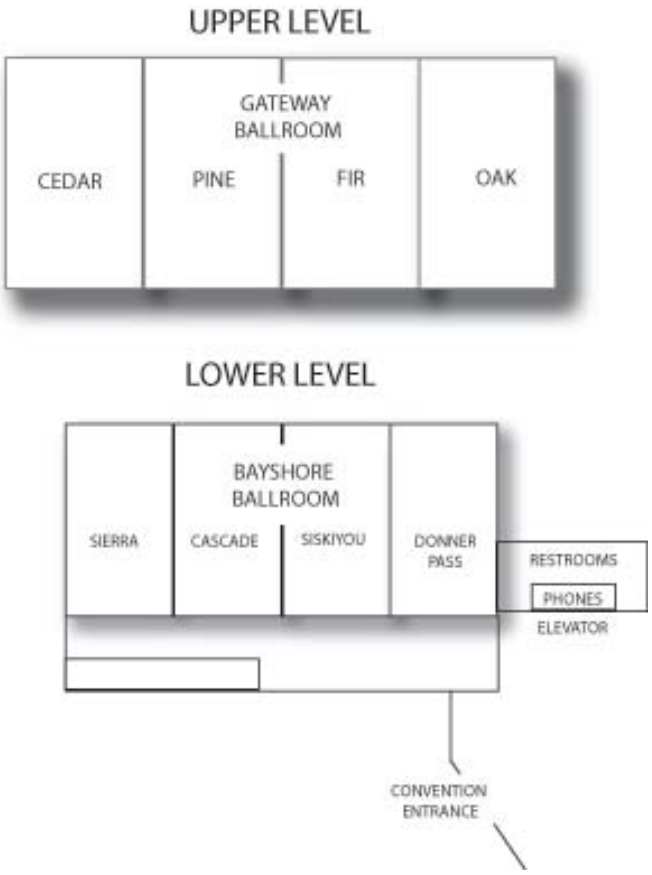
ON-SITE REGISTRATION

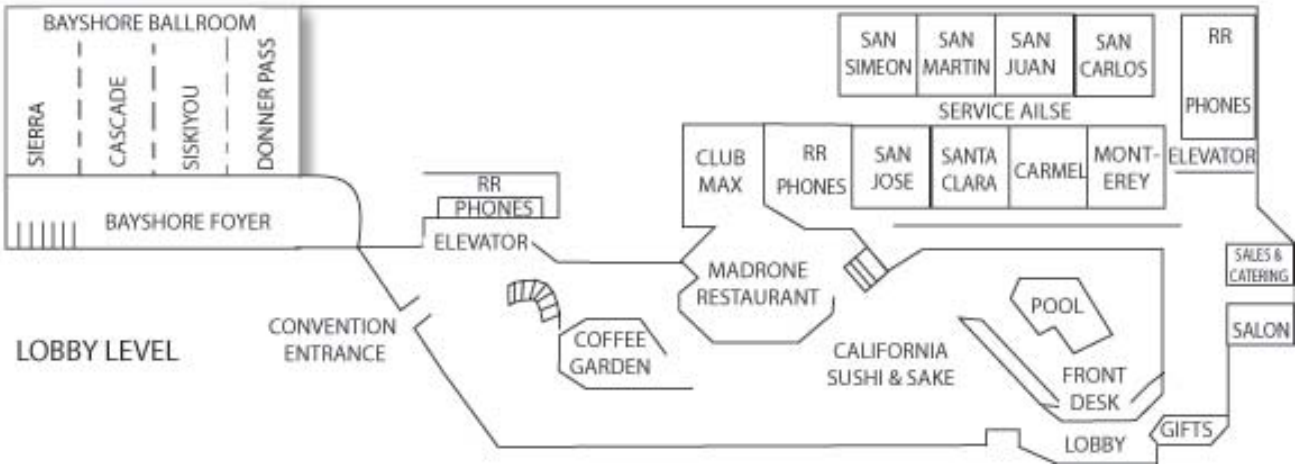
Location and time of on-site registration are as follows:

Sunday, March 21, 2004	*5:00pm-7:00pm*
Monday, March 22, 2004	*8:00am-7:00pm*
Tuesday, March 23, 2004	*8:00am-7:00pm*
Wednesday, March 24, 2004	*8:00am-11:00am*

To facilitate the registration process, the location of the registration will alternate between Bayshore foyer near Donner Pass ball room, and the City foyer near the Monterey room. In general during the plenary sessions and the panel discussion sessions, the location in Bayshore foyer will be used. During the breakup technical sessions, the location in City foyer will be used.

DOUBLETREE HOTEL





CONFERENCE AT A GLANCE

Date	Time			
Monday 3/22/04	9:00am-5:00pm	**TUTORIALS** **Compact Modeling and Analysis for Nanometer-scale CMOS Design** Room: San Carlos/San Juan		
	6:30pm-8:30pm	**Evening Panel Discussion EP1** Sponsored by PDF Solutions **DFM PDK's: Where do they belong?** Are Process Design Kits (PDKs) the answer for modern Design For Manufacturing (DFM) issues?		
Tuesday 3/23/04	8:30am-10:15pm	**PLENARY SESSION 1P** Sponsored by Synopsys **Keynote Speeches by:** **John Chilton, Marc Levitt, SY Wang**		
	10:15am-10:30am	Morning Break		
	10:30am-12:00pm	**Session 1A** Physical Design Migration Room: San Carlos	**Session 1B** CMOS device and memory Room: San Juan	**Session 1C** Poster Papers City Foyer
	12:00pm-1:00pm	**ISQED LUNCHEON AWARDS & SPEECH** **Committee Recognition Awards** **Best Paper Awards** (Sponsored by Synopsys)		
		The IP Quality Revolution Michael Keating		
	1:00pm-3:05pm	**Session 2A** Topics in printability Room: San Carlos	**Session 2B** Package design and interaction Room: San Juan	**Session 2C** Test generation and application Room: San Martin
	3:05pm-3:30pm	Afternoon Break		
	3:30pm-5:30pm	**Session 3A** Electromigration & Eletromagnetic Effects Room: San Carlos	**Session 3B** Interconnect: Capacitance extraction and delay calculation Room: San Juan	**Session 3C** Substrate noise: Analysis and prevention Room: San Martin
	6:30pm-8:30pm	**Evening Panel Discussion EP2** **IP Industry: Nordstrom or K-Mart?** **The trend toward tighter relationships between supplier and user**		
Wednesday 3/24/04	8:30am-10:15am	**PLENARY SESSION 2P** Sponsored by Magma **Keynote Speeches by:** **Hiroto Yasuura, Pierre Paulin, Krishna Saraswat**		
	10:15am-10:30am	Morning Break		
	10:30am-12:00pm	**SESSION 4A** Interconnect delay and coupling Room: San Carlos	**SESSION 4B** Analysis of variations Room: San Juan	**SESSION 4C** Layout and design techniques for quality and reliability Room: San Martin
	12:00pm-1:00pm	**LUNCH BREAK**		
	1:00pm-3:05pm	**SESSION 5A** Analog testing Room: San Carlos	**SESSION 5B** Low power design Room: San Juan	**SESSION 5C** ESD Room: San Martin
	3:05pm-3:30pm	Afternoon Break		
	3:30pm-5:30pm	**SESSION 6A** DFM design techniques Room: San Carlos	**SESSION 6B** Delay test issues Room: San Juan	**SESSION 6B** Circuit design trends in DSM Room: San Martin

TUTORIALS
San Carlos/San Juan
9:00am-4:30pm

Compact Modeling and Analysis for Nanometer-scale CMOS Design

Chair & Moderator:
***Dennis Sylvester**, University of Michigan*

This year ISQED offers a single full-day tutorial track focusing on a range of critical issues in circuit design at sub-100nm CMOS. We are pleased to have five noted experts in their respective fields (Manufacturability, Variability/Uncertainty, Advanced Devices, Low-Power Design, and Interconnect Modeling/Analysis) to present the latest research in these compelling areas.

9:00am
Part 1

Nanometer-Scale CMOS Devices

Speaker:
Kerry Bernstein
IBM T.J. Watson Research Center

This part of the tutorial will examine the operation and idiosyncrasies of emerging deep submicron CMOS devices and materials appearing in future high speed logic products. These novel structures include ultra-thin and fully depleted silicon-on-insulator devices, double-gated transistors, strained silicon, and crystal re-oriented MOSFETs. Molecular computing technologies, such as carbon nano-tubes, and new materials which extend scaling, such as high-k dielectrics, will also be explored. Circuit design issues, soft error vulnerabilities, defect mechanisms and required device model accommodations will also be discussed.

10:30am
Break

11:00am
Part 2

Interconnect Modeling

Speaker:
Jeff Davis
Georgia Tech

This tutorial will review compact VLSI interconnect models for both parameter extraction (e.g. R, L, and C) and key transient waveform characteristics (e.g. time delay, crosstalk, and overshoot). The tradeoff between model simplicity and accuracy will be explored by comparing the results of these compact models to more detailed interconnect simulations. The impact of the variability of interconnect layout geometries on the accuracy of these compact models will also be discussed. In addition, these compact models will be used to analyze a variety of VLSI interconnect circuits and structures. This analysis will include an overview of the impact of embedded low-k dielectrics on time delay and crosstalk, time delay optimizations with non-ideal repeater placements, interconnect device optimization with coplanar shield lines, and the impact of repeater insertion on inductive crosstalk.

12:00pm
Lunch

1:00pm
Part 3

Manufacturability

Speaker:
Andrew B. Kahng
University of California, San Diego

This portion of the tutorial reviews physical design complications and methodology changes – for example, in the detailed routing arena - that arise from sub-wavelength lithography and deep submicron manufacturing (antennas, metal planarization and mask-wafer mismatch). In addition, yield-constrained optimizations in PD are covered, especially “beyond corners” approaches that escape today’s pessimistic or even incorrect corner-based approaches. We also discuss current and near-term prospects for the overall design-to-manufacturing PD methodology. Key aspects include better integrations with analysis and manufacturing interfaces, as well as cost-benefit tradeoffs for “regular” layout structures that are likely beyond 90nm, cost optimizations for low volume production, and the role of robust and/or stochastic optimization in PD.

Tutorials Continued…

2:00pm
Part 4

Low-Power Design

Speaker:
Kaushik Roy
Purdue University

This section of the tutorial will present technology scaling and its impacts on dynamic and static power dissipation. Both leakage and dynamic power estimation and design techniques to reduce power dissipation in scaled technologies will be described.

3:00pm
Break

3:30pm
Part 5

Coping with Uncertainty

Speaker:
Nagib Hakim
Intel Corporation

Uncertainties from process variations, tool and model inaccuracies, as well as operating environment limit the designers ability to accurately predict product performance and power consumption. Understanding and modeling these effects would enable the development of strategies to better optimize these circuits and perform the desired power-performance tradeoff. The presentation will discuss various sources of uncertainty, their modeling, their impact on various types of circuits, and their use in product development and optimization.

Session EP1
Panel Discussion & Dinner

Sponsored by PDF Solutions

Donner Pass Room
6:30pm - 8:30pm

DFM PDK's: Where do they belong?
Are Process Design Kits (PDKs) the answer for modern Design For Manufacturing (DFM) issues?

Panel Organizer: ***Pallab Chatterjee***
SiliconMap
Panel Moderator: ***Tets Maniwa***
Editor in Chief
Chip Design Magazine

Current DSM designs require that the design methodologies be modified to accommodate the design tools chosen to implement them. This trend requires a level of EDA and general CAD methodology expertise that was previously provided by the Semiconductor design engineer, now be provided by the manufacturing partner at both the masking and fabrication/modeling level. The current solution to this shift, is to have the foundry or EDA vendor transfer a Process Design Kit (PDK) to the design house with an incorporated EDA infrastructure. This panel will address the issue of the Process Design Kits as a replacement for traditional device models and design rules and discuss the topics of quality standards for PDKs, capabilities of these "blind application" PDKs, applicability of these PDKs to the existing flow and supply chain, and level of expertise that is assumed for both creation and use of these PDKs.

Panelists:

***John Kibarian**, CEO & President, PDF Solutions*
***Nick English**, Chairman OpenKit Initiative*
***Dan Hillman**, Vice President of Business Operations and Infrastructure, Virtual Silicon*
***Richard Tobias**, Vice President ASIC and Foundry Business Unit for the System LSI Group at Toshiba America Electronic Components, Inc. (TAEC)*
***Richard Siemiakowski**, President, E*ECAD, Inc.*
***Felicia James**, Vice President and General Manager, Cadence Design Systems*
***David Lan**, TSMC*

Plenary Session 1P

Sponsored by Synopsys

Donner Pass Room

8:30AM - 10:15AM

Co-Chairs: ***Bharath Rajagopalan***
Texas Instruments
Kaustav Banerjee
University of California, Santa Barbara

8:30am
Introduction & Announcements

8:45am

Simplify: Enable Quality, Enable Innovation

John Chilton
Sr. VP and General Manager
Synopsys, Inc.

As the old sales adage goes, "Nothing happens until somebody sells something." For the semiconductor-based electronics industry, the never-ending challenge is to find and sell the next IC-based new "something" (or "somethings") that consumers just can't live without. It's an immense and extremely expensive undertaking to find/create/deliver a killer app, requiring a single-minded, undistracted business focus and an immense amount of creative design innovation. Fortunately, there is a wealth of business-savvy, creative systems companies able to meet that challenge, as long as they are free to concentrate on what drives their core competency: designing and selling exciting new business systems and consumer devices. What they need from their chip manufacturers is an agreement on specs, models, pricing, and delivery. Simple. Fortunately, there are semiconductor firms up to the challenge, as long as they are free to exercise their core mission: designing and selling faster and slicker chips, often now with software and boards attached. They need to focus on taking their customer's performance specifications and turning out a system on a chip that does exactly those things, on time and on budget. What they need from their EDA vendors are tightly integrated design tools that allow them to meet their goals of performance, price, and predictability. Simple. Unfortunately, these industries don't reflect this simplified, rosy picture… yet. The hard reality is, however, that they do have to get there, and soon, or live with dwindling prospects for the future. This presentation will discuss strategies for simplifying the semiconductor value chain, thereby enabling each segment to focus on doing well what it does best, for the sake of the future of the entire electronics industry.

9:15am

Design for Manufacturing? Design for Yield!!!

Marc Levitt
Vice President and General Manager
Cadence Design Systems, Inc.

Today's nanometer-scale designs are two orders-of-magnitude more complex than designs were in the early 1990s and are commonly manufactured with processes at or below the 130nm feature size. This has brought about a fundamental change in the way design teams must approach the release for their design data to their manufacturing partners. In the past, once a design was taped out and proven to be functional, the responsibility for ramping yield and enhancing the profitability of a design was primarily the responsibility of the manufacturing partner. This is no longer possible at 130nm and below. Once a manufacturing process has stabilized, direct action must be taken by each and every design team to "tune" their design for yield. Design-specific yield enhancement is the new frontier in EDA and while it includes the traditional Design for Manufacturing (DFM) technologies, it also covers much more. Failure to consider yield-degrading effects in IR drop, signal integrity, electro migration, and process variation will result is severe downstream problems in timing closure, functional errors during system bring-up, and the inability to achieve silicon yield and quality targets. In this talk Marc Levitt will discuss what is needed in a new generation design-for-yield tool suite to address the quality of silicon at its source.

TUESDAY

9:45am

Nanotechnology-Nanoscale Molecular Memory

Shih-Yuan (SY) Wang
Senior Scientist Quantum Science Research
Hewlett Packard Laboratories

An overview of nanotechnology research at HP Labs/ Quantum Science Research will be given with focus on nanoscale molecular memories. Densities of 100 Gb/cm2 are within reach. QSR aim is to break away from the current "scaling" down approach and look for and/or invent innovative approaches that have the potential for high volume manufacturability to break through the ITRS Red Brick Wall and push the limit of the technology. Nanofabrication challenges and possible applications will also be discussed.

10:15am
Morning Break

Session 1A

San Carlos Room
10:30AM - 12:00PM

Physical Design Migration

Chairs: ***Vamsi Srikantam****, Agilent*
Vasantha Erraguntla*, Intel*

10:30pm
Introduction

10:35am
1A.1
Calligrapher: A New Layout Migration Engine Based on Geometric Closeness
F. Fang and J. Zhu

11:05am
1A.2
Methodology for Automated Layout Migration for 90 nm Itanium®2 Processor Design
K.-K. Lin, S. Kale, and A. Nigam

11:35am
1A.3
Automatic Generation of Standard Cell Library in VDSM Technologies
M. Hashimoto, K. Fujimori, and H. Onodera

Session 1B

San Juan Room
10:30AM - 12:00PM

CMOS Device and Memory

Chairs: ***Amit Mehrotra****, University of Illinois, Urbana*
Payam Heydari*, UC-Irvine*

10:30am
Introduction

10:35am
1B.1
A Non-Charge-Sheet Based Analytical Model of Undoped Symmetric Double-Gate MOSFETs Using SPP Approach
J. He, X. Xi, M. Chan, C.-H. Lin, A. Niknejad, and C. Hu

11:05am
1B.2
Leakage Increase of Narrow and Short BCPMOS
Y. Z. Xu, O. Pohland, C. Cai, and H. Puchner

11:35am
1B.3
SRAM Leakage Suppression by Minimizing Standby Supply Voltage
H. Qin, K. Cao, D. Markovic, A. Vladimiresc, and J. Rabaey

Session 1C
City Foyer
10:00AM - 12:00PM

Poster Session

Chairs: ***Adrian Ionescu****, Swiss Federal Institute of Technology (EPFL)*
Siva Narendra*, Intel*

1C.1
Transient Analysis of On-Chip Power Distribution Networks Using Equivalent Circuit Modeling
Z. Pan, Y. Cai, S. X.-D. Tan, Z. Luo, and X. Hong

1C.2
Leveraging Delay Slack in Flip Flop and Buffer Insertion for Power Reduction
L. Simonson, K. H. Tam, L. He, and M. Mohan

1C.3
Moment Computations of Nonuniform Distributed Coupled RLC Trees
with Applications to Estimating Crosstalk Noise
H.-J. Lee, C.-C. Chu, and W.-S. Feng

1C.4
New Test Access for High Resolution SD ADC's for Noise Transfer Function Evaluation
D. De Venuto

1C.5
Design for Testability of FPGA Blocks
S. McCracken and Z. Zilic

1C.6
New Challenges Emerging on the Design of VLSI Circuits Made of MOSFETs Using New Gate Dielectric Materials
N. Konofaos and G. P. Alexiou

1C.7
Simultaneous Multiple-Vdd Scheduling and Allocation for Partitioned Floorplan
D. Kang, M. C. Johnson, and K. Roy

1C.8
Node Voltage Dependent Subthreshold Leakage Current Characteristics of Dynamic Circuits
V. Kursun and E. G. Friedman

1C.9
Automated Formal Verification of Scheduling Process Using Finite State
Machines with Datapath (FSMD)
Y. Kim and N. Mansouri

1C.10
Transistor Level Budgeting for Power Optimization
E. Kursun, S. Ghiasi, and M. Sarrafzadeh

1C.11
Resistance Matrix in Crosstalk Modeling for Multiconductor Systems
S. Yu, D. M. Petranovic, S. Krishnan, K. Lee, and C. Y. Yang

1C.12
Low Power 260k Color TFT LCD One-Chip Diver IC
B. Kim, W.-H. Lee, Y. Kim, K.-W. Park, and S.-Y. Hong

1C.13
Analysis and Reduction of On-Chip Inductance Effects in Power Supply Grids
W. H. Lee, S. Pant, and D. Blaauw

1C.14
A Variable Reduction Technique for the Analysis of Ultra Large-Scale Power Distribution Networks
J.-E. Koo, K.-H. Lee, Y.-H. Cheon, J.-H. Choi, M.-H. Yoo, and J.-T. Kong

1C.15
Rewiring for Watermarking Digital Circuits
M. M. Khan and S. Tragoudas

ISQED Luncheon Awards & Speech
Donner Pass Room
12:00pm-1:00pm

Chairs: ***Ali Iranmanesh, Anadigics***
Bharath Rajagopalan

12:05pm
Committee Recognition Awards
Best Paper Awards (Sponsored By Synopsys)

TUESDAY

12:25pm

The IP Quality Revolution

Michael Keating
Synopsys

Session 2A

San Carlos Room
1:00PM - 3:05PM

Topics in Printability

Chairs: ***Vinod Malhotra****, Synopsys*
David Overhauser*, Cadence*

1:00pm
Introduction

1:05pm
2A.1
Printability Optimization of Layout Using a Silicon Simulation Methodology
M. Cote and P. Hurat

1:35pm
2A.2
A Pattern Matching System for Linking TCAD and EDA
F. E. Gennari

2:05pm
2A.3
Shifting Methods: Adopting a Design For Manufacture Flow
J. Ferguson

Session 2B

San Juan Room
1:00PM - 3:05PM

Package Design and Interaction

Chairs: ***Ravi Mahajan****, Intel*
Erwin Cohen*, IBM*

1:00pm
Introduction

1:05pm
2B.1
Design Tools for Packaging (Invited)
Lalitha Immaneni, Anju Kapur, Brett Neal

1:35pm
2B.2
Robustness Enhancement through Chip-Package Co-Design for High-Speed Electronics
M. Shen, L.-R. Zheng, and H. Tenhunen

2:05pm
2B.3
Flip Chip Advanced Package Solder Joint Embrittlement Fault Isolation Using TDR
R. Cruz

2:20pm
2B.4
Clap: A Clustering Based Area I/O Planning For Flip-Chip Technology
J. G. Kumar, K. K. Muchherla, and J. Wang

Session 2C

San Martin Room
1:00PM - 3:05PM

Test Generation and Application

Chairs: ***George Alexiou****, University of Patras and RA-CTI*
Li-C Wang*, UC Santa Barbara*

1:00pm
Introduction

1:05pm
2C.1
Low Power Testing by Test Vector Ordering with Vector Repetition
D. Bakalis, M. Bellos, D. Nikolos, and X. Kavousianos

1:35pm
2C.2
Test Application Time Reduction for Scan Circuits Using Limited Scan Operations
Y. Cho, I. Pomeranz, and S. M. Reddy

2:05pm
2C.3
Functional Vector Generation for Combinational Circuits Based on Data Path Coverage Metric and Mixed Integer Linear Programming
J. Sosa, J. A. Montiel-Nelson, H. Navarro, and J. C. Garcia

2:35pm
Afternoon Break

TUESDAY

Session 3A
San Carlos Room
3:30PM - 5:30PM

Modeling and Simulations of Electromigration and Eletromagnetic Effects

Chairs: ***Tom Chen****, Colorado State University, Fort Collins*
James Lei*, Altera*

3:30pm
Introduction

3:35pm
3A.1
Physically-Based Simulation of Electromigration Induced Failures in Copper Dual-Damascene Interconnect
V. Sukharev

4:05pm
3A.2
A Methodology for Chip-Level Electromigration Risk Assessment and Product Qualification
C. Oh, H. Haznedar, V. Zolotov, M. Gall, A. Grinshpon, P. Ku, and R. Panda

4:35pm
3A.3
Circuit Level Reliability Analysis of Cu Interconnects
S. M. Alam, G. C. Lip, C. V. Thompson, and D. E. Troxel

5:05pm
3A.4
Modeling and Simulation of Circuit-Electromagnetic Effects in Electronic Design Flow
Pavel Nikitin, Vikram Jandhyala, Daniel White, Nathan Champagne, John D. Rockway, Richard Shi, Chuanyi Yang, Gong Ouyang, Yong Wang, Rob Sharpe, John W. Rockway

Session 3B
San Juan Room
3:30PM - 5:30PM

Interconnect: Capacitance Extraction and Delay Calculation

Chairs: ***Narain Arora****, Cadence*
Samar Saha*, Silicon Storage Technology*

3:30pm
Introduction

3:35pm
3B.1
A Divide-and-Conquer Algorithm for 3D Capacitance Extraction
W. Shi and F. Yu

4:05pm
3B.2
A Comprehensive Analytical Capacitance Model of a Two Dimensional Nanodot Array
A. Basu, S.-C. Lin, C. Wasshuber, A. M. Ionescu, and K. Banerjee

4:35pm
3B.3
Interconnect Mode Conversion in High-Speed VLSI Circuits
Y. Quéré, T. Le Gouguec, P. M. Martin, and F. Huret

5:05pm
3B.4
Efficient Capacitance Extraction for Periodic Structures by Shanks Transformation
Y. Liu, M. Xue, Z.-F. Li, and R.-F. Xue

5:20pm
3B.4
PARADE: PARAmetric Delay Evaluation under Process Variation
X. Lu, Z. Li, W. Qiu, D. M. H. Walker, and W. Shi

Session 3C
San Martin Room
3:30PM - 5:30PM

Substrate Noise: Analysis and Prevention

Chairs: ***Howard Chen****, IBM*
Charlie Chung-Ping Chen*, National Taiwan University*

3:30pm
Introduction

3:35pm
3C.1
Substrate Noise: A Modeling, Simulation, and Design Perspective (Invited)
R. Gharpurey and E. Charbon

4:05pm
3C.2
An Overview of Substrate Noise Reduction Techniques
S. Ardalan and M. Sachdev

4:35pm
3C.3
Supply and Substrate Noise Tolerance Using Dynamic Tracking Clusters in Configurable Memory Designs
M.-F. Chang, D.-M. Kwai, and K.-A. Wen

5:05pm
3C.4
Modeling of Wave Behavior of Substrate Noise Coupling for Mixed-Signal IC Design
G. Veronis, Y.-C. Lu, and R. W. Dutton

5:20pm
3C.5
Estimating Phase-Locked Loop Jitter due to Substrate Coupling: A Cyclostationary Approach
H. H. Y. Chan and Z. Zilic

Session EP2
Panel Discussion & Dinner

Sponsored by Ascend Design Automation

Donner Pass Room
6:30PM -8:30PM

IP Industry: Nordstrom or K-Mart?
The Trend Toward Tighter Relationships Between Suppliers and Users

Panel Organizer: ***Phil Dworsky,*** *Director of Marketing, DesignWare IP, Synopsys*
Panel Moderator: ***Ron Wilson,*** *Semiconductor Editor, EE Times (CMP Media Electronics Group)*

Current DSM designs require that the design methodologies be modified to accommodate the design tools chosen to implement them. This trend requires a level of EDA and general CAD methodology expertise that was previously provided by the Semiconductor design engineer, now be provided by the manufacturing partner at both the masking and fabrication/modeling level. The current solution to this shift, is to have the foundry or EDA vendor transfer a Process Design Kit (PDK) to the design house with an incorporated EDA infrastructure. This panel will address the issue of the Process Design Kits as a replacement for traditional device models and design rules and discuss the topics of quality standards for PDKs, capabilities of these "blind application" PDKs, applicability of these PDKs to the existing flow and supply chain, and level of expertise that is assumed for both creation and use of these PDKs.

Panelists:

Joachim Kunkel, *Vice President of Engineering, DesignWare, Synopsys*
Neal J. Carney*, VP of Marketing, Artisan Components*
Tim Holden, Strategic *WW EDA Vendor Relations Manager, ARM Limited Cambridge UK*
Mamta Bansal*, Manager- Foundation IP, PMC-Sierra, Burnaby, Canada*
Rafi Kedem, *Senior Director, CoreWare Technology Group, LSI Logic*
CorporationPeter Hirt*, IP Program Manager, Central R&D Group, ST Microelectronics*

Plenary Session 2P

Donner Room

8:30AM - 10:15AM

Co-Chairs: ***Ken Shepard,*** *Columbia University*
Siva Narendra, *Intel Corporation*

8:30am

Introduction & Announcements

8:45am

Digitally Named World: Challenges for New Social Infrastructures

Hiroto Yasuura
System Research Center
Kyushu University, Fukuoka, Japan

In the last three decades of the 20th century, many information and communication technologies have been developed and also introduced in social infrastructures, which are supporting our daily lives. Since the information technologies have progressed very rapidly, the basic structure of each social infrastructure, which was mostly designed in the 19th or the beginning of 20th centuries with few possibility of information technology, should be redesigned with an assumption of the existence of the advanced information technologies. Based on the high-performance SoCs (System-on-a-Chips) connected by wide-band networks, we can design next generation of social systems, which are directly related with quality of our society including individual rights and national security. In this talk, two social infrastructure information technologies are introduced. Personal Identifier (PID) system is an infrastructure for bidirectional mutual authentication, which will be used for electric commerce and governmental services. An RF-ID tag system is also important technology to implement efficient management of products and economic activities. Using PID and RF-ID tags, we can bridge a gap between the real world and the virtual one on computers automatically. We call the society, in which all persons and goods have their own digital names (identifiers) and are recognizable both in the real and virtual world, Digitally Named World. The systems require advanced technologies of SoC, networking, security and software. Here, technical challenges and social requirements for the new technologies are discussed. Some people are afraid of the infringement of their privacy in the digitally named world. Our discussions also include the technology to protect privacy and individual rights as well as efficiency and stability of our society.

9:15am

Designing High Quality, Scaleable SoC's with Heterogeneous Components

Pierre G. Paulin
Director, SoC Platform Automation
Central R&D, STMicroelectronics,
Ottawa, Canada

Today's SoC's combine an increasingly wide range of heterogenous processing elements, consisting of general purpose RISC's, DSP's, application-specific processors, and fixed or configurable hardware. Five to ten processors on an SoC is now common. A bottom-up assembly of these heterogeneous components using an ad-hoc interconnect topology, different instruction sets and embedded S/W development tools leads to unmanageable complexity and low quality. This talk will present an approach to effectively integrate heterogenous parallel components – H/W or S/W – into a homogeneous programming environment. This leads to higher quality designs through encapsulation and abstraction. This approach, supported by ST's MultiFlex multi-processing SoC tools, allows for the combination of a range of heterogeneous processing elements, supported by high-level programming models. Two programming models are supported: a distributed system object component (DSOC) message passing model, and a symmetrical multi-processing (SMP) model using shared memory. We present the results of mapping an Internet traffic management application, running at 2.5Gb/s. We demonstrate the combined use of the MultiFlex multi-processor compilation tools,

supported by high-speed hardware-assisted messaging, context-switching and dynamic task allocation in the StepNP platform.

9:45am

Performance Limitations of Devices and Interconnects and Possible Alternatives for Nanoelectronics

Krishna Saraswat
Rickey/Nielsen Professor of Engineering
Stanford University

For over three decades, there has been a quadrupling of transistor density and a doubling of electrical performance every 2 to 3 years. Si transistor technology, in particular CMOS has played a pivotal role in this. It is believed that continued scaling will take the industry down to the 35-nm technology node, at the limit of the ”long-term” range of the International Technology Roadmap for Semiconductors (ITRS). However, it is also well accepted that this long-term range of the 70-nm to 35-nm nodes remains solidly in the “no-known solution” category. The difficulty in scaling the conventional MOSFET makes it prudent to search for alternative device structures. This will require new structural, material and fabrication technology solutions that are generally compatible with current and forecasted installed Semiconductor Manufacturing. In addition, new and revolutionary device concepts need to be discovered and evolved. These can be split into two categories: one is the continued used of silicon FET-type devices but with additional materials, e.g., Ge and innovative structural aspects that deviate from the classical planar/bulk MOSFET, e.g., double gate MOSFET. The second category is a set of potentially entirely different information processing and transmission devices from the transistor as we know it, e.g. silicon-based quantum-effect devices, nano-tube electronics and molecular and organic semiconductor electronics. Continuous scaling of VLSI circuits can pose significant problems for interconnects, especially for those responsible for long distance communication on a high performance chip. Our modeling predicts that the situation is worse than anticipated in the ITRS, which assumes that the resistivity of copper will not change appreciably with scaling in the future. We show that resistance of interconnect wires in light of scaling induced increase in electron surface scattering, fractional cross section area occupied by the high resistivity barrier and realistic interconnect operation temperature will lead to a significant rise in the effective resistivity of Cu. As a result both power and delay of these interconnects is likely to rise significantly in the future. In the light of various metal interconnect limitations, alternate solutions need to be pursued. We focus on two such solutions, optical interconnects and three-dimensional (3-D) ICs with multiplicative Si layers.

10:15am
Morning Break

Session 4A

San Carlos Room
10:30AM - 12:00PM

Interconnect Delay and Coupling

Chairs: ***James Lei****, Altera*
Kris Verma*, Seagate*

10:30am
Introduction

10:35am
4A.1
A Sensitivity Based Approach to Analyzing Signal Delay Uncertainty of Coupled Interconnects
M. Kulkarni and T. Chen

11:05am
4A.2
Analytical Dynamic Time Delay Model of Strongly Coupled RLC Interconnect Lines Dependent on Switching
S. Shin, Y. Eo, W. R. Eisenstadt, and J. Shim

11:35am
4A.3
A Scalable Communication-Centric SoC Interconnect Architecture
C. Grecu, P. P. Pande, A. Ivanov, and R. Saleh

Session 4B
San Juan Room
10:30AM - 12:00PM

Analysis of Variations

Chairs: ***Enrico Malavasi****, PDF Solutions*
Sani Nassif*, IBM*

10:30am
Introduction

10:35am
4B.1
Application Specific Worst Case Corners Using Response Surfaces and Statistical Models
M. Sengupta, S. Saxena, and L. Daldoss

11:05am
4B.2
SPICE-Compatible Thermal Simulation with Lumped Circuit Modeling for Thermal Reliability Analysis Based on MEKS
T.-Y. Wang and C. C.-P. Chen

11:35am
4B.3
A Linear Fractional Transform (LFT) Based Model for Interconnect Parametric Uncertainty
J. Wang and O. Hafiz

Session 4C
San Martin Room
10:30AM - 12:00PM

Layout and Design Techniques for Quality and Reliability

Chairs: ***Marco Casale-Rossi****, ST Microelectronics*
Tanay Karnik*, Intel Corporation*

10:30am
Introduction

10:35am
4C.1
A High Performance SIMD Framework for Design Rule Checking on Sony's PlayStation 2 Emotion Engine Platform
S. Koranne

11:05am
4C.2
Exact Wiring Fault Minimization via Comprehensive Layout Synthesis for CMOS Logic Cells
T. Iizuka, M. Ikeda, and K. Asada

11:35am
4C.3
Buffered Clock Tree for High Quality IC Design
R. Chaturvedi and J. Hu

12:05pm
Lunch Break

Session 5A
San Carlos Room
1:00PM - 3:05PM

Analog Testing

Chairs: ***Jacob Abraham****, University of Texas at Austin*
Daniela De Venuto*, Polytechnic of Bari, Italy*

1:00pm
Introduction

1:05pm
5A.1
Frequency Specification Testing of Analog Filters Using Wavelet Transform of Dynamic Supply Current
S. Bhunia, A. Raychowdhury, and K. Roy

1:35pm
5A.2
A Versatile High Speed Bit Error Rate Testing Scheme
Y. Fan, Z. Zilic, and M. W. Chiang

2:05pm
5A.3
Automated Test Generation and Test Point Selection for Specification Test of Analog Circuits
A. Halder and A. Chatterjee

Session 5B
San Juan Room
1:00PM - 3:05PM

Low Power Design

Chairs: ***David Overhauser****, Cadence*
Dennis Sylvester*, University of Michigan*

1:00pm
Introduction

1:05pm
5B.1
Power Supply Optimization in sub-130 nm Leakage Dominant Technologies
M. L Mui, K. Banerjee, and A. Mehrotra

1:35pm
5B.2
Leakage Control Techniques for Designing Robust, Low Power Wide-OR Domino Logic for sub-130 nm CMOS Technologies
B. Chatterjee, M. Sachdev, and R. Krishnamurthy

2:05pm
5B.3
Low Power and High Performance Circuit Techniques for High Fan-In Dynamic Gates
G. Yang, Z. Wang, and S.-M. Kang

2:20pm
5B.4
Stacked FSMD: A Power Efficient Micro-Architecture for High Level Synthesis
K. Jasrotia and J. Zhu

Session 5C
San Martin Room
1:00PM - 3:05PM

ESD

Chairs: ***Prasun Raha****, Texas Instruments*
Enrico Malavasi*, PDF Solutions*

1:00pm
Introduction

1:05pm
5C.1
Low-Voltage-Triggered PNP Devices for ESD Protection Design in the Mixed-Voltage I/O Interface with Over-VDD and Under-VSS Signal Levels
M.-D. Ker, W.-J. Chang, and W.-Y. Lo

1:35pm
5C.2
Full-Chip Analysis Method of ESD Protection Network
S. Hayashi, F. Minami, and M. Yamada

2:05pm
5C.3
Design to Avoid the Over-Gate-Driven Effect on ESD Protection Circuits in Deep-Submicron CMOS Processes
M.-D. Ker and W.-Y. Chen

2:35pm
Afternoon Break

Session 6A
San Carlos Room
3:30PM - 5:30PM

DFM Design Techniques

Chairs: ***Sani Nassif****, IBM*
James Tschanz*, Intel*

3:30pm
Introduction

3:35pm
6A.1
Post Silicon Power/Performance Optimization in the Presence of Process Variations Using Individual Well Adaptive Body Biasing (IWABB)
J. Gregg and T. Chen

4:05pm
6A.2
Concurrent Error Detection for Combinational and Sequential Logic via Output Compaction
S. Almukhaizim, P. Drineas, and Y. Makris

4:35pm
6A.3
Cost Model Analysis of DFT Based Fault Tolerant SOC Designs
K. Sundararaman, S. Upadhyaya, and M. Margala

5:05pm
6A.4
Managing Derivative SoC Design Projects to Better Results
L. Albanese

5:20pm
6A.5
IPQ: IP Qualification for Efficient System Design
H.-J. Brand, S. Rülke, and M. Radetzki

Session 6B
San Juan Room
3:30PM - 5:30PM

Delay Test Issues

Chairs: ***Sreejit Chakravarty****, Intel*
Jayashree Saxena*, Texas Instruments*

3:30pm
Introduction

3:35pm
6B.1
Delay Fault Diagnosis Using Real Timing Information
Z. Wang, M. Marek-Sadowska, K.-H. Tsai, and J. Rajski

4:05pm
6B.2
An Adaptive Path Delay Fault Diagnosis Methodology
S. Padmanaban and S. Tragoudas

4:35pm
6B.3
Scan BIST Targeting Transition Faults Using a Markov Source
H. Lee, I. Pomeranz, and S. Reddy

5:05pm
6B.4
The Effect of Threshold Voltages on the Soft Error Rate
V. Degalahal, N. Rajaraman, N. Vijaykrishnan, Y. Xie, and M. J. Irwin

Session 6C
San Martin Room
3:30PM - 5:30PM

Circuit Design Trends in DSM

Chairs: ***Prasun Raha****, Texas Instruments*
Farid Najm*, University of Toronto*

3:30pm
Introduction

3:35pm
6C.1
FinFET SRAM—Device and Circuit Design Considerations
H. Ananthan, A. Bansal, and K. Roy

4:05pm
6C.2
High Input Voltage Step-Down DC-DC Converters For Integration in a Low Voltage CMOS Process
V. Kursun, S. G. Narendra, V. K. De, and E. G. Friedman

4:35pm
6C.3
A High Performance Radiation-Hard Field Programmable Analog Array
J. Luo, J. B. Bernstein, J. A. Tuchman, H. Huang, and K.-J. Chung

5:05pm
6C.4
The Design and Analysis of Non-Uniform Down-Sized Differential Distributed Amplifiers
A. Yazdi and P. Heydari

5:20pm
6C.5
An Asymmetric SRAM Cell to Lower Gate Leakage
N. Azizi and F. N. Najm

Thanks for attending ISQED04. We are looking forward to your participation in future events.

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