Assessing the Implications of Process Variations on Future Carbon Nanotube Bundle Interconnect Solutions

Authors Removed for Review

Abstract— **Determining the impact of process variations on nanotube-based interconnect solutions relative to standard copper technology is vital for predicting the reliability of future nanotube-based integrated circuits. In this paper, we investigate the impact of process variations on future interconnect solutions based on single-walled carbon nanotubes (SWCNT) bundles. Leveraging an equivalent RLC model for SWCNT bundle interconnect, we calculate the relative impact of ten potential sources of variation in SWCNT bundle interconnect on resistance, capacitance, inductance, and delay. We compare the relative impact of variation for SWCNT bundles and standard copper wires as process technology scales and find that SWCNT bundle interconnect will typically have larger overall 3-sigma variations in delay. In order to achieve the same percentage variation in both SWCNT bundles and copper interconnect, the percentage variation in bundle dimensions must be reduced by 63% in 22 nm process technology.**

I. Introduction

The tremendous advancement in integrated circuit manufacturing achieved over the past decade can largely be attributed to the successful scaling of CMOS technology. While transistor scaling and increased frequencies have improved overall performance, the impact of interconnect on performance and reliability has continued to increase. Traditional copper interconnect will suffer from high resistivity, electromigration, and electromagnetic interference problems as the cross-sectional area of the conductors decreases [1]. Therefore, future interconnect solutions will require alternative technologies.

Single-walled carbon nanotubes (SWCNT) have been proposed as a possible replacement for on-chip copper interconnect due to their large conductivity and current carrying capabilities [2]. SWCNTs are rolled graphitic sheets that can either be metallic or semiconducting depending on their chirality [3]. Due to their covalently bonded structure, carbon nanotubes are extremely resistant to electromigration and other sources of physical breakdown [4]. In addition, carbon nanotubes can have significantly lower resistance than standard copper interconnect, especially in global interconnect applications [5]. While SWCNTs have desirable material properties, individual nanotubes suffer from a large contact resistance that is not dependent on the length of the nanotube [6]. To alleviate this problem, bundles or ropes of SWCNTs in parallel, depicted in Figure 1, have been proposed and physically demonstrated as a possible interconnect medium [2], [5], [7].

As process technology continues to scale downward and physical interconnect dimensions become smaller, the impact of process variations on interconnect characteristics has become increasingly significant. For standard copper interconnect, multi-conductor pattern erosion and dishing within individual conductors due to chemical-mechanical polishing can have a significant impact on conductor thickness, and conductor line width may also vary due to subwavelength lithographic distortions [1], [8]. Given the manufacturing challenges associated with future nanotube-based interconnect [9]–[12], investigating the impact of the process variations associated with SWCNT bundles and comparing these sources of variation to those in copper interconnect is vital for evaluating the reliability of nanotube-based interconnect in future integrated circuits. While previous studies have evaluated the performance of nanotube-based interconnect solutions [5], [13]–[21], the performance and reliability implications of process variations on this promising technology have yet to be explored.

In this paper, we investigate the impact of process variation on future interconnect solutions based on SWCNT bundles. We first identify ten potential sources of variation for SWCNT bundles and quantify the expected statistical distribution of each type of variation based on current experimental results. Leveraging an equivalent RLC model for SWCNT bundles [5], we calculate the relative impact of each source of variation on resistance, capacitance, inductance, and delay to determine what sources of variation will be important for future nanotube bundle-based interconnect solutions. Finally, we compare the performance and reliability implications of process variations for SWCNT bundles and standard copper wires as process technology scales. Given the same amount of variation in bundle and copper wire dimensions, SWCNT bundle interconnect will typically have larger overall 3-sigma variations in delay due to the additional statistical uncertainty caused by intra and inter-bundle variations in individual nanotube properties. To achieve the same percentage variation in both SWCNT bundles and copper interconnect, the percentage variation in SWCNT bundle interconnect dimensions must be reduced by 63% in 22 nm process technology.

II. Capturing Process Variations for SWCNT Bundle Interconnect

A. Modeling SWCNT Bundles

To evaluate SWCNT bundles for interconnect in future VLSI applications, we utilize the circuit model from [5], which

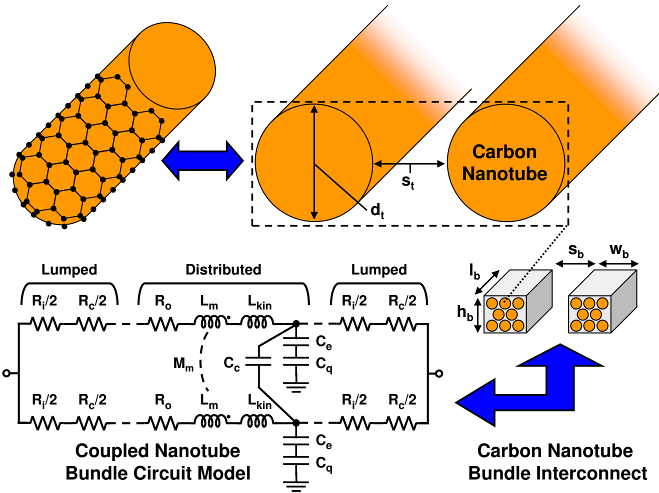

Fig. 1. SWCNT bundle interconnect geometric parameters and circuit model.

is displayed in Figure 1. Each SWCNT has lumped ballistic ($R_i \approx 6.5\ k\Omega$) and contact (R_c) resistances that have fixed values regardless of the length of the nanotube bundle (l_b). The contact resistance is due to imperfect SWCNT-metal contacts, which are typically constructed using Gold, Palladium, or Rhodium [22]. Contact resistance has the largest impact when l_b is relatively short. The nanotubes also have a distributed ohmic resistance (R_o), which is determined by l_b and the mean free path of acoustic-phonon scattering (λ_{ap}) in the individual nanotubes. Since the individual SWCNTs have a maximum saturation current (I_o), the overall resistance also depends on the applied bias voltage ($R_{hb} = V_{bias}/I_o$) [6].

The diameter of the individual nanotubes in the bundle plays an important role in determining the resistance of SWCNT bundle interconnect. For ohmic resistance, λ_{ap} is proportional to the individual nanotube's diameter (d_t) [14]. Recent experimental results have revealed that the contact resistance of a SWCNT greatly increases when $d_t < 2.0\ nm$ [22]. In addition, I_o substantially decreases to approximately $5\ \mu A$ for $d_t = 1\ nm$ [22], which increases the overall impact of R_{hb}. In contrast, as d_t decreases, the number of nanotubes in the bundle (n_b) increases, which decreases the overall ohmic and contact resistances for the bundle. Therefore, for relatively short length bundles, a trade-off exists between minimizing increases in R_c and R_{hb} for individual nanotubes due to decreases in d_t and increasing n_b by reducing d_t. We exploit the aforementioned trade-off to locate the optimal d_t value to minimize R_{bundle} for a particular l_b value [14]. For longer l_b values where contact resistance is insignificant, we assume that $d_t = 0.8\ nm$ since nanotubes with diameters on the order of 0.8 to 1.0 nm have demonstrated both mechanical stability and good electrical conductivity [23]. Note that we utilize the diameter-dependent resistance model from [14] to characterize the resistance associated with SWCNT bundles.

The capacitance of a nanotube bundle consists of both a quantum capacitance and an electrostatic capacitance [16]. The quantum capacitance has relatively little impact on the SWCNT bundle as n_b is increased [17]. The electrostatic capacitance between adjacent conductors and to the ground plane depends on the bundle geometry and the spacing between bundles and can be modeled using the techniques from [5]. In addition to the capacitance, SWCNTs have both magnetic (L_m) and kinetic (L_k) inductances, which can be modeled using the scalable inductance model from [15]. The kinetic inductance depends on n_b while the magnetic inductance primarily depends on the geometry of the bundle and its current return paths. In order to calculate the delay associated with SWCNT bundle interconnect, we utilize the delay model presented in [24] with driver and load transistor parameters from various nodes in the 2005 International Technology Roadmap for Semiconductors (ITRS) [1]. Using the circuit model, we can evaluate SWCNT bundle interconnect for future VLSI applications.

B. *Sources of Variation*

For future interconnect solutions based on SWCNT bundles, we have identified 10 possible sources of manufacturing variation, which are depicted in Figure 2. The potential sources of variation include (a) the probability that a given nanotube is metallic; (b) inter-bundle variation in the spacing between individual nanotubes; (c) intra-bundle variation in individual nanotube diameter; (d) inter-bundle variation in average individual nanotube diameter; (e) intra-bundle variation in contact resistance for individual nanotubes; (f) inter-bundle variation in average contact resistance; (g) intra-bundle variation in mean free path of acoustic and optical phonon scattering effecting both λ_{ap} and I_o; (h) variation in dielectric thickness between interconnect layers of nanotube bundles; (i) variation in bundle width values; and (j) variation in bundle height values. Note that the last three listed sources of variation [(h)-(j)] are also present for standard copper interconnect in scaled process technologies.

1) Distribution of Metallic Nanotubes in the Bundle: One of the most critical challenges to realizing high performance SWCNT-based interconnect is controlling the proportion of metallic nanotubes in the bundle. Current SWCNT fabrication techniques cannot effectively control the chirality of the nanotubes in the bundle [9]–[12]. Therefore, SWCNT bundles have metallic nanotubes that are randomly distributed within the bundle as depicted in Figure 2a. With no special separation techniques, the metallic nanotubes are distributed with probability $P_m = 1/3$ since approximately one-third of possible SWCNT chiralities are metallic [3]. The impact of the probability that a given nanotube is metallic (P_m) on SWCNT bundle resistance, inductance, and delay has been the subject of several studies [5], [13]–[15], [20]. P_m may cause reliability problems in SWCNT bundle interconnect since n_b decreases as the cross-sectional dimensions of the bundle are reduced [5]. Techniques such as alternating current (AC) dielectrophoresis [25], sequence-dependent DNA assembly [26], and ion-exchange chromatography [27] have the potential to increase the proportion of metallic nanotubes, which could reduce the impact of this source of variation.

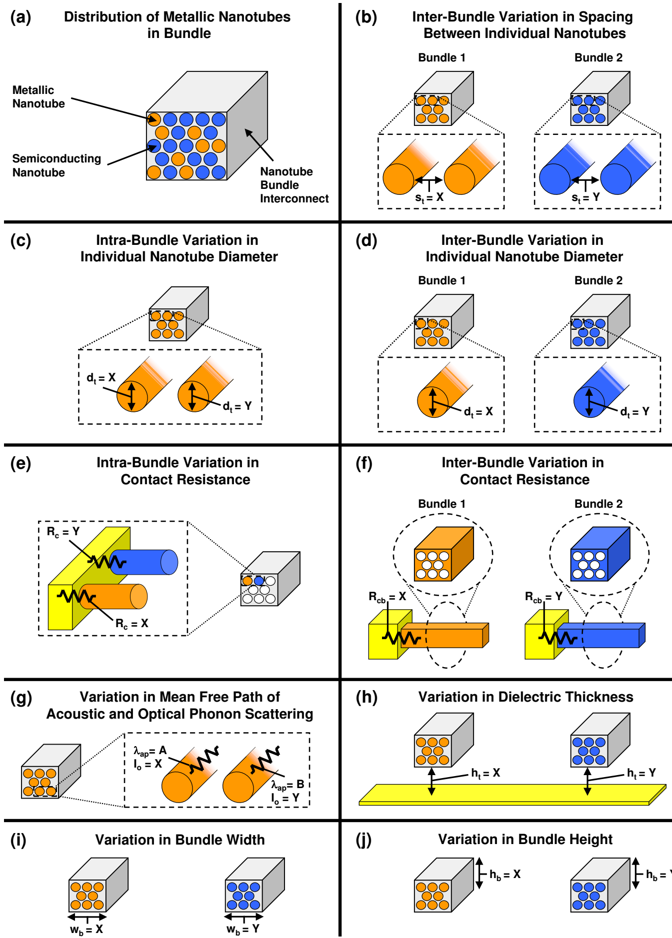

Fig. 2. Sources of variation in SWCNT bundle interconnect include (a) the probability that a given nanotube is metallic; (b) inter-bundle variation in the spacing between individual nanotubes; (c) intra-bundle variation in individual nanotube diameter; (d) inter-bundle variation in average individual nanotube diameter; (e) intra-bundle variation in contact resistance for individual nanotubes; (f) inter-bundle variation in average contact resistance; (g) variation in mean free path of acoustic and optical phonon scattering effecting both λ_{ap} and I_o; (h) variation in dielectric thickness between interconnect layers; (i) variation in bundle width values; and (j) variation in bundle height values.

2) Individual Nanotube Diameter and Spacing Variation: The individual nanotube diameters (d_t) and spacing between nanotubes in the bundle (s_t), depicted in Figures 2(b)-(d), are also potential sources of variation for SWCNT bundle interconnect. We consider the impact of both variations of d_t within a single bundle (intra-bundle) and between bundles (inter-bundle). Intra-bundle d_t variation has been reported to be relatively small with typical measured 3-sigma percentage variations of 4.4% [7], [11]. The small intra-bundle d_t variation can be attributed to the physical formation of the nanotube bundles during either laser ablation or arc-discharge evaporation [7], [11]. Significantly larger values of inter-bundle d_t variation are present during the SWCNT bundle fabrication process. Reported 3-sigma percentage variations ranging from 20% to 60% have been reported [28]–[30]. The spacing between nanotubes in the bundle is due to the Van der Waals forces between the atoms in adjacent nanotubes [7], [11]. Therefore, variations in intra-bundle s_t should be relatively small. Nanotube spacing between 0.315 and 0.340 nm have been reported [7], [11]. Based on the range of reported values, we assume that the 3-sigma percentage inter-bundle variation in s_t is 23%.

3) Variation in Mean Free Path and Contact Resistance: Defects in the chiral structure of metallic carbon nanotubes can significantly alter the mean free path of both acoustic-phonons (λ_{ap}) in the low bias voltage regime ($V < 0.1V$) and optical-phonons (λ_{op}) in the high bias voltage regime, which can impact the saturation current of the individual nanotubes (I_o). These defects can cause uncertainty in the ohmic (R_o) and high bias (R_{hb}) resistances of the individual SWCNTs in the bundle as depicted in Figure 2g. Variations in the resistance due to imperfect metal-SWCNT contacts (R_c) can be caused by statistical uncertainty in the quality of the overall nanotube bundle-metal contact (Figure 2e) or uncertainty in the quality of contacts between each individual nanotube in the bundle (Figure 2f). Since detailed information on the statistical distribution of ohmic and contact resistances has not appeared in the experimental literature, we assume that variations in λ_{ap}, I_o, and R_c have the same 3σ values as the reported diameter distribution, 50%, since the nanotube diameter and the ohmic, contact, and high bias resistances are related [14].

4) Variation in Bundle Dimensions: Variations in bundle width (w_b), height (h_b), and dielectric thickness (h_t), depicted in Figures 2(h)-(j), can impact the resistance, capacitance, inductance, and delay of nanotube bundle-based interconnect. Unlike the aforementioned sources of variation, variations in conductor dimensions also impact standard copper interconnect in scaled process technologies. Multi-conductor pattern erosion and dishing within individual conductors due to chemical-mechanical polishing (CMP) can have a large impact on conductor thickness with 3-sigma variations of up to 35% for future process technologies [1], [31]. Dielectric thickness variations can also result due to the CMP process. Variations in conductor width can occur due to lithographic errors [8]. For SWCNT bundles, the percentage variation in bundle dimensions has not been experimentally investigated in the literature. Therefore, we assume that the percentage variation in bundle dimensions is equivalent to the predicted values for copper interconnect in [1]. Variations in bundle dimensions must be controlled more precisely in future SWCNT based interconnect than they are in standard copper interconnect to achieve the same overall percentage variation in resistance, capacitance, inductance, and delay since SWCNT-based interconnect will also be affected by the aforementioned sources of variation in the individual nanotube characteristics.

C. Simulation of Variation

In order to identify the relative importance of each possible source of variation on future nanotube-based interconnect solutions, we have performed an extensive set of Monte Carlo simulations using the circuit model described in Section II-A to analyze the impact of each variation on resistance, capacitance, kinetic inductance, magnetic inductance, and de-

TABLE I

PREDICTED VARIATIONS IN SWCNT BUNDLE PROCESS PARAMETERS, RLC CHARACTERISTICS AND DELAY

		3σ percentage variation in interconnect characteristics					Delay distribution type	
Variation type	Geometric variation	Resistance	Capacitance	Kinetic inductance	Magnetic inductance	Delay	Global interconnect	Local interconnect
Probability nanotube is metallic (P_m)	$P_m = 1/3$	13.42	0.14	13.41	0	12.55	Gaussian	
Inter-bundle nanotube spacing (s_t)	$3\sigma = 23\%$	7.76	0.08	7.76	0	7.25	Gaussian	
Intra-bundle nanotube diameter (d_t)	$3\sigma = 4.4\%$	0.24	0	0	0	0.22	Gaussian	
Inter-bundle nanotube diameter (d_t)	$3\sigma = 50\%$	32.33	0.87	8.30	0	29.71	Gaussian	Lognormal
Intra-bundle contact resistance (R_c) - Global	$3\sigma = 50\%$	0.03	0	0	0	0.03	Gaussian	
Intra-bundle contact resistance (R_c) - Local	$3\sigma = 50\%$	1.06	0	0	0	0.41	Gaussian	
Inter-bundle contact resistance (R_c) - Global	$3\sigma = 50\%$	0.66	0	0	0	0.62	Gaussian	
Inter-bundle contact resistance (R_c) - Local	$3\sigma = 50\%$	19.03	0	0	0	7.40	Gaussian	
Intra-bundle mean free path (λ_{ap} and I_o) - Global	$3\sigma = 50\%$	2.90	0	0	0	2.74	Gaussian	
Intra-bundle mean free path (λ_{ap} and I_o) - Local	$3\sigma = 50\%$	2.23	0	0	0	0.87	Gaussian	
Inter-bundle dielectric thickness (h_t)	$3\sigma = 32\%$	0	13.25	0	0	12.61	Gaussian	
Inter-bundle width (w_b)	$3\sigma = 32\%$	34.12	7.83	34.12	3.11	24.46	Slight lognormal	
Inter-bundle height (h_b)	$3\sigma = 32\%$	33.40	6.20	33.39	2.49	25.39	Slight lognormal	

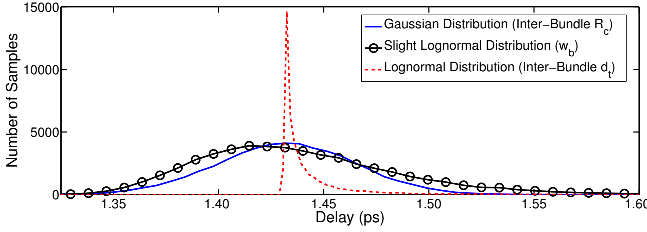

Fig. 3. Types of delay distributions that result from process variations for SWCNT bundles.

lay. Note that do not simulate process variations in driver parameters to highlight the relative effect of process variations on SWCNT bundles and copper interconnect. When possible, we have utilized sources in the literature to determine the expected standard deviation of each type of variation, which is listed in Table I and described in the preceding sections.

For sources of variation that vary inter-bundle [(b), (d), (f), (h) - (j) in Figure 2], we determine the mean and standard deviation of the SWCNT interconnect properties from a large number of simulated bundle geometries. We assume that the inter-bundle process parameter variations are normally distributed since reported experimental inter-bundle d_t values have this distribution [28]–[30]. To capture the relationship between the process parameters, we apply each source variation in a hierarchical manner. For each statistical sample in the Monte Carlo simulation, we first determine the inter-bundle w_b, h_b, h_t, d_t, s_t, and R_c values from their respective distributions. This sets the n_b value for the sampled nanotube bundle interconnect. We then apply the probability distributions for the intra-bundle sources of variation [(a), (c), (e), (g) in Figure 2] to each individual nanotube in the bundle for each of the sample bundle geometries in the Monte Carlo simulation. With the exception of the probability that a given nanotube is metallic, we assume that the intra-bundle variations are also normally distributed. When simulating both inter and intra-bundle variations, we assume that the sampled inter-bundle value is the mean for the intra-bundle distribution.

III. EFFECT OF INDIVIDUAL PROCESS VARIATIONS

Table I displays the 3-sigma variation in SWCNT bundle RLC characteristics and propagation delay for each of the ten potential sources of process variation. We utilize the process parameters from the 2016 node of [1] (22 nm technology) and assume a 22 nm bundle width. The SWCNT bundles are 1 mm long unless specified as local interconnect, in which case the bundles are 10 μm long. Three different types of delay distributions, depicted in Figure 3, result from the variation in the nanotube bundle process parameters. For sources of variation that only impact either resistance or capacitance, the resulting delay distribution is approximately Gaussian. Variations in nanotube bundle width and height produce slightly lognormal distributions that are almost normally distributed since both the resistance and capacitance are simultaneously varying. The variation in delay due to inter-bundle d_t for local interconnect applications has a strong lognormal distribution that does not closely match a standard normal distribution since the optimal d_t value is greater than the minimum d_t value due to the diameter-dependence of the bundle's contact resistance. Therefore, variations that either increase or decrease the diameter of the nanotubes in the bundle both cause the bundle delay to increase. For global interconnect applications, the minimum nominal diameter is the optimal diameter since the contact resistance has only a small impact, and therefore, decreases in diameter due to process variations improve the bundle delay.

In 22 nm technology, the inter-bundle sources of variation have a significantly larger impact than the intra-bundle variation in nanotube characteristics with the exception of variations due to P_m. Inter-bundle variations that effect n_b have a large impact on the resistance of the nanotube bundle. Note that while the resistance plays a large role in determining the delay of the bundle, the kinetic inductance has a much smaller role despite its large nominal value since $R \gg \omega L_k$ for the simulated nanotube bundle geometries [13]. Furthermore, recent experimental and theoretical studies [32]–[34] have demonstrated that the per unit length value of kinetic inductance may be significantly lower than the value predicted

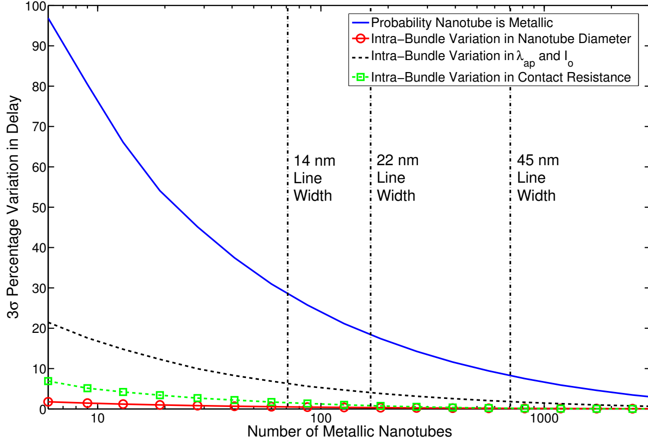

Fig. 4. Percentage 3-sigma delay variation versus n_b for several sources of intra-bundle process variation.

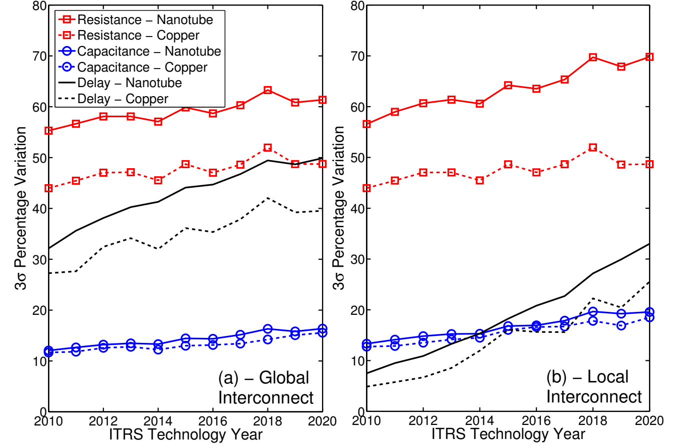

Fig. 5. Percentage 3-sigma variation in resistance, capacitance, and delay versus the ITRS technology year for SWCNT bundles and standard copper interconnect for both (a) global and (b) local interconnect applications.

in [16] for typical interconnect geometries. Variations in magnetic inductance are relatively small since it primarily depends on the overall current loop and has only a second order dependence on conductor dimensions [35]. Only variations in bundle dimensions cause significant statistical variation in capacitance since the capacitance is primarily determined by the spacing between the bundles and the total surface area of the bundle.

In general, intra-bundle sources of variation have a relatively small impact on SWCNT bundle delay since they vary for each nanotube in the bundle and the bundle typically contains a large number of nanotubes. Since the impact of intra-bundle sources of variation is dependent on n_b, they will become more significant as process technology scales and as the conductor's cross-sectional area decreases. Figure 4 displays the percentage 3-sigma delay variation versus n_b for several sources of intra-bundle variation. Intra-bundle variations in d_t, λ_{ap}, I_o, and R_c for both local and global interconnect applications cause less than 10% 3-sigma variation in delay for 2020 node in [1] ($w_b = 14\ nm$). Therefore, these sources of variation will be relatively insignificant for nanotube bundles with the predicted interconnect dimension in future process technologies. In contrast, delay variation due to P_m can be large with up to 30% 3-sigma variation possible for the interconnect geometries predicted by ITRS assuming $P_m = 1/3$. P_m causes significantly more variation since a given nanotube either has metallic conduction properties or does not contribute to the conduction. This results in a large effective variation in the resistance of the individual nanotubes.

IV. Comparison Between Variations in SWCNT and Copper Interconnect

In order to effectively determine the suitability of SWCNT bundles as a replacement for copper interconnect, we must analyze the relative impact of process variations on nanotube-based interconnect solutions and scaled copper interconnect in future process technologies. Since SWCNT bundles will suffer from sources of process variation that are inherently present in the nanotubes, nanotube-based interconnect will typically experience greater overall variation in resistance, capacitance, and delay than scaled copper interconnect assuming that the percentage variation in conductor dimensions for both technologies is equivalent. Therefore, additional control over conductor dimensions in SWCNT bundles will be required to achieve the same level of variation that is predicted for scaled copper interconnect. This is crucial for ensuring that SWCNT bundle interconnect has the same level of reliability as scaled copper interconnect with respect to process variation in future process technologies.

A. Combined Impact of All Sources of Variation

Figure 5 displays the 3-sigma percentage variation in resistance, capacitance, and delay versus the ITRS technology year for SWCNT bundles and standard copper interconnect for both global and local interconnect applications. The difference in resistance variation between SWCNT bundles and copper interconnect is significantly larger than it is for capacitance since the nanotube-specific sources of variation primarily impact resistance. In both the local and global interconnect cases, the interconnect resistance is becoming larger relative to the driver resistance as technology scales. This accounts for the overall increase in delay variation as process technology scales. In the more near-term current nodes of the ITRS roadmap, the percentage difference in 3-sigma delay variation between SWCNT bundles and copper interconnect stays relatively constant since inter-bundle sources of variation, which do not depend on the bundle dimensions, dominate the intra-bundle sources of variation as described in Section III. In the long-term ITRS nodes, the differences between SWCNT bundle and copper interconnect variations increases since n_b becomes small as the bundle dimensions scale, which increases its impact for SWCNT bundle interconnect.

For the local interconnect cases simulated in Figure 5, the percentage variation in delay for SWCNT bundles is larger than that of scaled copper interconnect. However, increasing

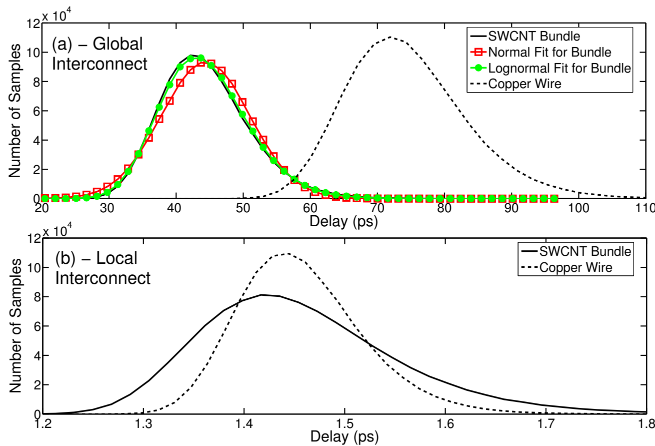

Fig. 6. Distribution of delay values for SWCNT bundles and standard copper wires for (a) global and (b) local interconnect in 22 nm technology. Note that the distributions are slightly skewed Gaussian distributions, which can be fit to a lognormal distribution.

the driver resistance through device sizing or decreasing the SWCNT bundle resistance due to changes in P_m can result in cases where the delay variation of SWCNT-based solutions is less than that of copper interconnect. For instance, if P_m is increased from 1/3 to 0.6, the absolute difference in the 3-sigma percentage variation in delay between SWCNT bundles and copper interconnect in the 2016 node of ITRS changes from 5% to -2%. If P_m is increased to 0.9, then the absolute difference in the 3-sigma percentage variation in delay between SWCNT bundles and copper interconnect becomes -5%. Consequently, copper interconnect can have significantly greater delay variation than SWCNT bundles when the mean resistance value for SWCNT bundles is significantly lower than it is for scaled copper interconnect relative to the driver resistance.

Figure 6 displays the distribution of delay values for SWCNT bundles and standard copper wires in 22 nm technology. In 22 nm technology (2016 node of ITRS), the 3-sigma variation in delay increases from 35% to 44% in global interconnect and from 15% to 21% in local interconnect. Note that the distributions are slightly skewed Gaussian distributions due to the lognormal distributions that result from variations in conductor dimensions. The delay distribution can be almost perfectly fit to a lognormal distribution and closely matches a standard Gaussian distribution. Since SWCNT bundles will experience greater overall variation than scaled copper interconnect, additional control over the bundle's dimensions will be required to achieve the same level of delay variation that is predicted for scaled copper interconnect.

B. Required Control of SWCNT Bundle Dimensions

To achieve the same level of delay variation as scaled copper interconnect, the sources of variation in SWCNT bundles must be effectively controlled. While controlling the nanotube-specific properties of SWCNT bundles could provide one mechanism to reduce the impact of process variations, achieving greater control over the individual nanotube properties during the SWCNT bundle fabrication process remains an difficult challenge [9]–[12]. Therefore, controlling the variation in the dimensions of the nanotube bundles will probably provide a feasible means for reducing the impact of process variations on nanotube characteristics. Figure 7 depicts the behavior of the 3-sigma percentage delay variation versus the 3-sigma variation in bundle dimensions, including dielectric thickness, for both global and local interconnect applications in future process technology. As expected, reducing the percentage variation in bundle dimensions decreases the overall variation in delay for both global and local interconnect as depicted in Figures 7a and 7d. Furthermore, the trend of larger percentage variations as process technology scales, which was discussed in Section IV-A, exists for both SWCNT bundles and copper interconnect as displayed in Figures 7a, 7b, 7d, and 7e.

Figures 7c and 7f depict the percentage difference in delay variation between SWCNT bundles and copper interconnect for both local and global interconnect applications for different values of bundle dimension variation. Note that the ITRS predicted percentage 3-sigma variation in conductor dimensions increases from 30% to 35% from the 2010 to 2018 nodes and then decreases slightly to 33% in the 2019 and 2020 nodes [1]. As process technology scales, the decrease in percentage bundle dimension variation needed to make SWCNT and copper interconnect delay variation equivalent remains relatively constant until the 2018 node in ITRS. For these technologies, the absolute reduction in bundle dimension variation required for global interconnect is approximately 12%, which is a 40% relative reduction in conductor dimension variation between SWCNT bundle and copper interconnect. For local interconnect, the required absolute reduction in bundle dimension variation increases due to the increased impact of inter-bundle contact resistance variations to approximately 19%, which is a 63% relative reduction in conductor dimension variation. Beyond the 2018 node, the required absolute reduction in bundle dimension variation increases for both global and local interconnect due to the increasing impact of intra-bundle variations in resistance due to P_m. Based on the results displayed in Figure 7, controlling the impact of process variations for SWCNT bundles is crucial for ensuring that nanotube-based interconnect has a similar level of reliability as scaled copper interconnect with respect to process variation in future technologies.

C. Fabrication Challenges for Reducing Process Variation in SWCNT Bundles

Manufacturing solutions for SWCNT bundle interconnect will ultimately dictate what sources of variation can be controlled to reduce the overall variation compared to scaled copper interconnect. Controlling intra-bundle variations in d_t, R_c, λ_{ap}, and I_o will likely be difficult since this will require fine-grain control of the individual nanotube properties including the characteristics of the nanotubes in the interior of the bundle, which cannot be physically accessed without removing the nanotubes from the bundle [36], [37]. However,

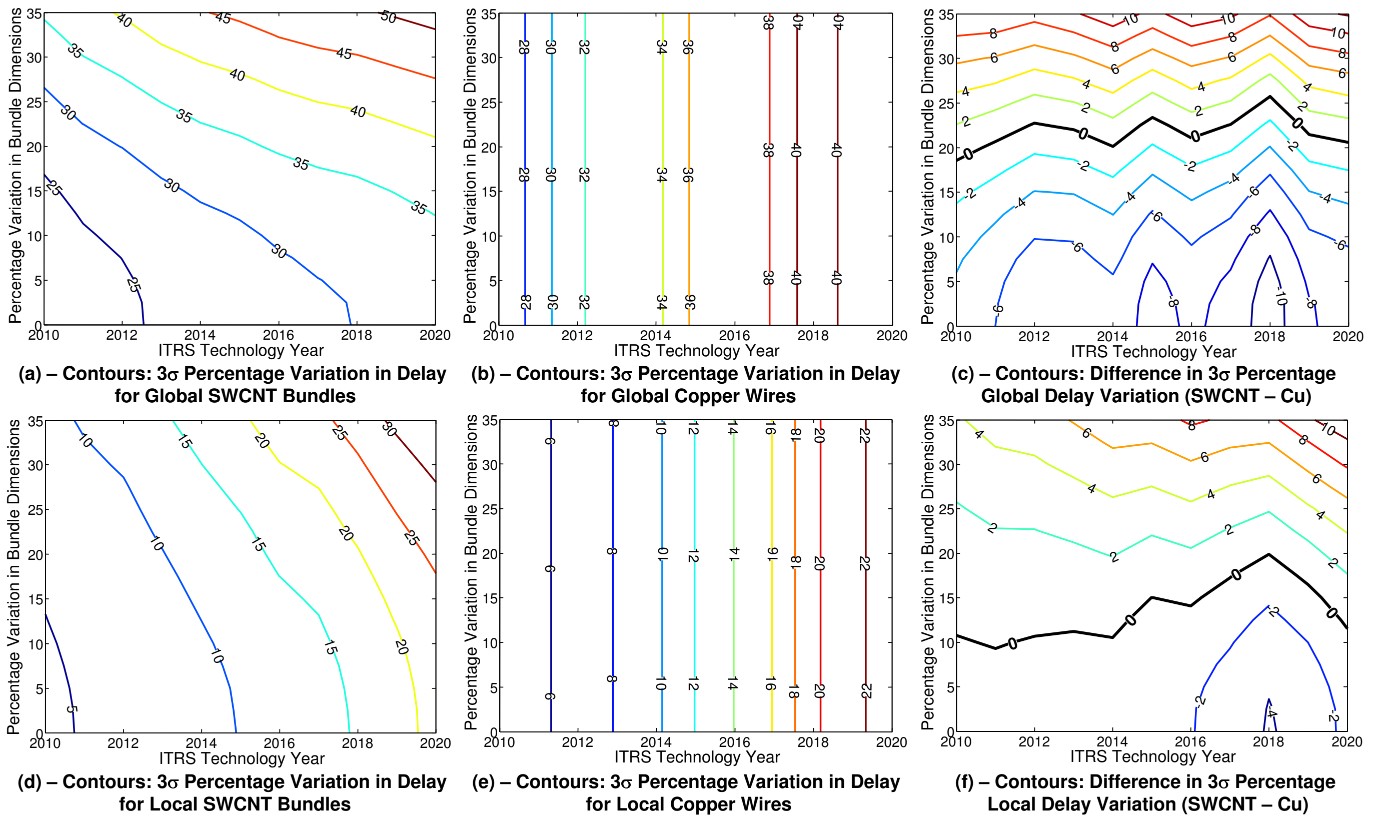

Fig. 7. Behavior of 3-sigma percentage variation in delay versus the ITRS technology node and the 3-sigma percentage variation in bundle dimensions for the following cases: (a) global SWCNT bundle interconnect; (b) global copper interconnect; (c) difference between delay variation in global SWCNT bundles and copper interconnect; (d) local SWCNT bundle interconnect; (e) local copper interconnect; and (f) difference between delay variation in local SWCNT bundles and copper interconnect.

since these sources of variation have a relatively low impact on the overall delay variation for SWCNT interconnect bundles with predicted geometric dimensions as depicted in Figure 4, controlling these intra-bundle sources of variation is not critical. In contrast, recent progress in SWCNT fabrication techniques has the potential to significantly reduce intra-bundle variations due to P_m, which can have a large impact on overall delay variation. Among potential metallic nanotube separation techniques [25]–[27], AC dielectrophoresis is a particularly promising solution since it generates bundles of metallic nanotubes by construction. By adjusting the frequency of the current between the electrodes in the dielectrophoresis process, the simultaneous synthesis of a hundreds of SWCNT bundles with a high percentage of metallic nanotubes has been reported [25]. This could essentially eliminate process variation due to P_m while significantly decreasing the overall resistance of SWCNT bundle interconnect [14].

Reducing the effect of inter-bundle sources of process variation will most likely provide a more tractable solution to reducing the impact of statistical uncertainty on SWCNT bundle interconnect performance since controlling inter-bundle sources of variation requires less fine-grain control of individual nanotube properties than it does for intra-bundle process variations. Significant research efforts have been devoted to reducing the inter-bundle variation in d_t with 3-sigma variation as low as 20% reported [28]–[30]. Since this source of process variation can have a significant impact on the overall variation in delay as displayed in Table I, controlling it will be crucial. Variation in inter-bundle s_t values will most likely be correlated with inter-bundle variations in d_t since s_t depends on the Van der Waals forces between the atoms in adjacent nanotubes [7], [11]. Therefore, reducing the percentage variation in inter-bundle d_t should also reduce the variation in s_t. It should also be feasible to reduce the percentage variation in the nanotube bundle dimensions since these dimensions are closely related to environmental conditions and catalyst properties during the SWCNT fabrication process [9], [38], [39]. Therefore, advances in SWCNT fabrication technology have to potential to reduce the impact of inter-bundle process variations on the statistical uncertainty of SWCNT bundle interconnect performance, which could lead to similar or even reduced levels of performance variation relative to that of scaled copper interconnect in future process technologies.

V. Conclusion

In this paper, we investigate the impact of the sources of process variation on resistance, capacitance, inductance, and delay for future interconnect solutions based on carbon nanotube bundles. We find that SWCNT bundle interconnect will typically have larger overall 3-sigma variations in delay

due to the additional statistical uncertainty caused by intra and inter-bundle variations in individual nanotube properties. In order to achieve the same percentage variation in both SWCNT bundles and copper interconnect, the percentage variation in bundle dimensions must be reduced by 63% in 22 nm process technology. Therefore, to realize nanotube-based interconnect with suitable performance and reliability, significant control over conductor dimensions and other inter-bundle sources of process variation in SWCNT bundles will be required in high performance VLSI applications as process technology scales.

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