Final Program

ISQED

2021
22nd International Symposium on

QUALITY ELECTRONIC DESIGN

AI/ML. Autonomous Vehicles. Security.
IoT. Quantum Computing.

April 7-9, 2021
Virtual Conference
California Pacific Daytime
San Jose, CA USA

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ISQED'21 is produced and sponsored by the
International Society for Quality Electronic Design

WELCOME TO ISQED'21

On behalf of the ISQED conference and technical committees, we are pleased to welcome you to the 22nd anniversary of the International Symposium on Quality Electronic Design, ISQED'21.

For the past 22 years, ISQED has been the leading voice and pioneer in Quality Electronic Design (QED). With the drastic increase in complexity of semiconductor technology and design, following QED and its underlying principles are becoming more necessary and essential as never before. ISQED'21 strives to lead the community in that direction with a comprehensive program consisting of keynotes, panel, tutorials, and over 100 peer-reviewed articles.

The conference is held in Virtual format, with the technical sponsorship of the IEEE Electron Devices Society, the IEEE Circuits and Systems Society, IEEE Reliability Society, and In-cooperation with ACM/SigDA. Conference proceedings & Papers will published in IEEE Xplore digital library and indexed by Scopus.

ISQED'21 is organized around the important trends in AI/ML, Autonomous Vehicles, Security, IoT, and Quantum Computing. The conference program consists of two keynote talks, four embedded tutorials and a panel discussion, and many Peer-reviewed technical papers with focus on these timely and hot topics.

We are pleased to see an increase in the number of papers submitted to the conference this year. The two- and half-day technical program with four parallel sessions packs over 100 peer-reviewed papers highlighting the latest trends in electronic circuit and system design & automation, testing, verification, sensors, security, semiconductor technologies, cyber-physical systems, etc.

All technical presentations, plenary sessions, panel discussions, tutorials and related events will take place on April 7-9, conducted virtually, at Pacific Daylight Time (PDT).

We would like to thank the ISQED'21 corporate sponsors: Synopsys, Siemens EDA, and Innovotek for their valuable financial support of this conference. Welcome to another exciting year of ISQED and thanks for your support and participation.

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ISQED'21 Best Papers

3B.3

Six-track Standard Cell Libraries with Fin Depopulation, Contact over Active Gate, and Narrower Diffusion Break in 7nm Technology

Tzu-Hsuan Wang, Chih-Chun Hsu, Li Kao, Bing-Yu Li, Tung-Chun Wu, Tsao-Hsuan Peng, Rung-Bin Lin

Yuan Ze University, Taoyuan City, Taiwan

1A.2

Design Space Extrapolation for Power Delivery Networks using a Transposed Convolutional Net

Osama Waqar Bhatti[1], and Madhavan Swaminathany[2]

[1]School of Electrical and Computer Engineering

[2]School of Material Science and Engineering

3D Systems Packaging Research Center, Georgia Institute of Technology, Atlanta, USA

BEST WIP PAPER

PW4.4

Large-Scale Quantum System Design on Nb-based Superconducting Silicon Interconnect Fabric

Yu-Tao Yang, Subramanian S. Iyer

Department of Electrical and Computer Engineering

University of California, Los Angeles (UCLA)

Authors of best papers are acknowledged on Wednesday April 7.

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GENERAL INFORMATION
ISQED'21

April 7-9, 2021
Pacific Daylight Time (PDT)
Virtual Event

AWARDS & RECOGNITIONS

Wednesday April 7, 9:00 AM - 9:20 AM
Track G

Best Paper Awards

Recipients of the ISQED'21 Best Paper Awards will be recognized in this segment of the program. The best papers are shown in Page 2 of this document.

Keynotes

Wednesday, April 7, 9:20 AM - 9:55 AM
Track G

Confluence of AI/ML with EDA and Software Engineering

Arun Venkatachar
Vice President, Artificial Intelligence and Central Engineering
Synopsys

Thursday April 8, 9:00 AM - 9:35 AM
Track G

Cars Driving Chips or Chips Driving Cars?

Ravi Subramanian, Ph.D
Senior Vice President - IC Verification
Siemens EDA

Panel Discussion

Wednesday, April 7, 12:55 PM - 2:25 PM
Track G

State of Autonomous Vehicle Development: Moving Forward with Safe Cars

The automotive industry is going through a disruptive phase and one of the major factors causing this disruption is autonomous cars. The digitalization of the automotive industry is changing the traditional patterns of transport and mobility, and connected vehicles, self-driving vehicles, and vehicles that are increasingly connected to the internet and equipped with electromechanical controls are defining some of today and most of the future automotive industry. Though there is strong demand from users, how realistic is the future of autonomous vehicles? Is the safety of autonomous cars an issue for drivers and will potential safety issues cause the autonomous vehicle development to crash? Is the mobility trend shifting towards ride sharing? What new challenges and opportunities do driverless cars bring to the microelectronic industry? What are the safety and security constraints? What are the implications of the inclusion of AI hardware and software? Join us to listen to our panelist's thoughts on the subject.

Panelists:
Nirmal R. Saxena - NVIDIA
Lee Harrison - Mentor, A Siemens Business
James Herman - CMU/Roborace
Sweta Mehta - Tata Consultancy Services
Srijani Dey - DXC Technology

Moderator:
Aditya Sharma - Microsoft (Chair)

Chairs:
Shigeki Tomishima - Intel Corporation (Chair)
Siddha Ganju - Nvidia (Co-Chair)

Embedded Tutorials

Chair & Moderators:
José Pineda de Gyvez - NXP Semiconductors (Co-Chair)
Yu Pu - Alibaba (Co-Chair)

Track G

Tutorial 1
Wednesday, April 7, 11:50 PM - 12:50 PM

Semiconductors for the next wave in Automotive

Clara Otero Perez
NXP Semiconductors

Tutorial 2
Thursday April 8, 12: 35 PM 1:35 PM

Large-Scale Quantum Computers:
The need for Cryo-CMOS

Dr. Fabio Sebastiano
Delft University of Technology, Delft, The Netherlands

Tutorial 3
Friday April 9, 9:00 AM - 10:00 AM

Putting AI on Diet:
TinyML and Efficient Deep Learning

Prof. Song Han, MIT EECS

Tutorial 4
Friday April 9, 10:00 AM - 11:00 AM

Security challenges and opportunities at the Intersection of Architecture and ML/AI
Nael Abu-Ghazaleh
University of California, Riverside

TECHNICAL SESSIONS

There are a total of 16 paper sessions held on Wednesday to Friday. Technical sessions are held in the format of four parallel virtual tracks **A, B, C, D**.

ISQED'21 PROGRAM AT A GLANCE

DATE	TIME				
WEDNESDAY 4/7/2021	9:00 AM - 9:20 AM	WELCOME AND INTRODUCTION			
		KEYNOTE SPEECH - PLENARY SESSION P1 TRACK G			
	9:20 AM - 9:55 AM	**CONFLUENCE OF AI/ML WITH EDA AND SOFTWARE ENGINEERING** ARUN VENKATACHAR - VICE PRESIDENT, ARTIFICIAL INTELLIGENCE AND CENTRAL ENGINEERING , SYNOPSYS TRACK G			
	9:55 AM - 10:00 AM	BREAK			
	10: AM - 11:20 AM	SESSION 1A **ADVANCED ANALOG DESIGN AND CONCEPTS** TRACK A	SESSION 1B **VERIFICATION AND FAULT ANALYSIS OF CIRCUITS** TRACK B	SESSION 1C **EMERGING DEVICES AND TECHNOLOGIES** TRACK C	SESSION 1D **APPLIED MACHINE LEARNING FOR HARDWARE CYBERSECURITY** TRACK D
	11:20 AM - 11:50 AM	BREAK			
	11:50 AM -12:55 PM	EMBEDDED TUTORIAL 1 **SEMICONDUCTORS FOR THE NEXT WAVE IN AUTOMOTIVE** CLARA OTERO PEREZ - NXP SEMICONDUCTORS TRACK G			
	12:55 PM - 2:25 PM	PANEL DISCUSSION **STATE OF AUTONOMOUS VEHICLE DEVELOPMENT: MOVING FORWARD WITH SAFE CARS** TRACK G			
	2:25 PM - 2:30 PM	BREAK			
	2:30 PM - 3:50 PM	SESSION 2A **LOW POWER COMPUTATION TECHNIQUES AND CONCEPTS** TRACK A	SESSION 2B **HARDWARE-SOFTWARE CO-DESIGN OF EMBEDDED AI FOR NEXT-GENERATION IOT SYSTEMS** TRACK B	SESSION 2C.1 **EFFICIENT AI COMPUTING** SESSION 2C.2 **EDA METHODOLOGIES FOR SECURE AND ERROR RESILIENT HARDWARE DESIGN** TRACK C	SESSION 2D **ANALOG, NANOTUBE, AND QUANTUM RELEVANCE OF MACHINE LEARNING** TRACK D
		END OF DAY 1			

ISQED'21 PROGRAM AT A GLANCE

DATE	TIME				
THURSDAY 4/8/2021	8:50 AM - 9:00 AM	WELCOME & INTRODUCTION			
		KEYNOTE SPEECH - PLENARY SESSION P2 TRACK G			
	9:00 AM -9:35 AM	**CARS DRIVING CHIPS OR CHIPS DRIVING CARS?** RAVI SUBRAMANIAN, PH.D., SENIOR VICE PRESIDENT - IC VERIFICATION, SIEMENS EDA TRACK G			
	9:35 AM -10:20 AM	SESSION PW1 POSTER AND WIP PAPERS TRACK A	SESSION PW2 POSTER AND WIP PAPERS TRACK B	SESSION PW3 POSTER AND WIP PAPERS TRACK C	SESSION PW4 POSTER AND WIP PAPERS TRACK D
	10:20 AM - 10:25 AM	BREAK			
	10:25 AM - 12:05 PM	SESSION 3A ROBUST AND EFFICIENT AI COMPUTING TRACK A	SESSION 3B EDA METHODOLOGIES FOR DESIGN PLANNING AND CHARACTERIZATION TRACK B	SESSION 3C REVERSE ENGINEERING AND HARDWARE OBFUSCATION TRACK C	SESSION 3D APPLICATION OF AI/ML IN HARDWARE SECURITY TRACK D
	112:05 PM -12:35 PM	BREAK			
	12:35 PM -1:35 PM	EMBEDDED TUTORIAL 2 **LARGE-SCALE QUANTUM COMPUTERS: THE NEED FOR CRYO-CMOS** FABIO SEBASTIANO - DELFT UNIVERSITY OF TECHNOLOGY, DELFT, THE NETHERLANDS TRACK G			
	1:35 PM -1:40 PM	BREAK			
	1:40 PM -3:20 PM	SESSION 4A DESIGN TECHNIQUES & METHODOLOGIES FOR AN ENERGY-EFFICIENT SYSTEM TRACK A	SESSION 4B CAD FOR SYSTEM ANALYSIS AND OPTIMIZATION TRACK B	SESSION 4C MEMORY AND ARCHITECTURE LEVEL SECURITY TRACK C	SESSION 4D.1 SOLVING SOC/CHIPLETS COMMUNICATION AND COMPUTATION CHALLENGES SESSION 4D.2 N-MEMORY AND QUANTUM COMPUTING TECHNOLOGIES SESSION 4D.3 RELIABILITY IN NEURAL NETWORKS TRACK D
	END OF DAY 2				

ISQED'21 PROGRAM AT A GLANCE

DATE	TIME		
FRIDAY 4/9/2021	*9:00 AM - 10:00 AM*	EMBEDDED TUTORIAL 3 **PUTTING AI ON DIET: TINYML AND EFFICIENT DEEP LEARNING** PROF. SONG HAN, MIT EECS **TRACK G**	
	10:00 AM - 11:00 AM	EMBEDDED TUTORIAL 4 **SECURITY CHALLENGES AND OPPORTUNITIES AT THE INTERSECTION OF ARCHITECTURE AND ML/AI** PROF. NAEL ABU-GHAZALEH , UNIVERSITY OF CALIFORNIA, RIVERSIDE **TRACK G**	
	11:00 AM - 11:10 AM	**BREAK**	
	11:10 AM - 12:30 PM	SESSION 5A IOT AND WEARABLE COMPUTING TRACK A	
	END OF DAY 3		

Wednesday April 7

9:20 AM - 9:55 AM

Track G

Confluence of AI/ML with EDA and Software Engineering

Arun Venkatachar

Vice President, Artificial Intelligence and Central Engineering , Synopsys

Investments into AI/ML to solve EDA problems with ever-increasing complexities of chip-design is starting to come to light. Recent product announcements like the DSO.ai from Synopsys revolutionizes chip design by massively scaling exploration of options in design workflows. Similarly, there are many applications in production solving different challenges in areas like verification, place & route, dfm etc., that have harnessed the power of AI/ML, Big-Data and Compute to provide a new set of tools and techniques for EDA to address both existing and new challenges. Not only do these technologies aid EDA, they are also helping us address challenges during software engineering development of these complex EDA products. By harnessing the data from code, tests, and bugs one can now improve product quality, improve productivity, and provide greater customer experience. In my talk I will be also going over such applications that are in production. With such potential, companies now need to build good data strategies to harness these benefits across their organizations. They will also need to invest in good data and AI/ML infrastructures to expedite building these solutions. It is now time to have data generate algorithms instead of the other way around! While these investments are starting to come to fruition, semiconductor design industry is still in the early stages and future promise is very alluring and exciting.

About Arun Venkatachar

Arun Venkatachar is Vice President of Artificial Intelligence & Central Engineering at Synopsys. He is responsible for leading Synopsys' Artificial Intelligence strategy and development, along with driving Synopsys core EDA engineering infrastructure, tooling and operations. He has over 20+ years of experience in building EDA products in the areas of compilers and debuggers and is currently focused on building AI/ML, Big-Data and Cloud-based solutions to solve complex problems for both internal and external customers. He has several publications and patents in the areas of distributed computing and simulation. He holds a Master's Degree in Computer Engineering.

ISQED Keynote 2P

Thursday April 8

9:00 AM - 9:35 AM

Track G

Cars Driving Chips or Chips Driving Cars?

Ravi Subramanian, Ph.D.

Senior Vice President - IC Verification, Siemens EDA

The automotive industry, once driven by mechanical design, styling and fuel economy – has transformed. The road ahead for cars is now all about software and electronics in the pursuit of autonomous driving and electrification. Future automotive platforms are being shaped by new requirements around sensing, safety, and security - spanning design, manufacturing, and in-road operation. These are driving revolutionary changes in the required imaging, radar, computing, networking, and software platform technologies. In this talk, we will explore the evolution of automobile platforms and the resulting implications on IC design, manufacture, and field operation for automotive IC suppliers in the coming decade.

About Ravi Subramanian

Ravi Subramanian is Senior Vice-President of IC Verification at Siemens EDA. He joined Siemens through the acquisition of Mentor Graphics where he held the role of Vice President and General Manager of the Analog/RF/Mixed-Signal Verification Business Unit. Ravi joined Mentor through the acquisition of Berkeley Design Automation (BDA), where he was President and CEO. Prior to BDA, Ravi was at Infineon Technologies, where he was the VP and GM of the 3G WCDMA Business Group. Ravi joined Infineon through the acquisition of Morphics Technology, a fabless semiconductor company where he was the founder and VP Engineering, and then CEO. Ravi began his career at AT&T Bell Laboratories, where he worked on radio transceivers for CDMA and GSM mobile communications and led the Radio Systems Research Department. While at AT&T, Ravi won the AT&T Leadership Award for his work on digital radio platforms. Ravi received his BSEE (with honors) from the California Institute of Technology (1987). He earned his PhD in EECS from the University of California at Berkeley (1991) where he was a recipient of the prestigious UC Regent's Fellowship. He is the lead author on 18 issued United States patents on digital, analog, and RF signal processing techniques in mobile communications. With over 20 years of experience spanning semiconductor, software, wireless, and electronic design, Ravi has directly been involved in the transformations electronics, software, and semiconductors have enabled across multiple industries. Ravi is a respected and proven business leader, technologist, and entrepreneur. He is passionate about customer success, the business of technology, building teams, and fueling innovation.

Panel Discussion

Wednesday April 7

12:55 PM –2:25 PM
Track G

State of Autonomous Vehicle Development: Moving Forward with Safe Cars

Panel Committee:
Shigeki Tomishima - Intel Corporation (Chair)
Siddha Ganju - Nvidia (Co-Chair)

Summary:
The automotive industry is going through a disruptive phase and one of the major factors causing this disruption is autonomous cars. The digitalization of the automotive industry is changing the traditional patterns of transport and mobility, and connected vehicles, self-driving vehicles, vehicles that are increasingly connected to the internet and equipped with electromechanical controls are defining some of today and most of the future automotive industry. Though there is strong demand from users, how realistic is the future of autonomous vehicles? Is the safety of autonomous cars an issue for drivers and will potential safety issues cause the autonomous vehicle development to crash? Is the mobility trend shifting towards ride sharing? What new challenges and opportunities do driverless cars bring to the microelectronic industry? What are the safety and security constraints? What are the implications of the inclusion of AI hardware and software? Join us to listen to our panelist's thoughts on the subject.

Panelists:
Nirmal R. Saxena - NVIDIA
Lee Harrison - Siemens EDA
James Herman - CMU/Roborace
Sweta Mehta - Tata Consultancy Services
Srijani Dey - DXC Technology

Modedrator:
Aditya Sharma - Microsoft

Embedded Tutorial 1

Wednesday April 7

11:50 AM -12:50 PM
Track G

Semiconductors for the next wave in Automotive

Clara Otero Pereza
NXP Semiconductors

Summary:
This tutorial will provide insights on the NXP vision on mobility of the future: NXP is advancing intelligent transport systems and electrification in order to shape a future in which zero emissions, zero road fatalities and maximum convenience will become reality. ADAS – Advanced Driver Assistance Systems – will come within everyone's reach and provide the safe and increasingly autonomous experiences that will reshape our relationship to transport. The technologies of the Automated Driving Domain will soon allow passengers to experience the ultimate in personalized and connected convenience as vehicles seamlessly Sense, Think, and Act on real-time road situations.

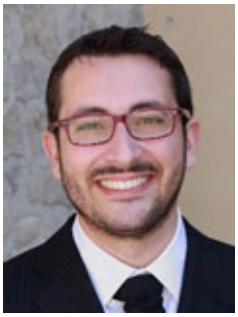
About Clara Otero Pereza
Clara Otero Pérez is Director Systems Innovations for Automotive at NXP Semiconductor in Eindhoven (NL). She is responsible for scouting new systems and applications where NXP's products would play a role and build proof of concepts and demonstrators for those new applications such as cooperative connected car, autonomous driving and UAV. After graduating in Physics by the University of Santiago de Compostela in Spain, she started to work for Philips Research in Eindhoven (NL) as a research scientist in the field of real-time systems and multimedia processors. In 2006 she moved to NXP and started working on automotive and secure connectivity related projects. In 2008 she became department manager driving innovation activities both internal as well as with partners in subsidy projects in the areas of IoT, connected car and cooperative mobility.

Thursday April 8

12:35 PM -13:35 PM

Track G

Large-Scale Quantum Computers: The need for Cryo-CMOS



Dr. Fabio Sebastiano

Delft University of Technology, Delft, The Netherlands

Summary:

Quantum computers hold the promise to change our everyday lives in this century in the same radical way as the classical computer did in the last century, by efficiently solving problems that are intractable today, such as large number factorization and simulation of quantum systems. Quantum computers operate by processing information stored in quantum bits (qubits), which must typically operate at cryogenic temperature. Today the qubits are mostly controlled by conventional electronics working at room temperature. This thermal gap can be readily bridged by a few wires since today's quantum computers employ only a few qubits.

However, practical quantum computers will require more than thousands of qubits, making this approach impractical. A solution is to build the qubit electrical interface using CMOS integrated circuits operate at cryogenic temperature (cryo-CMOS), hence very close to the qubits. This talk will give a brief introduction to quantum computers and their operations, followed by a description of their hardware implementation and their requirements in terms of electronic control and read-out, including the need for modeling the quantum/classical interface. Next, we will review the behavior of commercial CMOS devices and the available cryogenic device models required for circuit design. The demonstration of several state-of-the-art cryo-CMOS circuits and systems, both for qubit drive and readout, and their verification with qubits will be described, highlighting challenges and opportunities. Finally, we will outline the prospects towards qubit/electronics integration to enable the large-scale quantum computers required to address future world-changing computational problems.

About Fabio Sebastiano

Fabio Sebastiano holds degrees in Electrical Engineering from University of Pisa, Italy (BSc, 2003; MSc, 2005) from Sant'Anna school of Advanced Studies, Pisa, Italy (MSc, 2006) and from Delft University of Technology, The Netherlands (PhD, 2011). From 2006 to 2013, he was with NXP Semiconductors Research in Eindhoven, The Netherlands. In 2013, he joined Delft University of Technology, where he is currently an Associate Professor and the Research Lead for the Quantum Computing Division of QuTech. He has authored or co-authored one book, 11 patents, and over 70 technical publications. His main research interests are sensor read-outs, frequency references, cryogenic electronics, and quantum computing. Dr. Sebastiano was the co-recipient of the best student paper award at ISCAS in 2008, the best paper award at IWASI in 2017, and the best IP award at DATE in 2018. He is a senior member of IEEE, a TPC member for RFIC and IMS, and has served as Distinguished Lecturer of the IEEE Solid-State Circuit Society.

Friday April 9

9:00 AM - 10:00 AM

Track G

Putting AI on Diet: TinyML and Efficient Deep Learning

Prof. Song Han

MIT EECS

Summary:

Machine learning on tiny IoT devices based on microcontroller units (MCU) is appealing but challenging: the memory of microcontrollers is 2-3 orders of magnitude less even than mobile phones. We propose MCUNet, a framework that jointly designs the efficient neural architecture (TinyNAS) and the lightweight inference engine (TinyEngine), enabling ImageNet-scale inference on microcontrollers. TinyNAS adopts a two-stage neural architecture search approach that first optimizes the search space to fit the resource constraints, then specializes the network architecture in the optimized search space. TinyNAS can automatically handle diverse constraints (i.e. device, latency, energy, memory) under low search costs. TinyNAS is co-designed with TinyEngine, a memory-efficient inference library to expand the design space and fit a larger model. TinyEngine adapts the memory scheduling according to the overall network topology rather than layer-wise optimization, reducing the memory usage by 2.7x, and accelerating the inference by 1.7-3.3x compared to TF-Lite Micro and CMSIS-NN. MCUNet is the first to achieves >70% ImageNet top1 accuracy on an off-the-shelf commercial microcontroller, using 3.6x less SRAM and 6.6x less Flash compared to quantized MobileNetV2 and ResNet-18. On visual&audio wake words tasks, MCUNet achieves state-of-the-art accuracy and runs 2.4-3.4x faster than MobileNetV2 and ProxylessNAS-based solutions with 2.2-2.6x smaller peak SRAM. Our study suggests that the era of always-on tiny machine learning on IoT devices has arrived.

About Song Han

Song Han is an assistant professor in MIT EECS. His research focuses on efficient deep learning computing. He has proposed "deep compression" and "efficient inference engine" that first exploited model compression and weight sparsity in deep learning accelerators, which has been integrated into many commercial AI chips/frameworks. Recently he is interested in efficient and small NN design with AutoML and NAS. He is a recipient of NSF CAREER Award and MIT Technology Review Innovators Under 35. He earned a PhD in electrical engineering from Stanford University. synthesis algorithms.

Friday April 9

10:00 AM-11:00 AM
Track G

Security challenges and opportunities at the Intersection of Architecture and ML/AI

Prof. Nael Abu-Ghazaleh
University of California, Riverside

Summary:
Machine learning is an increasingly important computational workload as data-driven deep learning models are becoming increasingly important in a wide range of application spaces. Computer systems, from the architecture up, have been impacted by ML in two primary directions: (1) ML is an increasingly important computing workload, with new accelerators and systems targeted to support both training and inference at scale; and (2) ML supporting architecture decisions, with new machine learning based algorithms controlling systems to optimize their performance, reliability and robustness. In this talk, I will explore the intersection of security, ML and architecture, identifying both security challenges and opportunities. Machine learning systems are vulnerable to new attacks including adversarial attacks crafted to fool a classifier to the attacker's advantage, membership inference attacks attempting to compromise the privacy of the training data, and model extraction attacks seeking to recover the hyper parameters of a (secret) model. Architecture can be a target of these attacks when supporting ML, but also provides an opportunity to develop defenses against them, which I will illustrate with three examples from our recent work. First, I show how ML based hardware malware detectors can be attacked with adversarial perturbations to the Malware and how we can develop detectors that resist these attacks. Second, I will also show an example of a microarchitectural side channel attacks that can be used to extract the secret parameters of a neural network and potential defenses against it. Finally, I will also discuss how architecture can be used to make ML more robust against adversarial and membership inference attacks using the idea of approximate computing. I will conclude with describing some other potential open problems.

About Nael Abu-Ghazaleh
Nael Abu-Ghazaleh is a Professor with joint appointment in the CSE and ECE departments at the University of California, Riverside, and the director of the Computer Engineering program. His research interests include architecture support for security, high performance computing architectures, and networking and distributed systems. His group's research has lead to the discovery of a number of vulnerabilities in modern architectures and operating systems which have been reported to companies and impacted commercial products. He has published over 200 papers, several of which have been nominated or recognized with best paper awards. He is an ACM distinguished member, and IEEE distinguished visitor.

SESSION 1A

Wednesday April 7

Advanced Analog Design and Concepts

Chair: **Nihaar Mahatme**, NXP
Co-Chair: **Srinivasan Gopal**, Intel Corporation

10:00AM
1A.1
127 **PVT and Aging Degradation Invariant Automated Optimization Approach for CMOS Low-Power High-Performance VLSI Circuits**
Hema Sai Kalluru[1], Prasenjit Saha[2], Andleeb Zahra[2], Zia Abbas[3]
[1]IIIT Hyderabad, [2]International Institute of Information Technology Hyderabad, [3]International Institute of Information Technology (IIIT), Hyderabad

10:20AM
1A.2
133 **Design Space Extrapolation for Power Delivery Networks using a Transposed Convolutional Net**
Osama Waqar Bhatti and Madhavan Swaminathan
Georgia Institute of Technology

10:40AM
1A.3
137 **A Low Power Fully-Digital Multi-Level Voltage Monitor Operating in a Wide Voltage Range for Energy Harvesting IoT**
Shima Sedighiani[1], Kamlesh Singh[2], Roel Jordans[1], Pieter Harpe[1], Jose Pineda de Gyvez[1]
[1]Eindhoven university of technology, [2]Eindhoven University of Technology (TU/e)

11:00AM
1A.4
163 **A Resistorless NanoWatt CMOS Voltage Reference with High PSRR**
Naveed Naveed and Jeff Dix
University Of Arkansas

SESSION 1B

Wednesday April 7

Verification and Fault Analysis of Circuits

Chair: **Fei Su**, Intel Corporation
Co-Chair: **Sreejit Chakravarty**, Intel Corporation

10:00AM
1B.1
145 **Gate-Level Graph Representation Learning: A Step Towards the Improved Stuck-at Faults Analysis**
Aneesh Balakrishnan[1], Dan Alexandrescu[1], Maksim Jenihhin[2], Thomas Lange[1], Maximilien Glorieux[1]
[1]IROC Technologies, [2]Tallinn University of Technology

10:20AM
1B.2
174 **Efficient Reachability Analysis Based on Inductive Invariant Using X-value Based Flipflop Selection**
Ryogo Koike and Masahiro Fujita
University of Tokyo

10:40AM
1B.3
220 **Word-Level Multi-Fix Rectifiability of Finite Field Arithmetic Circuits**
Vikas Rao[1], Irina Ilioaea[2], Haden Ondricek[1], Priyank Kalla[1], Florian Enescu[3]
[1]University of Utah, [2]Louisiana State University Shreveport, [3]Georgia State University

11:00AM
1B.4
161 **Cell-Aware Diagnosis of Customer Returns Using Bayesian Inference**
Safa Mhamdi[1], Patrick Girard[2], Arnaud Virazel[3], Alberto Bosio[4], Aymen Ladhar[5]
[1]LIRMM - University of Montpellier, [2]LIRMM / CNRS, [3]LIRMM, [4]Lyon Institute of Nanotechnology, [5]STMicroelectronics

SESSION 1C

Wednesday April 7

Emerging Devices and Technologies

Chair: **Arijit Banerjee**, AMD
Co-Chair: **Rasit Topaloglu**, IBM

10:00AM
1C.1
196 **Achieving Wave Pipelining in Spin Wave Technology**
Abdulqader Mahmoud[1], Frederic Vanderveken[2], Christoph Adelmann[2], Florin Ciubotaru[2], Said Hamdioui[3], Sorin Cotofana[3]
[1]TU Delft, [2]IMEC, [3]Delft University of Technology

10:20AM
1C.2
205 **Architecture, Dataflow and Physical Design Implications of 3D-ICs for DNN-Accelerators**
Jan Moritz Joseph[1], Ananda Samajdar[2], Lingjun Zhu[2], Rainer Leupers[1], Sung Kyu Lim[3], Thilo Pionteck[4], Tushar Krishna[2]
[1]RWTH Aachen University, [2]Georgia Institute of Technology, [3]Georgia Tech, [4]Otto-von-Guericke-University Magdeburg

10:40AM
1C.3
226 **RobustONoC: Fault-Tolerant Optical Networks-on-Chip with Path Backup and Signal Reflection**
Yu-Kai Chuang[1], Yong Zhong[2], Yi-Hao Cheng[2], Bo-Yi Yu[2], Shao-Yun Fang[2], Bing Li[3], Ulf Schlichtmann[3]
[1]Technische Universität München, [2]National Taiwan University of Science and Technology, [3]Technical University of Munich

11:00AM

1C.4

230 **Decomposition-Based Watermarking of Quantum Circuits**

Vedika Saravanan[1] and Samah Saeed[2]

[1]City College of New York, City University of New York, [2]City College of New York

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SESSION 1D

Wednesday April 7

Applied Machine Learning for Hardware Cybersecurity

Chair: **Hossein Sayadi**, California State University Long Beach
Co-Chair: **Mehrdad Aliasgari**, California State University Long Beach

10:00AM

1D.1

271 **Machine Learning-Assisted Website Fingerprinting Attacks with Side-Channel Information: A Comprehensive Analysis and Characterization**

han wang[1], Hossein Sayadi[2], Avesta Sasan[3], Sai Manoj Pudukotai Dinakarrao[3], Setareh Rafatirad[1], Houman Homayoun[3]

[1]university of California, Davis, [2]California State University, Long Beach, [3]George Mason University

10:20AM

1D.2

272 **When Machine Learning Meets Hardware Cybersecurity: Delving into Accurate Zero-Day Malware Detection**

Zhangying He[1], Tahereh Miari[2], Hosein Mohammadi Makrani[3], Mehrdad Aliasgari[1], Houman Homayoun[4], Hossein Sayadi[1]

[1]California State University, Long Beach, [2]California State Polytechnic University, Pomona, [3]University of California, Davis, [4]University of California Davis

10:40AM
1D.3

273 **Leveraging Deep CNN and Transfer Learning for Side-Channel Attack**
Amit Garg and Nima Karimian
San Jose State University

11:00AM
1D.4

274 **Monotonic-HMDs: Exploiting Monotonic Features to Defend Against Evasive Malware**
Md Shohidul Islam, Behnam Omidi, Khaled N. Khasawneh
George Mason University

SESSION 2A

Wednesday April 7

Low Power Computation Techniques and Concepts

Chair: **Marshnil Dave**, Lion Semiconductor
Co-Chair: **Na Gong**, University of South Alabama

2:30PM
2A.1

215 **Flash ADC Utilizing Offset Voltage Variation With Order Statistics Based Comparator Selection**
Takehiro Kitamura, Mahfuzul Islam, Takashi Hisakado, Osami Wada
Kyoto University

2:50PM
2A.2

109 **Self-Learning Analog Comparator with Adaptive Sampling Rate Scheme for Energy Optimization in Continuous Input Monitoring Applications.**
G ANAND KUMAR and VEERAMANIKANDAN RAJU
TEXAS INSTRUMENTS INDIA PVT LTD

3:10PM

2A.3

136 **ACLA: An Approximate Carry-Lookahead Adder with Intelligent Carry Judgement and Correction**

Shobhit Belwal, Rajat Bhattacharjya, Kaustav Goswami, Dip Sankar Banerjee

Indian Institute of Information Technology Guwahati

SESSION 2B

Wednesday April 7

Hardware-Software Co-Design of Embedded AI for Next-Generation IoT Systems

Chair: **Mimi Xie**, University of Texas at San Antonio
Co-Chair: **Abhilash Goyal**, Velodyne

2:30PM

2B.1

249 **An End-to-end Multi-task Object Detection using Embedded GPU in Autonomous Driving**

Shanglin Zhou[1], Mimi Xie[2], Yufang Jin[2], Fei Miao[1], Caiwen Ding[1]

[1]University of Connecticut, [2]The University of Texas at San Antonio

2:50PM

2B.2

250 **SAC: A Novel Multi-hop Routing Policy in Hybrid Distributed IoT System based on Multi-agent Reinforcement Learning**

Wen Zhang[1], Tao Liu[2], Mimi Xie[3], Jun Zhang[4], Chen Pan[1]

[1]Texas A&M University-Corpus Christi, [2]Lawrence Technological University, [3]The University of Texas at San Antonio, [4]Harvard University

3:10PM

2B.3

Improving DNN Fault Tolerance using Weight Pruning and Differential Crossbar Mapping for ReRAM-based Edge AI

251 *Geng Yuan[1], Zhiheng Liao[2], Xiaolong Ma[1], Yuxuan Cai[1], Zhenglun Kong[1], Xuan Shen[1], Jingyan Fu[2], Zhengang Li[1], Chengming Zhang[3], Hongwu Peng[4], Ning Liu[1], Ao Ren[5], Jinhui Wang[6], Yanzhi Wang[1]*

[1]Northeastern University, [2]North Dakota State University, [3]Washington State University, [4]University of Connecticut, [5]Chongqing University, [6]University of South Alabama

3:30PM

2B.4

Accelerating Transformer-based Deep Learning Models on FPGAs using Column Balanced Block Pruning

257 *Hongwu Peng[1], Shaoyi Huang[1], Tong Geng[2], Ang Li[2], Weiwen Jiang[3], Hang Liu[4], Shusen Wang[4], Caiwen Ding[1]*

[1]University of Connecticut, [2]Pacific Northwest National Laboratory, [3]University of Notre Dame, [4]Stevens Institute of Technology

SESSION 2C.1

Wednesday April 7

Efficient AI Computing

Chair: **Hongyu An**, Michigan Tech University
Co-Chair: **Amey Kulkarni**, Nvidia

2:30PM
2C.1.1
263 **Regularization-Free Structural Pruning for GPU Inference Acceleration**
Chuliang Guo[1], Yanbing Yang[2], Li Zhang[1], Shaodi Wang[3], He Li[4], Keyu Long[2], Xunzhao Yin[1], Cheng Zhuo[1]
[1]Zhejiang University, [2]The Second Research Institute of Civil Aviation Administration of China, Chengdu, China, [3]WITIN Tech Co. Ltd., Beijing, China, [4]University of Cambridge, Cambridge, UK

2:50PM
2C.1.2
264 **Low-power Analog and Mixed-signal IC Design of Multiplexing Neural Encoder in Neuromorphic Computing**
Honghao Zheng[1], Nima Mohammadi[1], Kangjun Bai[2], Yang (Cindy) Yi[2]
[1]Virginia Tech, Blacksburg, VA, [2]Virginia Tech

3:10PM
2C.1.3
275 **Machine Learning for Evaluating the Impact of Manufacturing Process Variations in High-Speed Interconnects**
Cemil Geyik[1], Zhichao Zhang[1], Kemal Aygun[1], James Aberle[2]
[1]Intel Corporation, [2]Arizona State University

SESSION 2C.2

Wednesday April 7

EDA Methodologies for Secure and Error Resilient Hardware Design

Chair: **Srinivas Katkoori**, University of South Florida
Co-Chair: **Sheikh Ariful Islam**, University of Texas Rio Grande Valley

3:30PM
2C.2.1

259 **Secure High-Level Synthesis: Challenges and Solutions**
Nitin Pundir[1], Farimah Farahmandi[2], Mark Tehranipoor[2]
[1]Ansys, Inc (Intern), [2]University of Florida

3:50PM
2C.2.2

164 **An Error Resilient Design Platform for Aggressively Reducing Power, Area and Routing Congestion**
Tung-Liang Lin and Sao-Jie Chen
Graduate Institute of Electronics Engineering, National Taiwan University

SESSION 2D

Wednesday April 7

Hardware Security in Systems and Quantum Computing

Chair: **Anupam Chattopadhyay**, Nanyang Technological University
Co-Chair: **TBD**, TBD

2:30PM
2D.1
Deep Learning assisted Cross-Family Profiled Side-Channel Attacks using Transfer
245 **Learning**
Dhruv Thapar[1], Manaar Alam[1], Debdeep Mukhopadhyay[2]
[1]Indian Institute of Technology Kharagpur, [2]Department of Computer Science and Engineering, Indian Institute of Technology Kharagpur

2:50PM
2D.2
246 **Impact of Noise on the Resilience and the Security of Quantum Computing**
Abdullah Ash- Saki, Mahabubul Alam, Swaroop Ghosh
Pennsylvania State University

3:10PM
2D.3
247 **Sandbox Detection Using Hardware Side Channels**
Yehonatan Lusky and Avi Mendelson
Technion

3:30PM
2D.4
248 **Trusted Electronic Systems with Untrusted COTS**
Shuo Yang, Prabuddha Chakraborty, PATANJALI SLPSK, SWARUP BHUNIA
University of Florida

SESSION PW1

Thursday April 8

Poster and WIP Session 1

Chair: **Ali Iranmanesh**, Silicon Valley Polytechnic Institute

9:35AM
PW1.1
132 **Toward Intelligence in Communication Networks: A Deep Learning Identification Strategy for Radio Frequency Fingerprints**
Kangjun Bai[1], Clare Thiem[2], Nathan McDonald[2], Lisa Loomis[2], Yang Yi[1]
[1]Virginia Tech, [2]Air Force Research Laboratory

9:40AM
PW1.2
201 **Three-dimensional Memristive Deep Neural Network with Programmable Attention Mechanism**
Hongyu An[1], Kangjun Bai[2], Yang Yi[2]
[1]Michigan Technological University, [2]Virginia Tech

9:45AM
PW1.3
170 **Detection Limit for Intermediate Faults in Memristor Circuits**
Rasika Joshi and John Acken
Portland State University

9:50AM
PW1.4
177 **Enabling ECC and Repair Features in an eFuse Box for Memory Repair Applications**
Miguel F Costa[1] and Srikanth Beerla[2]
[1]Intel Corporation, [2]Intel Technology Pvt Ltd

9:55AM
PW1.5

146 **A crosstalk modelling method between a power supply and a nearby signal in high-density interconnection PCBs**
Faten Sahel[1], Pascal Guilbault[1], Farouk Vallette[2], Sylvain Feruglio[2]
[1]ATOS, [2]LIP6

10:00AM
PW1.6

168 **Formal Verification Aware Redundant Sequential Logic Optimization to Improve Design Utilization**
Rushabh Shah and Krishna Agrawal
Digital Design Engineer, Intel Technology India Pvt. Ltd

10:05AM
PW1.7

173 **A Wafer-scale Manufacturing Pathway for Fine-grained Vertical 3D-IC Technology**
Sachin Bhat, Sounak (Shaun) Ghosh, Sourabh Kulkarni, Mingyu Li, Csaba Andras Moritz
UMass Amherst

SESSION PW2

Thursday April 8

Poster and WIP Session 2

Chair: **Amey Kulkarni**, Nvidia

9:35AM
PW2.1

240 **Novel Memristor-based Nonvolatile D Latch and Flip-flop Designs**
Zhenxing Chang[1], Aijiao Cui[1], Gang Qu[2], Ziming Wang[1]
[1]Harbin Institute of Technology Shenzhen Graduate School, [2]Univ. of Maryland, College Park

9:40AM

PW2.2

Variation Aware Timing Model of CMOS Inverter for an Efficient ECSM Characterization

242 *Lomash Chandra Acharya[1], Arvind Kumar Sharma[2], Venkatraman Ramakrishnan[3], ajoy mandal[3], Sudeb Dasgupta[4], Anand Bulusu[5]*

[1]Indian Institute of technology,roorkee, [2]University of Minnesota, [3]Texas Instruments, [4]Associate Professor, IIT Roorkee, [5]Indian Institute of Technology Roorkee

9:45AM

PW2.3

232 **Reconfiguring the Mux-Based Arbiter PUF using FeFETs**

Srinivasa Varadan Ramanujam[1] and Wayne Burleson[2]

[1]University of MAssachusetts- Amherst, [2]UMass- Amherst

9:50AM

PW2.4

156 **A Lightweight Delay-based Authentication Scheme for DMA Attack Mitigation**

Yutian Gui, Ali Shuja Siddiqui, Geraldine Shirley Nicholas, Marcus Hughes, Fareena Saqib

University of North Carolina at Charlotte

9:55AM

PW2.5

106 **3D IC Packaging Utilizing a Metal structure for Heat Reduction, Noise Shielding, and High Interconnect Density**

Nahid Mirzaie and Ronald Rohrer

Southern Methodist University

10:00AM

PW2.6

147 **Chip Package Co-design and Physical Verification for Heterogeneous Integration.**

Rajsaktish Sankaranarayanan, Archanna Srinivasan, Arch Zaliznyak, Sreelekha Mittai

Intel Corporation

10:05AM

197 **PW2.7**

Analysis and Design of a 5G Multi-Mode Power Amplifier using 130 nm CMOS

technology
Marwa Mansour[1], Abdelhalim Zekry[2], Mohammed K. Ali[3], Heba Shawkey[1]
[1]Electronics Research Institute, [2]Ain shams University, [3]Fauyoum University

10:10AM
PW2.8
116 **A Comprehensive Multi-Voltage Design Platform for System-Level Validation of Standard Cell Library**
Akshay Kamath, Bharath Kumar, Sunil Aggarwal, Subramanian Parameswaran, Mitesh Goyal, Parag Lonkar, Somasunder Sreenath
Samsung Semiconductor India R&D

SESSION PW3

Thursday April 8

Poster and WIP Session 3

Chair: **Sara Tehranipoor**, Santa Clara University

9:35AM
PW3.1
149 **ChipAdvisor: A Machine Learning Approach for Mapping Applications to Heterogeneous Systems**
Hiwot Tadese Kassa, Tarunesh Verma, Todd Austin, Valeria Bertacco
University of Michigan

9:40AM
PW3.2
165 **Integration of Minimum Energy Point Tracking and Soft Real-Time Scheduling for Edge Computing**
Takumi Komori[1], Yutaka Masuda[1], Jun Shiomi[2], Tohru Ishihara[1]
[1]Nagoya University, [2]Kyoto University

9:45AM

PW3.3

140 **Global multi-voltage interface unit for diverse digital logic**

Manisha Girish[1], Karthik Suman[2], Sandeep Motebennur[1], Krishna Prasanna[1], Prashanth N[1]

[1]Intel Corporation, [2]Intel Corp

9:50AM

PW3.4

141 **Achieving Zero ADC Production Test Time with Self-calibration and BIST**

Maher Sarraj, Haydar Bilhan, Wahed Mohammed

Texas Instruments, Inc.

9:55AM

PW3.5

143 **LEC Vulnerability On Constant Propagation**

Sandeep Kumar Srivastav[1], Ming Yi Lim[2], Babu Trp[2], Jeevan K Y[2]

[1]Intel India, [2]Intel

10:00AM

PW3.6

166 **FPGA Accelerated Parameterized Cache Simulator**

Shivani Shah[1], Sahithi Meenakshi Vutakuru[1], Nanditha Rao[2]

[1]International Institute of Information Technology Bangalore, [2]IIIT Bangalore

10:05AM

PW3.7

175 **Back-Bias Modulated UTBB SOI for System-on-Chip I/O Cells**

Ming Yu Chang[1], Po Yu Chao[2], Meng Hsueh Chiang[2]

[1]+886 919181317, [2]National Cheng Kung University

SESSION PW4

Thursday April 8

Poster and WIP Session 4

Chair: **Abhilash Goyal**, Velodyne

9:35AM
PW4.1
190 **SALAH: Simulation-Assisted LAyout Hierarchy Construction**
Sherif Hany, Emad Hegazi, Hani Ragai
Ain Shams university

9:40AM
PW4.2
209 **A New Foe in GPUs: Power Side-Channel Attacks on Neural Network**
Hyeran Jeon[1], Nima Karimian[2], Tamara Lehman[3]
[1]University of California Merced, [2]San Jose State University, [3]University of Colorado Boulder

9:45AM
PW4.3
138 **Performance investigation of a Si/Ge Heterojunction Asymmetric Double Gate DLTFET considering Temperature and ITC variations**
Suruchi Sharma[1], Rikmantra Basu[2], Baljit Kaur[2]
[1]NIT, [2]NIT Delhi

9:50AM
PW4.4
192 **Large-Scale Quantum System Design on Nb-based Superconducting Silicon Interconnect Fabric**
Yu-Tao Yang and Subramanian Iyer
UCLA

9:55AM
PW4.5
199 **On Synthesizing Memristor-Based Logic Circuits in Area-Constrained Crossbar Arrays**

Hsin-Tsung Lee[1], Chia-Chun Lin[1], Yung-Chih Chen[2], Chun-Yao Wang[3]
[1]National Tsing Hua University, [2]Yuan Ze University, [3]Dept. CS, National Tsing Hua University

10:00AM
PW4.6
211 **Compressing CNNs by Exponent Sharing in Weights using IEEE Single Precision Format**
Prachi Kashikar and Sharad Sinha
Indian Institute of Technology Goa

10:05AM
PW4.7
Infineon Platform for SoC IO Ring and Package Design
244 *Sathvik Tarikere Sathyanarayana[1], Anna-Antonia Berger[2], Mahesh Simpy Kumar[3], Akbay Erkan[2], Ramkrishna Paira[3]*
[1]Infineon Technologies Pvt Ltd, [2]Infineon Technologies AG Neubiberg, Germany, [3]Infineon Technologies India Pvt. Ltd, Bangalore, India

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SESSION 3A

Thursday April 8

Robust and Efficient AI Computing

Chair: **Cindy Yi**, Virginia Tech
Co-Chair: **Amey Kulkarni**, Nvidia

10:25AM
3A.1
Diverse Knowledge Distillation (DKD): A Solution for Improving The Robustness of
114 **Ensemble Models Against Adversarial Attacks**
Ali Mirzaeian[1], Jana Kosecka[1], Homan Homayoun[2], Tinoosh Mohsenin[3], Avesta Sasan[1]
[1]George Mason University, [2]University of California, Davis, [3]University of Maryland, Baltimore County

10:45AM

3A.2

121 **Conditional Classification: A Solution for Computational Energy Reduction**

Ali Mirzaeian[1], Sai Manoj Pudukotai Dinakarrao[1], Ashkan Vakil[1], Homan Homayoun[2], Avesta Sasan[1]

[1]George Mason University, [2]University of California, Davis

11:05AM

3A.3

A Lightweight Error-Resiliency Mechanism for Deep Neural Networks

135 *Brunno F. Goldstein[1], Victor C. Ferreira[1], Sudarshan Srinivasan[2], Dipankar Das[2], Alexandre S. Nery[3], Sandip Kundu[4], Felipe M. G. França[1]*

[1]Federal University of Rio de Janeiro, [2]Intel Labs, [3]University of Brasilia, [4]University of Massachusetts Amherst

11:25AM

3A.4

158 **A Three-dimensional (3D) Memristive Spiking Neural Network (M-SNN) System**

Hongyu An[1], Mohammad Shah Al-Mamun[2], Marius Orlowski[2], Yang Yi[2]

[1]Michigan Technological University, [2]Virginia Tech

11:45AM

3A.5

207 **Exploring Fault-Energy Trade-offs in Approximate DNN Hardware Accelerators**

Ayesha Siddique[1], Kanad Basu[2], Khaza Anuarul Hoque[1]

[1]University of Missouri, [2]University of Texas at Dallas

SESSION 3B

Thursday April 8

EDA Methodologies for Design Planning and Characterization

Chair: **Srinivas Katkoori**, University of South Florida
Co-Chair: **R. Chidambaranathan**, Synopsys, Inc.

10:25AM
3B.1
150 **Fast and Accurate Library Generation Leveraging Deep Learning for OCV Modelling**
Eunice Naswali[1], Namhoon Kim[1], Pravin Chandran[2]
[1]Intel Corporation, [2]Intel Technologies India Pvt Ltd

10:45AM
3B.2
216 **On the Correlation Between Resource Minimization and Interconnect-related Complexities in High-Level Synthesis**
Shantanu Dutt[1], Xiuyan Zhang[1], Ouwen Shi[2]
[1]University of Illinois at Chicago, [2]Cadence Design Systems

11:05AM
3B.3
180 **Six-track Standard Cell Libraries with Fin Depopulation, Contact over Active Gate, and Narrower Diffusion Break in 7nm Technology**
Tzu-Hsuan Wang, Chih-Chun Hsu, Li Kao, Bing-Yu Li, Tung-Chun Wu, Tsao-Hsuan Peng, Rung-Bin Lin
Yuan Ze University

11:25AM
3B.4
125 **Fast Thermal Goodness Evaluation of a 3D-IC Floorplan**
Satya K. Vendra and Malgorzata Chrzanowska-Jeske
Portland State University

11:45AM
3B.5

235 **Mining Message Flows from System-on-Chip Execution Traces**
Md Rubel Ahmed[1], Hao Zheng[1], Parijat Mukherjee[2], Mahesh C. Ketkar[2], Jin Yang[2]
[1]University of South Florida, [2]Intel

SESSION 3C

Thursday April 8

Reverse Engineering and Hardware Obfuscation

Chair: **Ioannis Savidis**, Drexel University
Co-Chair: **Nima Karimian**, SJSU

10:25AM
3C.1

172 **SOMA: Security Evaluation of Obfuscation Methods via Attack Sequencing**
Abdulrahman Alaql[1], Xinmu Wang[2], Md Moshiur Rahman[1], SWARUP BHUNIA[1]
[1]University of Florida, [2]Northwestern Polytechnical University

10:45AM
3C.2

183 **ChaoLock: Yet Another SAT-hard Logic Locking using Chaos Computing**
Hadi Mardani Kamali[1], Kimia Zamiri Azar[1], Houman Homayoun[2], Avesta Sasan[1]
[1]George Mason University, [2]University of California Davis

11:05AM
3C.3

154 **Profiled Power Analysis Attacks by Efficient Architectural Extension of CNN Implementation**
Soroor Ghandali[1], Samaneh Ghandali[2], Sara Tehranipoor[1]
[1]Santa Clara University, [2]Google

11:25AM

3C.4

Exploring the RISC-V Vector Extension for the Classic McEliece Post-Quantum Cryptosystem

203 *Sabine Pircher[1], Johannes Geier[2], Alexander Zeh[3], Daniel Mueller-Gritschneder[2]*

[1]HENSOLDT Cyber GmbH, Research and Development; Technical University of Munich, Department of Electrical and Computer Engineering, Professorship of Coding for Communications and Data Storage, [2]Technical University of Munich, Department of Electrical and Computer Engineering, Chair of Electronic Design Automation, [3]HESOLDT Cyber GmbH, Research and Development

11:45AM

3C.5

236 **Defending Misspeculation-based Cache Probe Attacks Using Variable Record Table**

Love Sah[1], Sheikh Ariful Islam[2], Srinivas Katkoori[1]

[1]University of South Florida, [2]University of Texas Rio Grande Valley

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SESSION 3D

Thursday April 8

Application of AI/ML in Hardware Security

Chair: **Rajat Subhra Chakraborty**, Indian Institute of Technology Kharagpur
Co-Chair: **Pranesh Santikellur**, Indian Institute of Technology Kharagpur

10:25AM

3D.1

252 **Application of Machine Learning in Hardware Trojan Detection**

Shamik Kundu[1], Xingyu Meng[1], Kanad Basu[2]

[1]The University of Texas at Dallas, [2]University of Texas at Dallas

10:45AM

3D.2

253 **TRGP: A Low-Cost Re-Configurable TRNG-PUF Architecture for IoT**

Vikash Kumar Rai[1], Somanath Tripathy[2], Jimson Mathew[3]

[1]IIT Patna, [2]Indian Institute of Technology, Patna, [3]University of Bristol

11:05AM

3D.3

254 **Chaogate Parameter Optimization using Bayesian Optimization and Genetic Algorithm**

Rabin Yu Acharya[1], Noeloikeau F. Charlot[2], Md Mahbub Alam[3], Fatemeh Ganji[4], Daniel Gauthier[2], Domenic Forte[1]

[1]University of Florida, [2]Ohio State University, [3]Intel, [4]Worcester Polytechnic Institute

11:25AM

3D.4

255 **Hardware Trojan Detection Method for Inspecting Integrated Circuits Based on Machine Learning**

Yuze Wang[1], Peng Liu[1], Xiaoxia Han[1], Yingtao Jiang[2]

[1]Zhejiang University, [2]University of Nevada Las Vegas

11:45AM

3D.5

256 **Towards automatic and portable data loading template attacks on microcontrollers**

Unai Rioja[1], Lejla Batina[2], Jose Luis Flores[3], Igor Armendariz[3]

[1]Radboud University, [2]Radboud University Nijmegen, [3]Ikerlan Technological Research Centre

SESSION 4A

Thursday April 8

Design Techniques & Methodologies for an Energy-Efficient System

Chair: **Harsh Patel**, AMD
Co-Chair: **Georgios Keramidas**, Think Silicon

1:40PM
4A.1
MACcelerator: Approximate Arithmetic Unit for Computational Acceleration
144 *Alice Sokolova[1], Mohsen Imani[2], Andrew Huang[1], Ricardo Garcia[1], Justin Morris[3], Tajana Rosing[4], Baris Aksanli[5]*
[1]University of California San Diego, [2]University of California Irvine, [3]University of California, San Diego, [4]UCSD, [5]San Diego State University

2:00PM
4A.2
Towards Row Sensitive DRAM Refresh through Retention Awareness
181 *Tanmay Goel[1], Divyansh Maura[2], Kaustav Goswami[3], Shirshendu Das[4], Dip Sankar Banerjee[3]*
[1]*Indian Institute Of Information Technology*, *Guwahati*, [2]IIIT-G, [3]Indian Institute of Information Technology Guwahati, [4]Indian Institute of Technology Ropar

2:20PM
4A.3
HardCompress: A Novel Hardware-based Low-power Compression Scheme for DNN
208 **Accelerators**
Ayush Arunachalam[1], Shamik Kundu[1], ARNAB RAHA[2], Suvadeep Banerjee[3], Suriya Natarajan[2], Kanad Basu[1]
[1]University of Texas at Dallas, [2]Intel Corporation, [3]Intel Labs, Intel

2:40PM
4A.4
Brightening the Optical Flow through Posit Arithmetic
214 *Vinay Saxena[1], Ankitha Reddy[1], Jonathan Neudorfer[2], John Gustafson[3], Sangeeth S. Nambiar[4], Rainer Leupers[5], Farhad Merchant[6]*
[1]Corporate Research, Robert Bosch, Bangalore, [2]Robert Bosch GmbH, [3]National University of Singapore, [4]Robert Bosch, [5]RWTH Aachen University, [6]Institute for Communication Technologies and Embedded Systems, RWTH Aachen University

3:00PM
4A.5
DAMUS: Dynamic Allocation based on Write Frequency in MUlti-Retention STT-RAM based Last Level Caches
239 *Mayank Baranwal[1], Udbhav Chugh[1], Shivang Dalal[1], Sukarn Agarwal[2], Hemangee Kapoor[1]*
[1]Indian Institute of Technology Guwahati, [2]Indian Institute of Technology (BHU) Varanasi

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SESSION 4B

Thursday April 8

CAD for System Analysis and Optimization

Chair: **Srini Krishnamoorthy**, Intel, Bangalore
Co-Chair: **Murthy Palla**, Synopsys Inc.

1:40PM
4B.1
A Novel NBTI-Aware Chip Remaining Lifetime Prediction Framework Using Machine Learning
185 *Yu-Guang Chen[1], Ing-Chao Lin[2], Yong-Che Wei[3]*
[1]National Central University, [2]National Cheng Kung University, [3]Yuan Ze University

2:00PM
4B.2

210 **Minimally Allocating Always-on State Retention Storage for Supporting Power Gating Circuits**
Soomin Kim and Taewhan Kim
Seoul National University

2:20PM
4B.3

160 **Automatic Generation of Translators for Packet-Based and Emerging Protocols**
Brian Crafton[1], Arijit Raychowdhury[1], Sung Kyu Lim[2]
[1]Georgia Institute of Technology, [2]Georgia Tech

2:40PM
4B.4

258 **SoC Trust Validation Using Assertion-Based Security Monitors**
Khitam Alatoun[1], Bharath Shankaranarayanan[1], Shanmukha Murali Achyutha[2], Ranga Vemuri[2]
[1]University of Cincinnati, Cincinnati, Ohio, [2]University Of Cincinnati

3:00PM
4B.5

227 **Analysis of Attack Surfaces and Practical Attack Examples in Open Source FPGA CAD Tools**
Sandeep Sunkavilli, Zhiming Zhang, Qiaoyan Yu
University of New Hampshire

SESSION 4C

Thursday April 8

Memory and Architecture Level Security

Chair: **Fareena Saqib**, University of North Carolina at Charlotte
Co-Chair: **Nima Karimian**, SJSU

1:40PM

4C.1

202 **True Random Number Generation using Latency Variations of Commercial MRAM Chips**

Farah Ferdaus[1], Bashir Mohammad Sabquat Bahar Talukder[1], Mehdi Sadi[2], Md Tauhidur Rahman[1]

[1]Florida International University, [2]Auburn University

2:00PM

4C.2

148 **CARE: Lightweight Attack Resilient Secure Boot Architecture with Onboard Recovery for RISC-V based SOC**

Avani Dave[1], Nilanjan Banerjee[2], Chintan Patel[3]

[1]University of Maryland Baltimore County, [2]Assistant Professor, UMBC, [3]UMBC

2:20PM

4C.3

238 **SeNonDiv: Securing Non-Volatile Memory using Hybrid Memory and Critical Data Diversion**

Arijit Nath[1], Manik B Bhosle[2], Hemangee Kapoor[3]

[1]IIT Guwahati, India, [2]IIT Guwahati, [3]Indian Institute of Technology Guwahati

2:40PM

4C.4

142 **Reliable Strong PUF Enrollment and Operation with Temperature and Voltage Optimization**

Kleber Stangherlin and Manoj Sachdev

University of Waterloo

3:00PM

4C.5

123 **Flush-Reload Attack and its Mitigation on an FPGA Based Compressed Cache Design**

Prashant Mata[1] and Nanditha Rao[2]

[1]International Institute of Information Technology Bangalore, [2]IIIT Bangalore

SESSION 4D.1

Thursday April 8

Solving SoC/Chiplets Communication and Computation Challenges

Chair: **Tobias Gemmeke**, Aachen University
Co-Chair: **Rakesh Mahto**, Computer Eng. Program

1:40PM
4D.1.1

260 **A Reconfigurable Asynchronous SERDES for Heterogenous Chiplet Interconnects**
Jainaveen Sundaram Priya[1], Srinivasan Gopal[1], Erika Ramirez Lozano[1], Thomas P Thomas[1], Edward Burton[1], Tanay Karnik[2]
[1]Intel Corporation, [2]Intel

2:00PM
4D.1.2

261 **Trends and Opportunities for SRAM Based In-Memory and Near-Memory Computation**
Srivatsa Srinivasa[1], Jainaveen Sundaram Priya[2], Dileep Kurian[3], Srinivasan Gopal[2], Anuradha Srinivasan[1], Vijaykrishnan Narayanan[4], Tanay Karnik[1]
[1]Intel, [2]Intel Corporation, [3]Intel technologies, [4]Penn State University

SESSION 4D.2

Thursday April 8

In-Memory and Quantum Computing Technologies

Chair: **Rasit Topaloglu**, IBM
Co-Chair: **Vita Pi-Ho Hu**, National Taiwan University

2:20PM
4D.2.1
269 **Cross-layer Optimization Strategy for Energy-efficient and Variation-aware In-memory Computing**
Tuo-Hung Hou
National Chiao Tung University

2:40PM
4D.2.2
270 **Challenges for Building a Silicon-based Quantum Computer**
Jonathan Baugh
University of Waterloo

SESSION 4D.3

Thursday April 8

Reliability in Neural Networks

Chair: **Rasit Topaloglu**, IBM
Co-Chair: **Vita Pi-Ho Hu**, National Taiwan University

3:00PM

4D.3.1

Runtime Long-Term Reliability Management Using Stochastic Computing in Deep Neural Networks

262

Yibo Liu[1], Shuyuan Yu[2], Shaoyi Peng[2], Sheldon Tan[3]
[1]University of Califronia, Riverside, [2]University of California, Riverside, [3]University of California at Riverside

SESSION 5A

Friday April 9

IoT and Wearable Computing

Chair: **Prabha Sundaravadivel**, University of Texas at Tyler
Co-Chair: **TBD**, TBD

11:10AM
5A.1
265 **Towards Internet-of-Things for Wearable Neurotechnology**
Salma Elmalaki[1], Berken Utku Demirel[1], Mojtaba Taherisadr[1], Sara Stern-Nezer[1], Jack J. Lin[1], Mohammad Al Faruque[2]
[1]University of California, Irvine, California, [2]University of California Irvine

11:30AM
5A.2
266 **Real-Time CNN Based ST Depression Episode Detection Using Single ECG-Lead**
LAKSHMAN TAMIL[1], Erhan Tiryaki[1], Akshay Sonawane[2]
[1]University of Texas at Dallas, [2]The University of Texas at Dallas

11:50AM
5A.3
267 **An Interactive IoT-based framework for Resource Management in Assisted living during pandemic**
Parker Wilmoth and Prabha Sundaravadivel
University of Texas at Tyler

12:10PM
5A.4
268 **SolicitudeSavvy: An IoT-based edge intelligent framework for monitoring anxiety in real-time**
Prabha Sundaravadivel, Parker Wilmoth, Ashton Fitzgerald
University of Texas at Tyler

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