2001 IEEE
2nd International Symposium on
QUALITY ELECTRONIC DESIGN
MARCH 26, 27, 28
DoubleTree Hotel
San Jose, CA
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On behalf of the ISQED 2001 conference and technical committees, we would like to cordially welcome you to the 2nd International Symposium on Quality Electronic Design, ISQED 2001. All the technical presentations, plenary sessions, panel discussions, tutorials and related events will take place on March 26-28 at the San Jose Double Tree Hotel. The hotel is located in the heart of Silicon Valley, near the San Jose International Airport, and is a very convenient location for all conference participants, whether local, US or international attendees.

The technical program addresses the variety of issues related to electronic design, and System-on-a-chip (SoC) design with intellectual property (IP), employing deep sub-micron (DSM) technologies. It is clear that DSM level integration, which will approach 1 billion transistors on a chip before the decade is out, is causing a paradigm shift to SoC/IP based design methodologies. However, DSM by itself is a major cause of failure due to a plethora of physical and electrical problems. As a result, there are enormous challenges to overcome to be able to design high-quality SoC’s in a given market window. The sessions in this conference address many of the issues that must be resolved in order for SoC design to become a reality. The technical sessions span the disciplines of high-level design methodologies, synthesis and verification, embedded memories and cores, interconnect issues, device modeling, power management, manufacturing and test. This conference provides an opportunity to understand the key issues faced by the industry in the next few years and possible solutions to these challenges.

The technical program for ISQED 2001 has been assembled by the technical program committee, which includes international experts from industry and academia. The technical committee is made up of ten subcommittees with a total of fifty active members. The technical committee members have selected papers for presentation from many excellent submissions. This year, a total of 38 papers were accepted for oral presentation from 93 papers submitted to ISQED 2001. An additional 16 papers were accepted for poster presentation. The technical program also includes 13 invited papers from leading experts in the field. ISQED will award three best papers during the luncheon held on Tuesday. In addition, the best PhD student paper will be also awarded during the same session.

The conference starts on Monday, March 26 with tutorial sessions organized by Frank Lee and David Overhauser. This year, due to popular demand, we have expanded the popular tutorial sessions to four tracks, with a total of twelve sessions. The tutorial session covers a variety of critical and timely topics such as Embedded Test Strategies for SoC, Design and Test of Low Voltage CMOS Circuits, Redundancy Requirements for Embedded Memories, Design Metrics for achieving Design Quality, Fundamental Methods to Enable SoC Design and Reuse, Deep Sub-micron State-of-the-Art ESD design, Application of Formal Verification to Design Creation and Implementation, Verification and Validation of Complex Digital Systems, Physical Verification of DSM designs, Re-Connecting MOS Modeling and Circuit Design, Interconnect Modeling for Timing, Signal Integrity and Reliability, as well as On-Chip inductance extraction and modeling.

One attractive feature of the first ISQED was the two popular plenary sessions. This year Kris Verma, and Carlo Guardiani have organized yet another outstanding plenary session of world-renowned leaders, from the industry and academia. The first plenary session will be held on Tuesday morning and features keynote speeches by Hajime Sasaki (Chairman of the board, NEC), Joe Costello (CEO, think3), Raul Camposano (CTO/GM, Synopsys), Edward Ross (President, TSMC, USA). The second plenary session will be held on Wednesday morning. The list of keynote speakers for this session includes Wojciech Maly (Professor, Carnegie Mellon University), Vinod Agrawal (CEO, Logic Vision), Aki Fujimura (COO and President, Simplex Solutions), and Philippe Magarshack (Vice President, Design Automation, ST Microelectronics).

In the first keynote speech, entitled “Future Platform for Mobile Communication,” Hajime Sasaki will explore three driving forces in the IT revolution that are actualizing an Information Society. The next keynote by Joe Costello will focus on the relationship between quality and profitability. Next, Raul Camposano, will address various formal techniques for design verification, and explores the “Expanding Use of Formal Techniques in Electronic Design.” Edward Ross will then discuss emerging trends in the EDA, IP, library and design communities, wherein deep collaboration with foundries is producing a variety of Internet-based solutions that are revolutionizing IC design methodologies. The title of his speech is “IC Design Methodology in the Foundry Era: Introducing ‘Heads-Up’ Design.” The second plenary session on Wednesday will start with a plenary speech by Wojciech Maly entitled “Quality of Design from an IC M Manufacturing Perspective.” Following this, Vinod Agrawal will describe how “Embedded Test Leads to Embedded Quality.” He will further expand on how embedded test is becoming a standard choice for IC and system developers.
In summary, we have put together an excellent program for practicing engineers and managers, to learn the latest on quality electronic design so that functional integrated circuits, with acceptable yield and reliability, can be manufactured within the frame work of the desired cycle time. This conference provides a forum for you to learn and share and exchange insight and knowledge with your peers. See you in March 2001.

Sincerely,

Ali Iranmanesh
ISQED Founder and General Chair

Tak Young
ISQED Program Chair

Res Saleh
ISQED Technical Program Chair

If you have ever wondered why a group of talented, highly motivated, hard-working software engineers consistently produce low-quality software after the deadline, you will find an answer in the next speech by Aki Fujimura entitled “Quality on Time.” Mr. Magarshack will deliver the final plenary speech entitled “Quality of SoC designs through quality of the design flow: Status and Needs.” This is a critical issue gaining importance with the ever-increasing complexity of systems that can be built on the same chip: current process capabilities are exceeding 100 million devices.

The ISQED’2001 program includes two evening panel sections on Monday and Tuesday evenings, and one embedded panel on Wednesday afternoon. Gabriele Eckert, Nader Vasseghi, Bill Alexander, and Rick Merrit have organized these panel sessions. The first evening panel is organized by Rick Merrit, and moderated by Richard Goering and will be held on the evening of Monday. This panel is titled “The 50-Million Transistor Chip: The Quality Challenge for 2001.” The second evening panel discussion on Tuesday is “0.13 micron: Will the Speed Bumps Slow the Race to Market?” This panel is organized by Bill Alexander, and moderated by Jacques Benkoski. Dinner will be served prior to these panels. The title of the embedded panel, which will take place on Wednesday afternoon, is “Consequences of Technology - What is the Impact of Electronic Design on the Quality of Life?” This panel is organized by Gabriele Eckert, and moderated by Steve Ohr.

A new component of the technical program this year is the PhD student forum which allows Ph.D. students to present and discuss their thesis work with experts in the area of Electronic Design and Design Automation. The forum was organized by Kaushik Roy and provides Ph.D. students, who are active in the research in the electronic design automation, and design-related areas, with the opportunity to gain visibility and get feedback on their work, and for the industry to gain insight into the academic work-in-progress. The technical program also includes a special poster session where the authors will summarize their research results on a poster. Attendees of the poster session will be able to discuss issues directly with the authors and view the research results on the prepared posters.
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TUTORIALS

Monday, March 26, 8:30am-5:30pm
Features four Parallel Tracks with 12 tutorials. Includes breakfast, lunch, and coffee breaks.

PLENARY SESSIONS

Plenary session I:
Tuesday, March 27, 8:30am-11:50am
Features keynote speeches by Hajime Sasaki (Chairman of the board, NEC), Joe Costello (CEO, think3), Raul Camposano (CTO/GM, Synopsys), Edward Ross (President, TSMC, USA).

Plenary Session II:
Wednesday, March 28, 8:30am-11:50am
Features keynote speeches by Wojciech Maly (Professor, Carnegie Mellon University), Vinod Agrawal (CEO, Logic Vision), Aki Fujimura (COO and President, Simplex Solutions), and Philippe Magarshack (Vice President, Design Automation, STMicroelectronics).

PANEL DISCUSSIONS

Evening Panel Discussion 1 & Dinner
Monday, March 26, 6:30pm-8:30pm
The 50-Million Transistor Chip: The Quality Challenge for 2001
Sponsored by EE Times

Evening Panel Discussion 2 & Dinner
Tuesday, March 27, 6:30pm-8:30pm
0.13 micron: Will the Speed Bumps Slow the Race to Market?
Sponsored by Monterey Design & Fujitsu

Embedded Panel Discussion
Wednesday, March 28, 1:00pm-3:10pm
Consequences of Technology - What is the Impact of Electronic Design on the Quality of Life?

BEST PAPER AWARDS

Tuesday, March 27, 12:00pm-12:30pm.
ISQED will award three best papers during Luncheon.
Sponsored by Numerical Technologies and Nassada.

LUNCHEONS & DINNER RECEPITIONS

Evening Reception 1
Sponsored by EE Times
Monday, March 26, 6:30pm-8:30pm
Features panel discussion 1:
The 50-Million Transistor Chip: The Quality Challenge for 2001
7:00pm-8:30pm

ISQED Luncheon
Sponsored by Synopsys Inc.
Tuesday, March 27, 12:00pm-1:00pm
Features best paper awards and the best Ph.D. Student Forum awards.

Evening Reception 2
Sponsored by Monterey Design & Fujitsu
Tuesday, March 27, 6:30pm-8:30pm
Features panel discussion 2:
0.13 micron: Will the Speed Bumps Slow the Race to Market?
7:00pm-8:30pm

TECHNICAL SESSIONS

Eleven technical sessions, including 13 invited papers from leading industry experts, as well as 38 papers selected from over 93 papers.

PH.D. STUDENT FORUM

Posters will be on display on Wednesday afternoon from 1:00pm to 5:00pm.
Sponsored by Fujitsu, Tavanza, and PDF Solutions.
This special poster session devoted to Ph.D. students to present and discuss their thesis work in the area of Electronic Design, and Design Automation.

POSTER SESSION

Poster papers will be on display on Wednesday afternoon from 1:00pm to 5:00pm.
Authors will be available to discuss their work and to answer questions.
REGISTRATION INFORMATION

ADVANCE REGISTRATION
For advanced registration using the on-line registration process, visit the ISQED web site located at: http://www.isqed.org. Alternatively you can fill the conference registration form, which is attached in the centerfold of this booklet. The form and payment should be forwarded to the address shown in the form.

Payment must be included to process the registration form. Fax can be accepted only with the credit card payment. To qualify for the discounted advance registration rate, all the registrations must be carried out on-line prior to February 25th, or if done by mail, postmarked before February 25th, 2001. After February 25th, you can register on site. Please note that the tutorial registration is only available to the conference attendees.

ON-SITE REGISTRATION
Due to limited space, you are encouraged to register in advance. However, the conference on site registration is available at the DoubleTree hotel as follows:

TUTORIAL REGISTRATION
Sunday, March 25, 2001 5:00pm-8:00pm
Monday, March 26, 2001 8:00am-12:00 pm

TECHNICAL SESSIONS REGISTRATION
Sunday, March 25, 2001 5:00pm-8:00pm
Monday, March 26, 2001 8:00am-5:00pm
Tuesday, March 27, 2001 8:00am-5:00pm
Wednesday, March 28, 2001 8:00am-12:00pm

HOTEL RESERVATION
A block of rooms has been reserved at DoubleTree hotel for ISQED attendees. To make reservation, please complete the hotel reservation form, attached in the centerfold of this booklet. Send the form directly to DoubleTree hotel. To qualify for a room at the special rate, the reservation should be made before March 11, 2001. Please refer to the hotel reservation form for details. Due to limited room availability, early hotel reservation is recommended.
# IEEE ISQED 2001 Conference at a glance

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<td>Room: Monterey/Carmel</td>
<td>Room: Santa Clara/San Jose</td>
<td>Room: San Carlos/San Juan</td>
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<td>6:30 pm-8:30 pm</td>
<td><strong>Dinner Reception</strong>, Reception sponsored by EE Times</td>
<td><strong>Evening Panel Discussion 1: The 50-Million-Transistor Chip: The Quality Challenge for 2001</strong></td>
<td>Room: Oak</td>
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<td>Tuesday</td>
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<td><strong>Plenary Session 1</strong></td>
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<td>ISQED Best Paper Awards, Best Ph.D. Student Forum Award</td>
<td>Room: Pine</td>
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<td>Keynote speeches by:</td>
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<td>Hajime Sasaki, Joe Costello, Raul Composano, Edward Ross</td>
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<td><strong>Session 1A</strong></td>
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<td>Impact of Verification on Complex SOC Quality</td>
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<td>Design, Fabrication and Reliability Challenges for Emerging Technologies</td>
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<td>3:10 pm-3:30 pm</td>
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<td>Capacitive Crosstalk Analysis</td>
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<td>6:30 pm-8:30 pm</td>
<td><strong>Dinner Reception</strong>, Sponsored by Monterey Design &amp; Fujitsu</td>
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<td><strong>Ph.D. Student Forum Poster Session D</strong></td>
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<td>ISQED Best Paper Awards, Best Ph.D. Student Forum Award</td>
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<td>Impact of Verification on Complex SOC Quality</td>
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MONDAY TUTORIALS

Tutorial Track A

Chair: Yervant Zorian, Logic Vision

9:00am-12:00pm

Tutorial A1: System-on-Chip: Embedded Test Strategies
Organizer: Dimitris Gizopoulos, University of Piraeus, Greece
Presenter: Yervant Zorian, Logic Vision

Spurred by technology leading to the availability of millions of gates per chip, system-level integration is evolving as a new paradigm, allowing entire systems to be built on a single chip. This tutorial presents the state-of-the-art in system-level integration and addresses the strategies and current industrial practices in the test of system-on-chip. It discusses the requirements for test reuse in hierarchical design, such as embedded test strategies for individual cores, test access mechanisms, test interface standardization, optimizing test resource partitioning, and embedded test management and integration at the System-on-Chip level.

1:00-3:00pm

Tutorial A2: Design and Test of Low Voltage CMOS Circuits
Organizer: Kaushik Roy, Purdue University
Presenter 1: Kaushik Roy, Purdue University
Presenter 2: Ali Keshavarzi, Intel Corp

This tutorial focuses on challenges of low voltage CMOS design and test. As technology scales leakage and leakage control becomes critical for design and test of integrated circuits. We explain testing techniques for intrinsically leaky ICs. This tutorial covers the following topics: Scaling of MOS devices, Low-voltage low-power CMOS design style, Cross-talk issues and predictable design, Transistor threshold scaling for high performance designs, Leakage current in CMOS circuits, Leakage control techniques such as multiple VT CMOS, dynamic VT CMOS, transistor stacking, Testing of low voltage low threshold CMOS circuits under elevated background leakage.

3:30pm-5:30pm

Tutorial A3: Redundancy Requirements for Embedded Memories
Organizer: Mo T amjidi, Dolphin Technology
Presenter 1: Mo Tamjidi, Dolphin Technology
Presenter 2: Bijoy Gumman, Genesys Testware

Multi-megabit embedded random access memories are widely used in complex system on chip ICs. The manufacturing yield of these system ICs, and consequently their unit cost is mainly dependent on the yield of these embedded memories. The yield of large embedded memories can be easily increased using spare memory cells, which are substituted for faulty memory cells during the manufacturing test process. The three main approaches to memory substitution are using laser blown fuses, electrical fuses and dynamic repair. Laser fuse based repair is the most popular approach. However, this increases test costs substantially since a 3-step test process (test, laser repair, retest) is required. Electrical fuse based repair can be performed as a single process on the IC tester. However, electrical fuses are not supported in most processes. Dynamic repair uses Built-In Self-Test, Diagnosis and Repair Circuitry, which recalculates faulty locations and remaps them to spare locations on system power-up. This approach does not require any changes to the backend manufacturing process. However, process-voltage-temperature sensitive failures cannot be corrected since the power-up operating point is unpredictable.
ADVANCE REGISTRATION FORM
# ISQED Advanced Registration Form

## 2001 IEEE International Symposium on Quality Electronic Design

March 26-28, 2001, DoubleTree Hotel, San Jose, CA

Last Name (Family Name) _________________ First ______________ Initial.____

Company/University ___________________________________________

Address ______________________________________________________

City _______________________ State/Country _______ Zip Code ____________

Work Phone (____) ________________ Fax (____) ________________

Email ________________________

Membership Information (required for discounted rates):
Mark ONLY ONE.

IEEE Member No. ______________________________________________________

ACM Member No. ______________________________________________________

FSA Member Company Name ____________________________________________

Full Time Student:
University Name _______________________ Student ID # ____________________

Mail this form and payment to:

ISQED Registrar
Christy A. Lankenau
Registration Coordinator
445 Hoes Lane
Piscataway, NJ 08855-1331
PH: 732.981.3415
Fax: 732.465.6447
Email: isqedreg@ieee.org

Make checks payable to:

IEEE ISQED 2001

Payment must be included to process this form. Fax can be accepted only with the credit card payment. Requests for cancellation or refund must be received before February 25th, 2001. A $25 processing fee will be withheld from the refund.

For Office Use Only

Check #
Amount $ ______________________
Deposit Date ______________

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Registration payment can be made by check (US Dollar on a US bank) or credit card.

Payment method:  
☐ Check enclosed for amount due $__________
☐ Credit-card  Type:  ☐ Visa  ☐ Mastercard  ☐ American Express (no Discover card)
☐ Wire Transfer  Amount Wired _____________ (*See instructions below)

Credit Card Number _________________ Exp. Date __________ Signature ______________________

* IEEE/TCMS Wire Transfer Instructions:

1. CONFERENCE BANK NAME: FLEET BANK, BOSTON, MASSACHUSETTS, USA  
2. BANK ACCOUNT #: 8459001469  
3. BANK ACCOUNT NAME: IEEE TRAVEL SERVICES  
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SPECIAL INSTRUCTIONS: Please be sure to add appropriate wire transfer charges to the Registration fees in order to avoid an outstanding balance. To insure proper credit to your account, you MUST SPECIFY in the Wire Transfer “Transaction Description” area the CONFERENCE AND ATTENDEE NAME. Attach a copy of the Wire Transfer RECEIPT with a copy of your registration. These instructions MUST BE FOLLOWED in order to apply payment accurately to your fees.
ISQED HOTEL RESERVATION FORM
IEEE ISQED 2001
March 25-28, 2001
Doubletree Hotel, San Jose, CA USA

A block of rooms has been reserved at the DoubleTree Hotel for ISQED participants. Special ISQED room rate is $159 for Single/Double. This rate is exclusive of applicable sales/room tax, currently 10.06 percent. This special rate will apply to all the registrations made before or on Sunday, March 11, 2001 before 5pm. All reservations made after the cut-off date will be based on space and rate availability only. Hotel check-in time is 3pm and the checkout time is noon.

To make a reservation, please complete this form and send it to the following address by mail or fax.

DoubleTree Hotel
Attention: Reservations
2050 Gateway Place
San Jose, CA 95110
Tel: (408) 453-4000
Fax: (408) 437-2898

Event Name: IEEE Computer Society ISQED 2001

Guest Name _________________________________________________________________________________________________

Company ___________________________________________________________________________________________________

Address _____________________________________________________________________________________________________

City ______________________________________________________________ State _______ Zip Code ______________________

Country _____________________________________ Phone ___________________________ Fax ___________________________

Arrival Date ______________________________________________ Arrival Time _________________________________________

Departure Date _________________________________________ Departure Time ________________________________________

Rooms will be held only until 6:00 pm unless guaranteed for late arrival by a credit card or an advanced deposit.

DoubleTree hotel will send you the reservation confirmation.

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Signature __________________________________________________________________________________________________

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HOTEL REGISTRATION FORM
**Tutorial Track C**

Chair: Frank Lee, Avant!

9:00am-12:00pm

**Tutorial C1: Application of Formal Verification to Design Creation and Implementation**

Organizer: Noel Strader, Avant!
Presenter 1: Andrew Moore, TSMC
Presenter 2: John Ferguson, Mentor Graphics
Presenter 3: NS Nagraj, Texas Instruments

Successful design requires verification at both the design creation phase and the design implementation phase. We consider the design implementation phase to occur once a “golden” design description is available. Formal equivalence checks and their application to this phase are described. The design creation phase builds the golden design description from the design specification. Formal verification of this phase is less mature and more difficult. Best current technology in use is described here.

Verification of the design creation phase is less mature. Here, several approaches are used including model checking (based on BDDs, SAT, or ATPG), symbolic simulation (STG) and theorem proving. There are many hybrid approaches proposed and used in semiconductor companies; finding still more effective approaches is a big challenge.

1:00pm-3:00pm

**Tutorial C2: Verification and Validation of Complex Digital Systems: An Industrial Perspective**

Organizer: Li-C. Wang, UC-Santa Barbara
Presenter 1: Magdy S. Abadir, Motorola
Presenter 2: Gerard Memmi, Avant!
Presenter 3: Carl Pixley, Motorola

Verification and validation of complex digital designs (microprocessors, large ASICs, SOCs, etc.) are very challenging in today’s industry. Traditionally, they rely upon extensive simulation that typically consumes a large amount of compute and design resources. The effectiveness of traditional approaches becomes questionable as the size and complexity of industrial designs increase rapidly. This tutorial aims to provide an overview of practical verification/validation methodologies in use today. It will highlight the key challenges and how these methodologies are evolving. Designers, verification practitioners, as well as tool developers can all be benefited from learning the up-to-date technologies and application issues/limitations of specific approaches.

We will first survey state-of-the-art techniques widely used in the industry, such as functional verification, directed and random testing, and equivalence checking. We will then describe advanced methods, including symbolic simulation, formal verification, ATPG-based verification, design error modeling, and design-for-debug/verification. During the tutorial, we will emphasize the relationship among validation, verification, and test. The tutorial will be primarily based on industrial experiences and real designs. Stories of success as well as failure will be presented. Strengths and weaknesses of various methodologies and a proper mix of tools in practice will be illustrated. Promising techniques and research directions for the future will be discussed.

3:30pm-5:30pm

**Tutorial C3: Physical Verification at 0.13 Micron and Below**

Organizer: John Ferguson, Mentor Graphics
Presenter 1: Andrew Moore, TSMC
Presenter 2: John Ferguson, Mentor Graphics

The advent of 0.13-micron and below production processes has increased capacity to multi-million gate designs. The data that must be managed is measured in hundreds of MB and billions of polygons. In addition, physical aspects of manufacturing must now be dealt with at the design stage, going far beyond traditional DRC.

The tutorial will present a survey of hierarchical verification and manufacturing issues that are required today and in the future. Example solutions of common problems in the field today will be shown, including: CMP density and tiling, metal slotting, and antenna detection.

**Tutorial Track D**

Chair: Tak Young, Monterey Design

9:00am-12:00pm

**Tutorial D1: Re-Connecting MOS Modeling and Circuit Design: New Methods for Design Quality**

Organizer: Daniel Foty, Gilgamesh Associates
Presenter 1: Daniel Foty, Gilgamesh Associates
Presenter 2: David Binkley, UNC Charlotte

Amid the blizzard of design-automation technologies, the analytical MOSFET models (and their associated model parameter sets) receive scant attention from the design community. However, these models and parameter sets are fundamental to the design process, since they represent the critical “communication link” between a design group and its wafer foundry. In particular, analog integrated circuit design is carried out at the transistor level; however, this fundamental aspect of analog design has not received much attention. The digital designer is also severely affected by slow MOS models, accuracy problems, and unpredictable model behavior.

The first part of this tutorial will examine the present “infrastructure” of MOS modeling for circuit simulation, with particular emphasis on how history has played a role at least as large as that of engineering. The tenor will be one of practical information for the circuit design “consumer” of transistor models. The second part of this tutorial will make the connection between MOS modeling and a modern approach to designing analog and digital integrated circuits. Here, it will be shown that a proper structural approach to MOS transistor modeling permits a more direct path to the key circuit information, allowing a designer to more carefully make decisions about critical design trade-offs.

1:00pm-3:00pm

**Tutorial D2: Interconnect Modeling for Timing, Signal Integrity and Reliability**

Organizer: Narain Arora, Simplex Solutions
Presenter 1: Narain Arora, Simplex Solutions
Presenter 2: NS Nagraj, Texas Instruments

As VLSI technology shrinks to deep sub-micron geometries below 0.25um, the propagation delay due to interconnects (wiring) begins to dominate the total chip delay. In fact, parasitic due to interconnects are becoming limiting factors in determining circuit performance. An accurate estimation of the interconnects R (resistance), C (capacitance) and L (inductance) parasitic effects is thus essential in...
determining various interconnect related issues such as delay (timing), crosstalk, IR drop, power dissipation, electromigration, etc.

This course will cover interconnect issues in chip design, particularly its impact on timing and reliability of integrated circuits. Starting with defining interconnect as a parasitic element, we will cover interconnect scaling laws and discuss analytical and numerical methods of calculating interconnect $R$, $C$, and $L$. This will be followed by discussing techniques for extracting $R$, $C$ and $L$ at the chip level. We will also briefly cover verification and calibration of interconnect capacitance models using silicon test chip.

The next section of the tutorial begins with an overview of model order reduction techniques for analyzing large RLCK networks. Parasitic coupling impact on delay and noise will be discussed in detail. Analysis methods for electromigration on signal and power lines will be presented. Practical considerations in crosstalk delay, crosstalk noise and electromigration analysis of large ULSI designs will be presented.

3:30pm-5:30pm
**Tutorial D3: On-Chip Inductance Extraction and Modeling**

**Organizer:** Tak Young, Monterey Design

**Presenter 1:** David Blaauw, Motorola

**Presenter 2:** Rajendran Panda, Motorola

With the VLSI feature sizes going deep submicron, interconnect issues have become dominant among the design issues. Interconnect issues now play a vital role in the performance of DSM circuits, and hence accurate analysis and careful design of interconnects is of critical importance in realizing quality designs with ambitious performance goals. Traditional models for interconnects considering only the $R$ and $C$ effects are proving to be inadequate in the DSM regime, especially for the global signal routes. The variation in delays and skews due to parasitic inductance is no longer ignorable, more so at GHz clock speeds. The “far coupling” effect of inductance is posing additional problems in analyzing and designing for possible signal integrity problems. Another trend affecting the performance and functional integrity of a design is the noise induced by the power supply network during abrupt power transience. Therefore, extracting and analyzing a detailed RLC model of the on-chip power interconnect, package, and decoupling structures is necessary to design a reliable supply network.

The first part of this tutorial will be devoted to provide the audience a comprehensive understanding of the various issues concerning inductance. We will then cover some of the popular approaches in modeling on-chip inductance, and analyzing the resulting large RLC networks, their complexity, and limitations. The objective here will be to equip a designer audience with an ability to evaluate and size up the claims of vendors for inductance extraction/analysis tools. The tutorial will then address various design issues and present methods to tackle noise in global signals and also noise induced by power supply network.

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**MONDAY**

**Session EP1**

Dinner reception, sponsored by EE Times

**Evening Panel Discussion**

6:30pm-8:30pm

**The 50-Million Transistor Chip: The Quality Challenge for 2001**

**Organizer:** Rick Merrit, Editor in Chief, EETimes

**Moderator:** Richard Goering, Managing Editor Design Automation, EETimes

**Description**

The panel will examine the core issues that leading edge semiconductor makers face in making quality and time-to-market decisions about how they design, verify and test high-end silicon devices.

One provocative question that can be posed is, “How much verification is enough?” Every design team must come to a point where a chip design is completed and ready for fabrication — but knowing when you’ve hit that point is very difficult. There are few guidelines or metrics. It’s pretty much a subjective, seat-of-the-pants kind of decision, although there are a few tools (such as code coverage tools) that might offer some help.

In the manufacturing test area, a similar question arises – “How much fault coverage is enough?” Just a slight increase in coverage can make a tremendous difference in yield, but those last few percentage points of fault coverage can be painfully difficult to get.

A panel representing users, EDA vendors, and semiconductor executives will share their experiences and concerns about verification and test.

**Panelists:**

**Thomas Daniel**
VP ASIC Technology,
LSI Logic,
Milpitas, CA

**Bryan Hoyer**
Senior Director of System Level Solutions,
Altera,
San Jose, CA

**Chris Malachowsky**
VP Engineering,
Nvidia,
Santa Clara, CA

**Janusz Rajski**
Chief Scientist,
Design “for” Test,
Mentor Graphics,
Portland, OR

**Greg Spirakis**
VP Microprocessor Products Group,
GM MPG Design Technology,
Intel,
Santa Clara, CA

**Tom Williams**
Chief Scientist and Director Test,
Synopsys,
Mountain View, CA
8:30am
Welcome and Introduction

8:45am
1P.1 Future Platform for Mobile Communication

Hajimi Sasaki,
Chairman of the Board,
NEC

This keynote would explore three driving forces in the IT revolution that are actualizing an Information Society: first, the Internet global, ever expanding nature and second, the ability to create the ultimate personal information tool. And last, at the heart of these forces is the cutting-edge semiconductor device. Especially in mobile where products are composed primarily of semiconductors, we see that the creation of advanced semiconductor devices controls to a large degree the superior nature of the mobile product. Mobile products must balance many constraining criteria such as size and weight against functionality such as low power consumption. There are also a wide array of technologies involved such as low power consumption circuit design, flash memory and RF power device. Additionally, intellectual property has become even more important.

Moreover, the harmonization of semiconductor technology and peripheral technologies such as small-scale, light-weight packaging technology, long life rechargeable batteries and flat panel displays has become an important factor.

9:25am
1P.2 Delivering Quality Delivers Profits

Joe Costello,
Chairman & CEO, think3

The future of electronics is SoC design. SoC design complexity is accelerating due to rapid change on multiple dimensions: design content, deep sub-micron (DSM) electrical and physical effects, and the sheer scale of SoC projects. At the same time, market windows are dramatically decreasing. These fundamental technology trends and economic forces underscore the need to rethink conventional design methodology and conventional business practices for SoC design delivery.

An SoC design foundry, combining a fast and scalable mixed-signal SoC design methodology with innovative design technology and electrical engineering expertise, enables not only the timely delivery of SoC designs, but also robust design quality through electrically correct silicon engineering.

10:05am
Break

10:30am
1P.3 The Expanding Use of Formal Techniques in Electronic Design

Raul Camposano,
CTO/GM, Synopsys, Inc.

Although Electronic Design Automation (EDA) tools allow some tolerance for features having only limited scope or not working in all cases, there is no tolerance for error in their final results. Since the beginning, EDA tools have included so-called "formal" techniques to ensure such error-free results. More and more, formal verification tools are being adopted as a necessary part of mainstream design flows to tackle the exploding verification challenge. In this keynote address, we will focus on some of these formal techniques; in particular, equivalence checking, property checking, and the combination of simulation with formal techniques — all of which play an important role in creating zero-defect results in state-of-the-art electronic design.

11:10am
1P.4 IC Design Methodology in the Foundry Era: Introducing 'Heads-Up' Design

Edward C. Ross,
President, TSMC, USA

The emergence of the foundry as a primary semiconductor manufacturing resource has created a sea-change in the way EDA companies interact with manufacturers. Since the key concern for many foundry customers is time-to-volume, EDA companies are now focused not just on system-level design, but on "heads-up" design, e.g., bringing to designers the ability to build whole systems at the speed of thought. Dr. Ross discusses emerging trends in the EDA, IP, library and design center communities, wherein deep collaboration with foundries is producing a variety of Internet-based solutions that are revolutionizing IC design methodologies.
Session 1A
1:00pm – 3:10pm
Impact of Verification on Complex SOC Quality
Co-Chairs: Marco Casale-Rossi, STMicroelectronics, Milan, Italy
Eileen Hong You, Sun Microsystems, Palo Alto, California

1:00pm
Introduction

1:05pm
1A.1 Stopping Criteria Comparison: Toward High Quality Behavioral Verification
Amjad Hajjar, Tom Chen, Isabelle Munn, Anneliese Andrews, and Maria Bjorkman, Colorado State University, Colorado

1:30pm
1A.2 Concrete Impact of Formal Verification on Quality in IP Design and Implementation
Umberto Rossi, Andrea Fedeli, Marco Boschini, and Franco Toto, STMicroelectronics, Milan, Italy

1:55pm
1A.3 Simulation Using Code-Perturbation: Black- and White-Box Approach
Zan Yang, Byeong Min, and Gwan Choi. Texas A&M University, College Station, Texas

2:20pm
1A.4 A “Design for Verification” Methodology
Francesco Sforza, Luca Battu’, Marco Brunelli, Andrea Castelnuovo, and Mauro Mgnahi, STMicroelectronics, Milan, Italy

2:45pm
1A.5 A Hardware and Software Monitor for High-Level System-on-Chip Verification
Mohammed El Shobaki and Lennart Lindh, M alardalen University, Vasteras, Sweden

Session 1B
1:00pm – 3:10pm
Quality of EDA Tools and Design Methodologies
Co-Chairs: Tom Chen, Hewlett-Packard/Colorado State University, Fort Collins, Colorado
Steve Start, AMI Semiconductors, Idaho

1:00pm
Introduction

1:05pm
1B.1 Techniques that Improved the Timing Convergence of the Gekko PowerPC Microprocessor (Invited)
Paul Kartschoke1, and Shervin Hojat2. 1IBM Microelectronics, Essex Junction, Vermont; 2Sun Microsystems

1:30pm
1B.2 I/O Cell Placement and Electrical Checking Methodology for ASICs with Peripheral I/Os
Gulsun Yasar, Charles Chiu, Robert A. Proctor, and James P. Libous, IBM Microelectronics, Essex Junction, Vermont

1:55pm
1B.3 Applying Moore’s Technology Adoption Life Cycle Model to Quality of EDA Software (Invited)
Giora Ben-Yaacov, Edward P. Stone, and Rich Goldman, Synopsys, Mountain View, California

2:20pm
1B.4 A System for Automatic Recording and Prediction of Design Quality Metrics
Andrew B. Kahng, and Stefanus M antik, University of California at Los Angeles, Los Angeles, California

2:45pm
1B.5 Scripting for EDA Tools: A Case Study
Pinhong Chen1, Desmond A. Kirkpatrick2, and Kurt Keutzer1, 1University of California at Berkeley, Berkeley, California, 2Intel Corporation, Hillsboro, Oregon

Session 1C
1:00pm – 3:10pm
Design, Fabrication and Reliability Challenges for Emerging Technologies
Co-Chairs: Bharath Rajagopalan, Texas Instruments, Texas
Hirokazu Yonezawa, Matsushita Electronics Corporation, Japan

1:00pm
Introduction

1:05pm
1C.1 High Quality Analog CMOS and Mixed Signal LSI Design (Invited)
Akira Matsuzawa, Matsushita Electric Industrial, Osaka, Japan

1:30pm
1C.2 CAD Issues for CMOS VLSI Design in SOI (Invited)
Kenneth L. Shepard, Columbia University, New York, New York and CadMOS Design Technology, San Jose, California

1:55pm
1C.3 Foundry’s Perspective of System Integration: Quality Design and Time to Volume (Invited)
Sheldon Wu2, Fred Wang1, and Lie-Szu Juang2, 1TSMC, Taiwan, 2TSMC North America

2:20pm
1C.4 Analysis and Design of ESD Protection Circuits for High-Frequency/RF Applications
Choshu Ito, Kaustav Banerjee, and Robert W. Dutton, Stanford University, Stanford, California

2:45pm
1C.5 Scaling-Induced Reductions in CMOS Reliability Margins and the Escalating Need for Increased Design-In Reliability Efforts (Invited)
J. W. McPherson, Texas Instruments, Inc., Dallas, Texas
Session 2A
3:30pm - 5:40pm

Capacitive Crosstalk Analysis

Co-Chairs: Justin Harlow, Semiconductor Research Corporation, North Carolina
           David Overhauser, Simplex Solutions, San Jose, California

3:30pm Introduction

3:35pm

2A.1 A Fast Coupling Aware Delay Estimation Scheme Based on Simplified Circuit Model
Ninglong Lu, and Ibrahim N. Hajj, University of Illinois at Urbana-Champaign, Urbana, Illinois

4:00pm

2A.2 A Model for Crosstalk Noise Evaluation in Deep Submicron Processes
Pirouz Bazargan-Sabet1, and Fabrice Ilponse 2, 1University of Paris, Paris, France, 2ST Microelectronics, Crolles, France

4:25pm

2A.3 Noise Model for Multiple Segmented Coupled RC Interconnects
Andrew B. Kahng, Sudhakar Muddu, Niranjan Pol, and Devendra Vidhani, University of California at Los Angeles, Los Angeles, California

4:50pm

2A.4 New Efficient and Accurate Moment Matching Based Model for Crosstalk Estimation in Coupled RC Trees
Qingjian Yu, and Ernest S. Kuh, University of California at Berkeley, Berkeley, California

5:15pm

2A.5 A Global Driver Sizing Tool for Functional Crosstalk Noise Avoidance
Murat R. Becer1, David Blaauw2, Suparnas Sirichotiyakul2, Rafi Levy3, Chanhee Oh4, Vladimir Zolotov4, Jinyang Zuo4, and Ibrahim N. Hajj1, 1University of Illinois at Urbana-Champaign, Urbana, Illinois, 2Motorola Inc., Austin, Texas, 3Motorola Semiconductor Israel Ltd., Israel

Session 2B
3:30pm - 5:40pm

Interconnect Modeling and Analysis

Co-Chairs: Norain Arora, Simplex, Sunnyvale, California
           Kastav Banerjee, Stanford University, Stanford, California

3:30pm Introduction

3:35 pm

2B.1 Models For Interconnect Capacitance Extraction (Invited)
Asim Husain, Intel Corporation, Santa Clara, California

4:00pm

2B.2 Impact of On-Chip Inductance When Transitioning from Al to Cu Based Technology
Tom Chen, Hewlett Packard, Fort Collins, Colorado

4:25pm

2B.3 Computational Cost Reduction in Extracting Inductance
Yusuke Nakashima, M akoto Ikeda, and Kunihiro Asada, University of Tokyo, Tokyo, Japan

4:50pm

2B.4 Effective On-chip Inductance Modeling for Multiple Signal Lines and Application on Repeater Insertion
Yu Cao1, Xuejue Huang1, Norman Chang2, Shen Lin2, O. Sam Nakagawa2, Weize Xie2, and Chenming Hu1, 1University of California at Berkeley, Berkeley, California, 2Hewlett-Packard Laboratories, Palo Alto, California

5:15pm

2B.5 Signal Attenuation in Transmission Lines
Mehdi Mechak, Cisco Systems, San Jose, California

Session 2C
3:30pm - 5:40pm

Power-Aware Design

Co-Chairs: Kaushik Roy, Purdue University, West Lafayette, Indiana
           George Stamoulis, Intel Corporation

3:30pm Introduction

3:35 pm

2C.1 Memory Bus Encoding For Low Power: A Tutorial
Wei-Chung Cheng, and Massoud Pedram, University of Southern California, Los Angeles, California

4:00pm

2C.2 RC Power Bus Maximum Voltage Drop in Digital VLSI Circuits
Geng Bai, S. Bobba, and Ibrahim N. Hajj, University of Illinois at Urbana-Champaign, Urbana, Illinois

4:25pm

2C.3 Instruction Prediction for Step Power Reduction
Zhenyu Tang1, Norman Chang2, Shen Lin2, Weize Xie2, Sam Nakagawa2, and Lei He1, 1University of Wisconsin, Madison, Wisconsin, 2Hewlett-Packard Laboratories, Palo Alto, California

4:50pm

2C.4 Power Trend and Performance Characterization of 3-Dimensional Integration for Future Technology Generations
Rongtian Zhang, Kaushik Roy, Cheng-Kok Koh, and David B. Janes, Purdue University, West Lafayette, Indiana

5:15pm

2C.5 A Compact Layout Technique for Reducing Switching Current Effects in High Speed Circuits
J.A. Montiel-Nelson, V. de Armas, R. Sarmiento, and A. Nunez, University of Las Palmas de Gran Canaria, Spain
Plenary Session II
8:30am-11:50am

Co-Chairs: Res Saleh, ISQED Program Chair
Kris Verma, ISQED Plenary Committee Chair

8:30am
Introduction

8:45am
2P .1 Quality of Design from an IC Manufacturing Perspective
Wojciech P. Maly, Professor, Carnegie Mellon University

There are many credible sources (including the ITRS) now seeing cost of IC manufacturing as a potentially negative factor that may affect the future of the IC industry. There are also a number of answers to the growing-cost-of-manufacturing challenge. One of them is IC design for efficient manufacturing — measured by such indices as yield, time-to-volume, etc.

The first objective of this presentation is to analyze publicly discussed visions for the IC industry and derive from them manufacturability conditions that must be met for these visions to materialize. We will focus our discussion on the recent version of the ITRS. It will be shown that ITRS predictions cannot be fulfilled by design or manufacturing approaches alone. Only by solving complex trade-offs on the design-test-manufacturing interface one may provide a chance to overcome the rising-cost-of-manufacturing problem — the main stumbling block on the ITRS horizon.

The second objective of the presentation is to propose a redefinition of the notion of the quality of IC design, so it can accommodate manufacturability measures as primary design goals in addition to traditional die size, performance and time-to-first-silicon design quality indices. Such a re-definition is possible and maybe necessary contribution of the IC design community in addressing the rising-cost-of-manufacturing problem.

9:25am
2P .2 Embedded Test Leads to Embedded Quality
Vinod Agrawal, CEO, Logic Vision

The concept of embedded test, wherein physical test engines are built right on to the semiconductor chip, has a very strong quality value throughout the lifecycle of the chip. These embedded testers can be reused throughout the lifetime of the chip from silicon debug, to characterization, to production testing (both wafer probe and final test), to board prototyping, to system integration and then finally to the diagnosis in the field.

More than 50 semiconductor and system companies world-wide are already using embedded test in their complex chips, to gain significant quality, cycle time and economic competitive advantage. This talk will explore how embedded test is becoming a standard choice for IC and system developers.

9:25am
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10:05am
Break
Plenary Session II continued

10:30am

2P.3 Quality on Time

Aki Fujimura, COO and President, Simplex

How is it that a group of talented, highly motivated, hard-working software engineers consistently produce low-quality software, late? It is the speaker’s view that schedule management and quality management go hand in hand. The traditional thinking that quality and schedule are tradeoffs is exactly the approach to engineering management that starts the downward spiral resulting in organizations that can never deliver quality software nor on-time delivery. The talk discusses the notion that schedules are probability distributions, and presents several practical quality and schedule management techniques.

11:10am

2P.4 Quality of SoC Designs Through Quality of the Design Flow: Status and Needs

Philippe Magarshack, Vice President, Central R&D Group and Director, Design Automation, STMicroelectronics

It is now universally recognized that System-on-Chip (SoC) is the appropriate product solution to meet the demand of cost and volume for many electronics markets. The increasing pressures coming from shrinking market windows, accelerating process roadmaps and increasing mask costs, render necessary that SoC be correct at first silicon. This is becoming a considerable challenge due to the complexity of systems that can be built on the same chip: current process capabilities are approaching 100 million devices. Additionally, this level of integration comes at the price of renewed parasitic effects, such as crosstalk, voltage drop and electro-migration.

A complex design flow is necessary to solve these conflicting trends, combining executable specifications, isolating function from communication, exploring architectures and trading off speed, power, area and schedules, and finally a fast route to implementation, be it in software running on embedded processors, dedicated digital hardware, or dedicated analog cells. The successive levels of abstraction of the system description warrant the need for extensive verification of the SoC, both at functional level, and at the timing, power and reliability levels.

Building such a design flow calls for mixing very good point tools, coming from established EDA vendors as well as start-ups and academia. But above all, it requires well-defined and structured interfaces between tools at key hand-off points in the design flow. Standard design languages and Application Programming Interfaces (API’s) are fundamental to the success of SoC.

Session D

1:00pm – 5:00pm

PhD Student Forum Poster Session

Co-Chair: Kaushik Roy, Purdue University, West Lafayette, IN
Hamid Rategh, Tavanz, Santa Clara, CA

D.1 Soft Core Based Model of a Microcomputer Family
Nguyen Quang Trung, Prof. Krystyna Siekierska, Institute of Electronics Technology, Warsaw, Poland

D.2 Design on ESD Protection Circuit with Very Low and Constant Input Capacitance
Tung-Yang Chen, Prof. Ming-Dou Ker, Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan

D.3 Diversity Techniques for Concurrent Error Detection
Subhasish Mitra, Prof. Edward J. McCluskey, Stanford University, Stanford, California

D.4 Refinements of Rent’s Rule Allowing Accurate Interconnect Complexity Modeling
Peter Verplaetse, Prof. Jan Van Campenhout, Ghent University, Belgium

D.5 Test Pattern Generators for Distributed and Embedded Built-In Self-Test at Register Transfer Level
Vladimir Vorisek, Prof. Elena Gramatova, Slovak Academy of Sciences, Slovakia

D.6 Design, Integration and Validation of Heterogeneous Systems
Steffen Klupsch, Prof. Sorin A. Huss, Darmstadt University of Technology, Darmstadt, Germany

D.7 RC Power Bus Maximum Voltage Drop in Digital VLSI Circuits
Geng Bai, S. Bobba and Prof. I. N. Hajj, University of Illinois at Urbana-Champaign, Urbana, Illinois

Session E

1:00pm – 5:00pm

Poster Session

Co-Chair: Res Saleh, University of British Columbia, Vancouver, B.C. Canada
Tak Young, Monterey Design, Sunnyvale, CA

E.1 Constructive Floorplanning with a Yield Objective
Rajnish K. Prasad, and Israel Koren, University of Massachusetts, Amherst, Massachusetts

E.2 Compact Layout Rule Extraction for Latchup Prevention in a 0.25-µm Shallow-Trench-Isolation Silicided Bulk CMOS Process
Ming-Dou Ker1, Wen-Yu Lo2, Tung-Yang Chen1, Howard Tang2, S. S. Chen2, M.-C. Wang2, 1National Chiao-Tung University, Taiwan, 2UMC, Taiwan
Session 3A
1:00 pm - 3:10pm

Defect Analysis and Test Generation

Co-Chairs: Fadi Maamari, LogicVision, San Jose, California
           George Ph. Alexiou, University of Patras and Computer
           Technology Institute, Patras, Greece

1:00pm

Introduction

1:05 pm

3A.1 Revisiting the Classic Fault Models through a Detailed
     Analysis of Realistic Defects (Invited)
     Michel Renovell, LIRMM, Montpellier, France

1:30pm

3A.2 Defect-Oriented Fault Simulation and Test Generation in
     Digital Circuits
     Raimund Ubar1, Wieslaw Kuzmicz2, Witold Pleskacz2, and Jaan
     Raik1, 1Tallinn Technical University, Tallinn, Estonia, 2Warsaw
     University of Technology, Poland

1:55pm

3A.3 Automatic Functional Vector Generation Using the Interacting
     FSM Model
     Chien-Nan Jimmy Liu, Chia-Chih Yen, and Jing-Yang Jou,
     National Chiao Tung University, Hsinchu, Taiwan

2:20pm

3A.4 Color Counting and its Application to Path Delay Fault
     Coverage
     Jayant Deodhar1, and Spyros Tragoudas2, 1Intel Corporation, Austin,
     Texas, 2Southern Illinois University at Carbondale, Carbondale,
     Illinois

2:45pm

3A.5 ATPG for Path Delay Faults without Path Enumeration
     Maria Michaud, and Spyros Tragoudas, Southern Illinois University
     at Carbondale, Carbondale, Illinois
The way communication, business and life-style changed, would not be possible without electronic design. The applications for electronic devices are unlimited and what sounds science fiction today, will be common sense tomorrow. Are there impacts on the way we operate as a society? What are the opportunities we have by utilizing actual and future electronic devices of all sorts? Where will electronic design take us?

One controversial question is how risky are computer-oriented communication, transactions, and operations, and how they can influence the quality of our life. Despite computer and electronic design related failures throughout the world, the increase of new applications of electronic devices will not slow down in the next decade.

Another provocative question will be how growing EMF influence electronic devices as well as the human body. How much trust in electronic design is healthy in the long term?

The panel, representing scientists, electronics and design executives, will share their visions, experiences and concerns regarding the impact of electronic design on our life.

Panelists:

Peggy Ayecinena
Editor,
ISD Magazine,
CMP Media
San Mateo, CA

Sabrina Kemeny
CEO and President,
Photobit, CA

Tom Mahon
Author,
President of Tom Mahon Associates
Walnut Creek, CA

Peter G. Neumann
Principal Scientist,
Stanford Research Institute,
Stanford, CA,
Co-Founder of PFIR – People for Internet Responsibility

Session 3C
1:00pm - 3:10pm

Embedded Panel Discussion

Consequences of Technology - What is the Impact of Electronic Design on the Quality of Life?

Organizer:  Nader Vasseghi, CEO, Auroranetics
Moderator:  Steve Ohr, Managing Editor, EDTN Networks

Electronic design changed the world in every aspect of our life. Latest semiconductor process technologies allow the integration of 50 million transistor chips and beyond. The panel will examine the impact of electronic design on our day-to-day life.

Session 3B
1:00pm - 3:10pm

Design of Programmable and Platform-Based IP

Co-Chairs:  Antonio Nunez, University of Las Palmas de Gran Canaria, Las Palmas GC, Spain
Vamsi Srikantam, Agilent Technologies, Palo Alto, California

1:00pm
Introduction

1:05 pm
3B.1 HW-SW Co-Design and Verification of a Multi-Standard Video and Image Codec (Invited)
Rafael Peset Llopis, Marcel Oosterhuis, Sethuraman Ramanathan, Paul Lippens, Albert van der Werf, Steffen Maul, and Jim Lin, Philips Research Laboratories, Eindhoven, The Netherlands

1:30pm
3B.2 Acceleration of DAB Chipset Development by Deployment of a Realtime Rapid Prototyping Approach based on Behavioral Synthesis (Invited)
Martin Spießl, Michael Schlicht, and Martin Leyh, FhG Erlangen, Erlangen, Germany

1:55pm
3B.3 ELITE Design Methodology of Foundation IP for Improving Synthesis Quality
Chih-Yuan Chen, and Shing-Wu Tung, Industrial Technology Research Institute, Taiwan, Republic of China

2:20pm
3B.4 High-quality FPGA Designs through Functional Decomposition with Sub-function Input Support Selection Based on Information Relationship Measures
Artur Chojnacki, and Lech Jozwiak, Eindhoven University of Technology, Eindhoven, The Netherlands

2:45pm
3B.5 Implementation of Multipliers in FPGA Structures
Kazimierz Wiatr, and Ernest Jamro, AGH Technical University Cracow, Krakow, Poland

Session 4A
3:30pm - 5:15pm

Design for Manufacturability

Co-Chairs:  Tuna Tarim, Texas Instruments, Dallas, Texas
Carlo Guardiani, PDF Solutions, San Jose, California

3:30pm
Introduction

3:35pm
4A.1 Early Detection of Design Sensitivities that Cause Yield Loss for New Products (Invited)
Ron Ross1, and Keith M Cccasland2, 1Texas Instruments, Santa Cruz, California, 2Texas Instruments, Tustin, California

4:00pm
4A.2 Assessment of True Worst Case Circuit Performance Under Interconnect Parameter Variations
Session 4B
3:30 – 5:15pm

Embedded Memories

Co-Chairs: Abed Mougharbel, Medtronic, Tempe, Arizona
Kris Verma, Seagate, Scotts Valley, California

3:30pm
Introduction

3:35pm
4B.1 A Fully Qualified Analog Design Flow for Non Volatile Memories Technologies
Pierluigi Daglio, M. Araldi, M. Morbarigazzi, and C. Roma,
STMicroelectronics N.V., Milan, Italy

4:00pm
4B.2 Memory Hierarchy Optimization of Multimedia Applications on Programmable Embedded Cores
K. Tatas1, A. Argyriou1, M. Dasigenis2, D. Soudris1, and N. Zervas2,
1Democritus University of Thrace, Xanthi, Greece, 2University of Patras, Patras, Greece

4:25pm
4B.3 A Method of Embedded Memory Access Time Measurement
Nai-Yin Sung, and Tsung-Yi Wu, Taiwan Semiconductor Manufacturing Company Ltd., Hsin-Chu, Taiwan, R.O.C.