IEEE 2001

2nd International Symposium on

Quality Electronic Design

March 26-28, 2001 - San Jose, CA

Delivering Quality Delivers Profits

Joe Costello

Chairman & CEO, think3

For System on a Chip Designs:

Quality

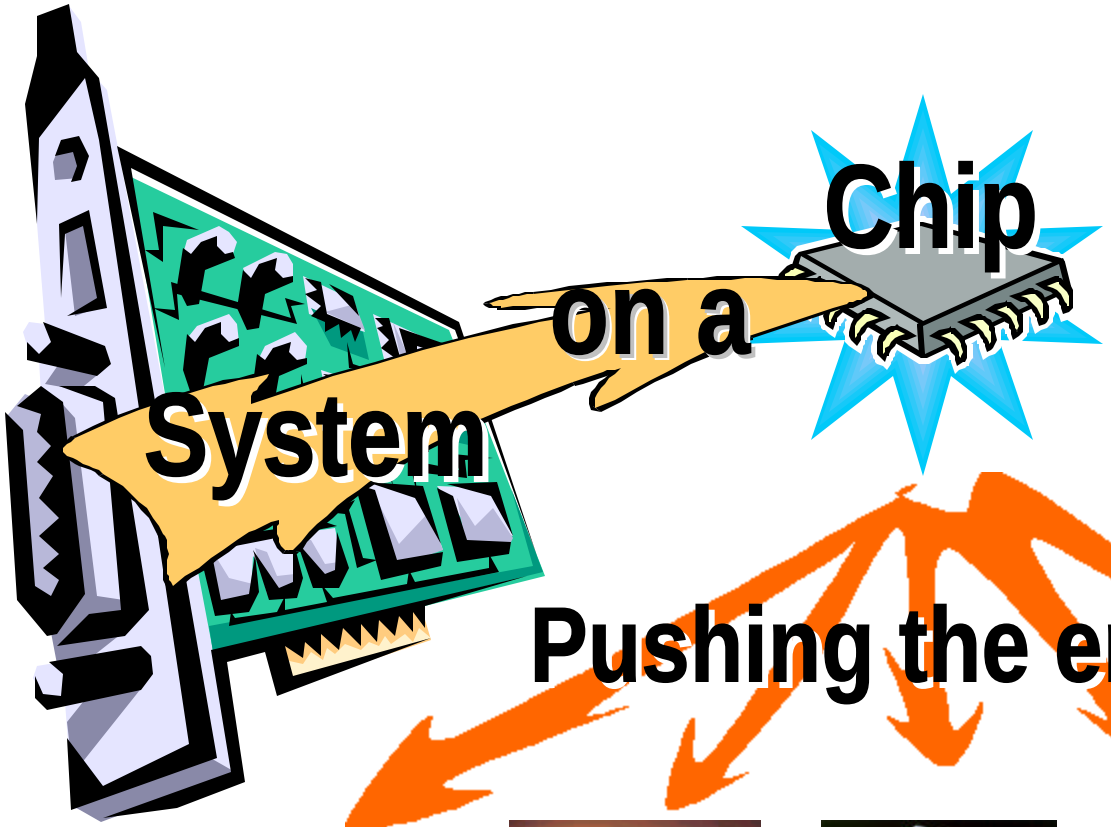
=

First Silicon Success

Summary

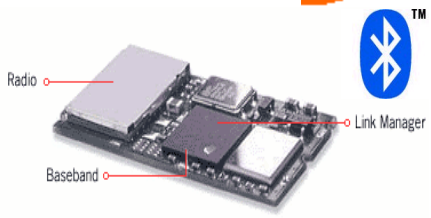
- **The future of electronics is System on a Chip (SoC)**
- **Design Lag + Design Gap = Economic Loss**
- **Bridging the Design Gap**
  - Design Methodology + Design Technology + Design Expertise
  - Drives business success and quality
- **High-end design is a driving force**
- **Innovative-EDA & high-end chip design are symbiotic**
- **Accelerating the SoC revolution**

The Future of Electronics is SoC

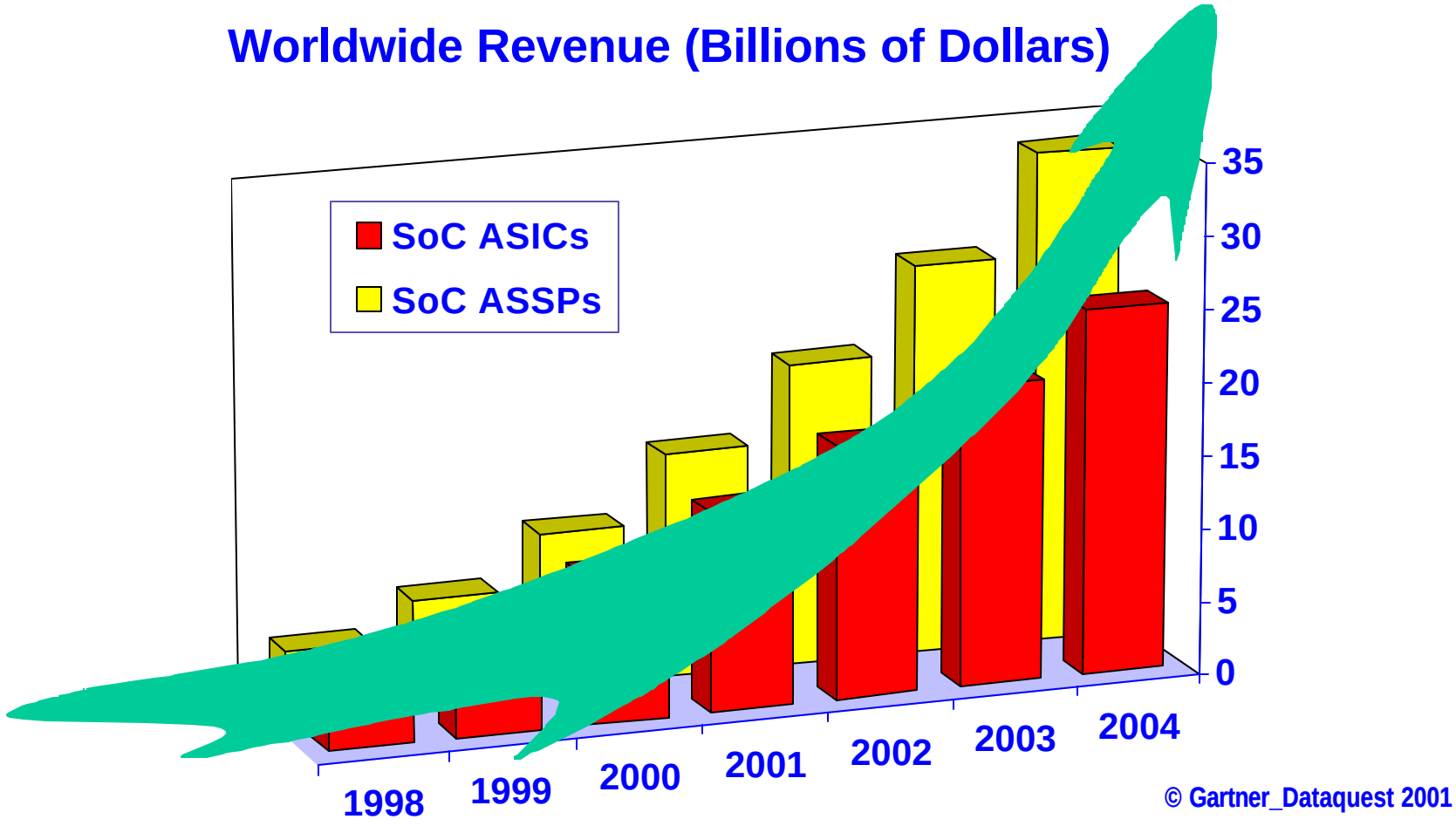


- Faster chips
- Smaller devices
- More functionality
- Broadband
- Wireless communications...

Pushing the envelope

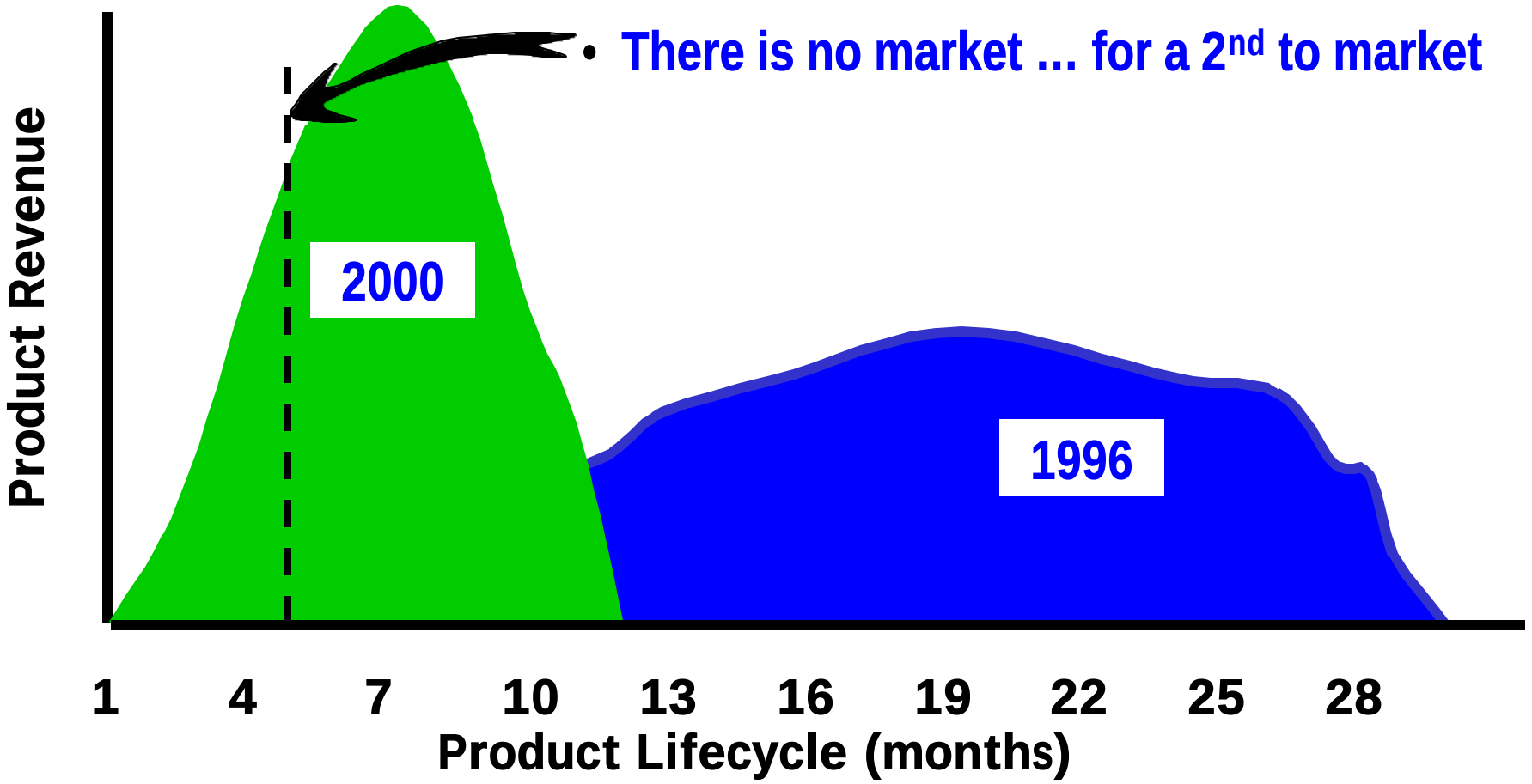


The SoC Market Is Hot



The SoC opportunity is $30B in 2001

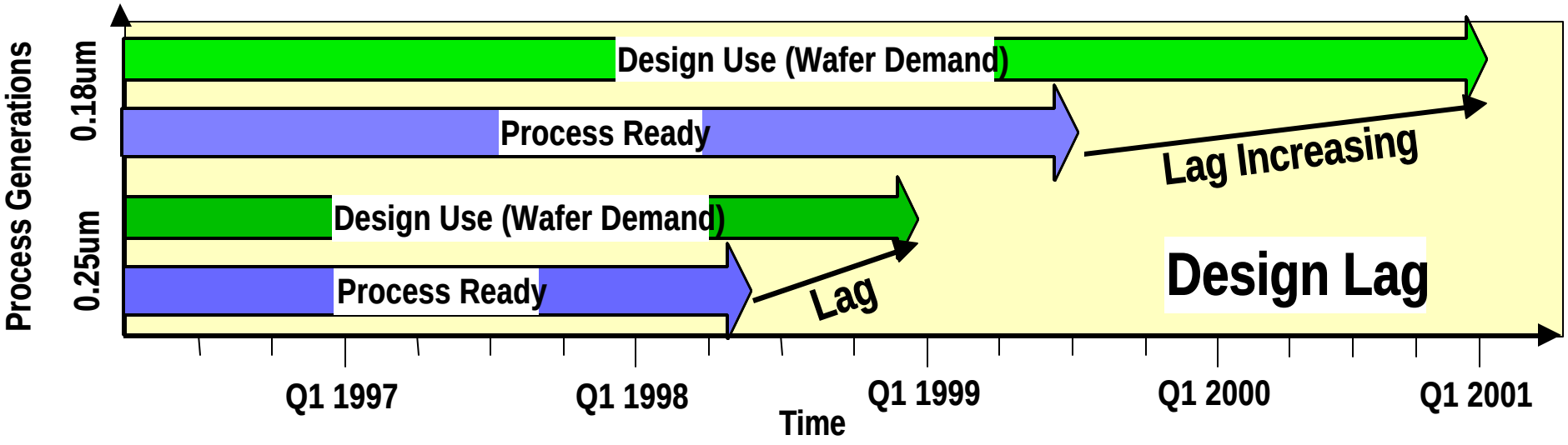
First-to-Market and First-to-Volume = Revenue



First-to-Market & Volume Þ Business Success

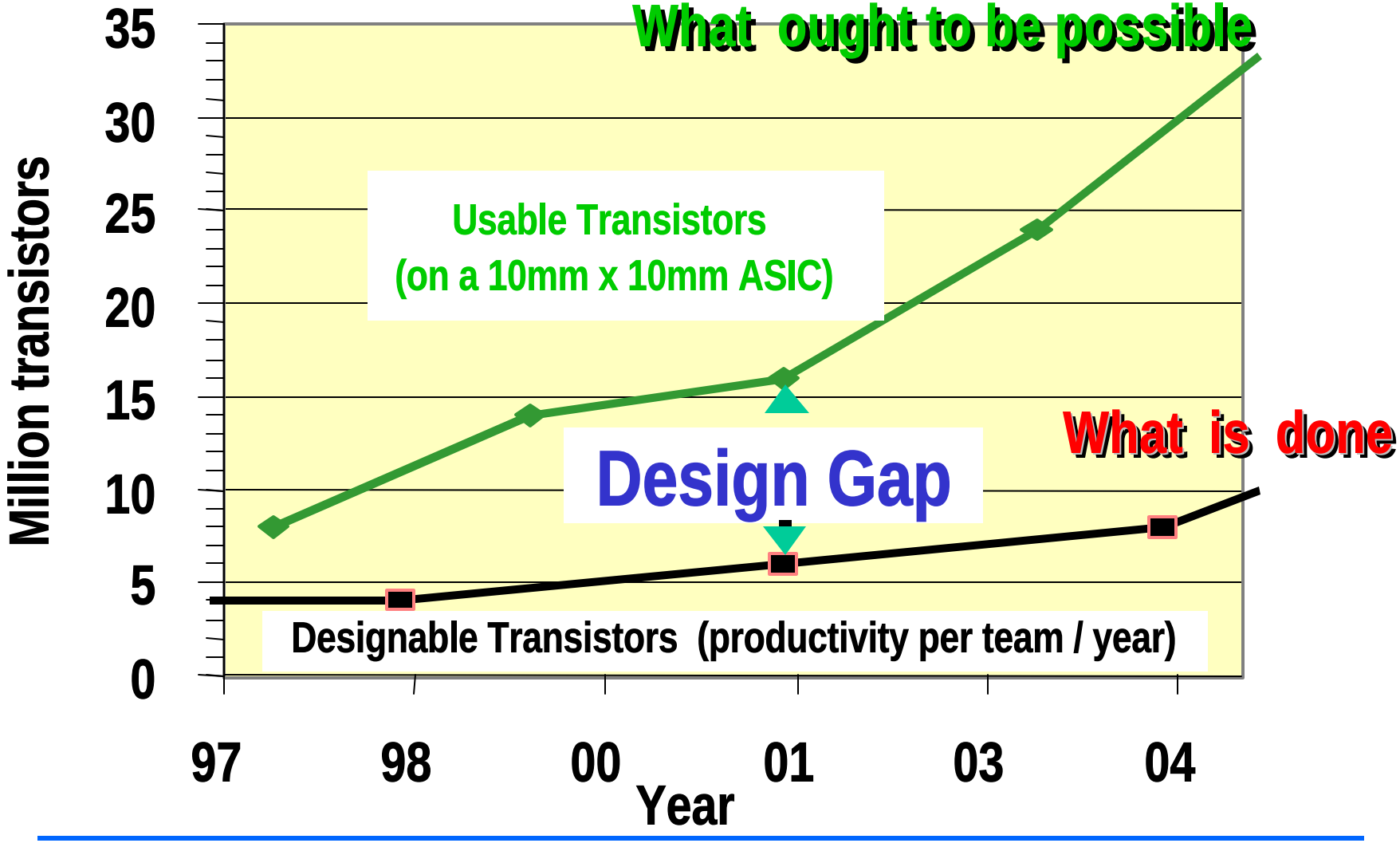
Design Lag = Economic Loss

- Design lag represents significant economic cost
  - Fab capacity under-utilization → many M$ / day depreciation
  - Higher product cost (carried in the entire product "food chain")



Increasing Lag with Advances in Technology

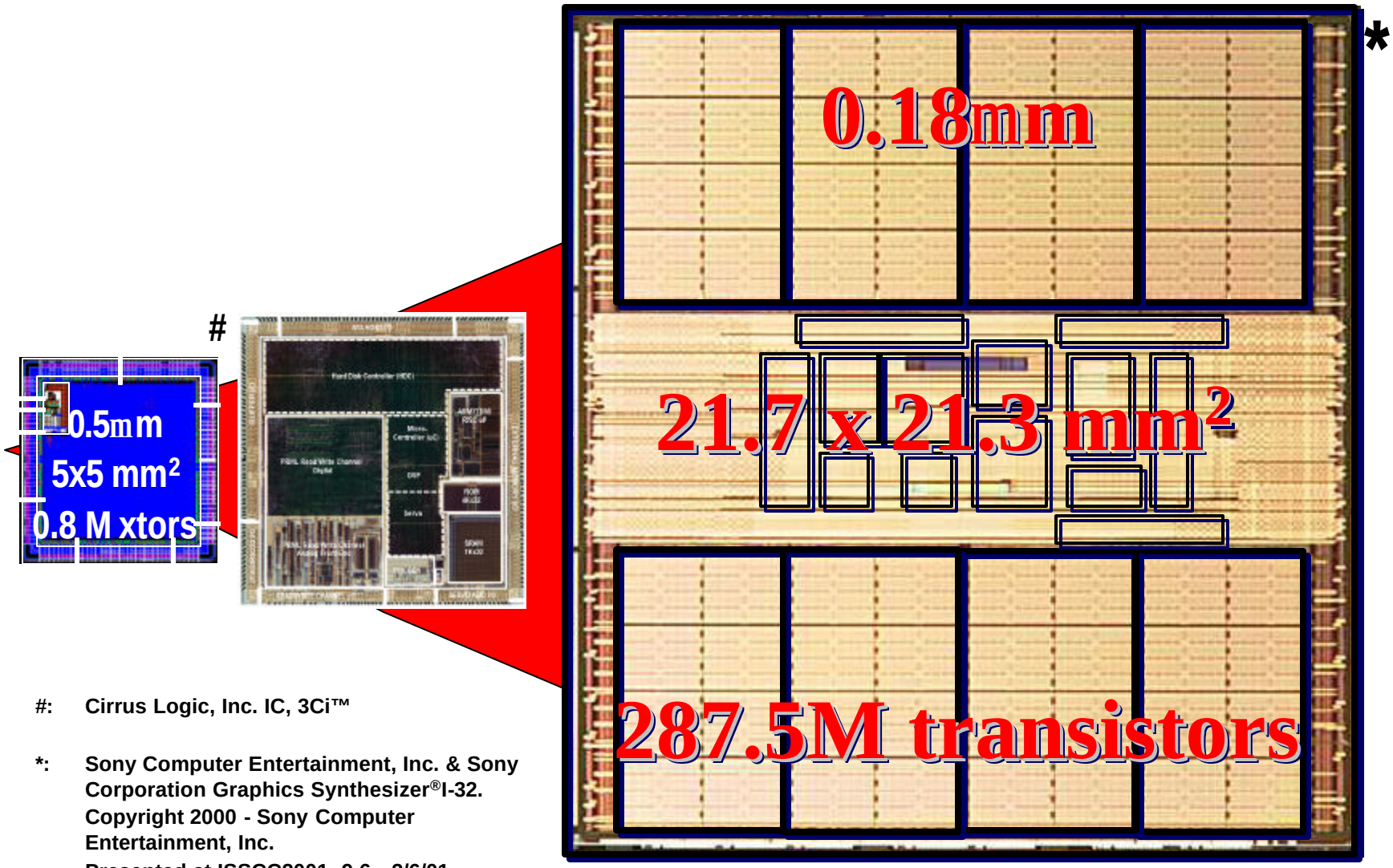
And Design Gap in Increasing



What are the Challenges?

- **Increasing design complexity**
  - IC complexity = ~58 % / year
  - Design productivity = ~21 % / year
- **DSM electrical design issues**
  - Timing closure, power, clocking, signal integrity
- **Program size & scale**
  - # development sites 1 → 5
  - # engineers (Platform) ~15 → ~70
- **IC Content**
  - Digital → Digital + analog

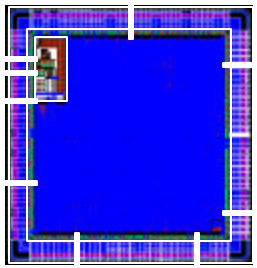
More System on a Chip



#: Cirrus Logic, Inc. IC, 3Ci™

*: Sony Computer Entertainment, Inc. & Sony Corporation Graphics Synthesizer®I-32. Copyright 2000 - Sony Computer Entertainment, Inc.
Presented at ISSCC2001; 9.6 - 2/6/01

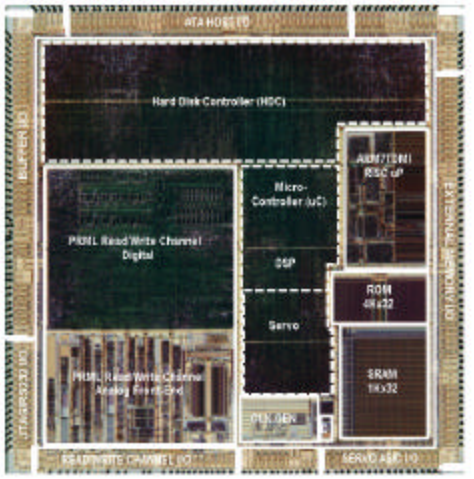
Cirrus Logic 0.5um - 0.35um VLSI ICs

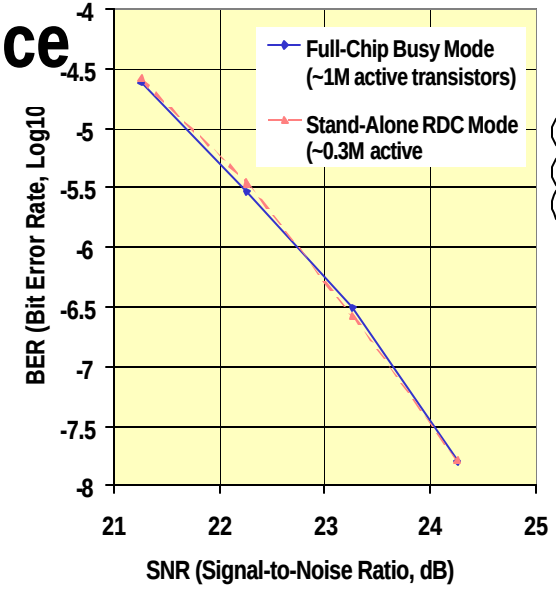


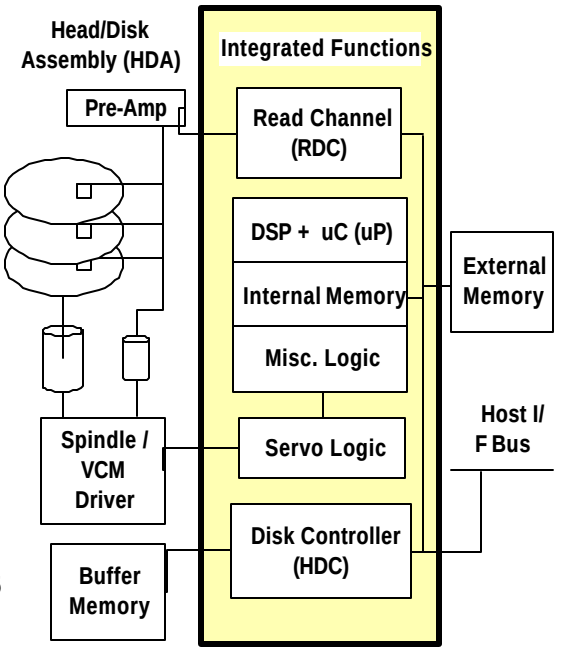
- **Design scale**
  - 66 – 100 MHz
  - ~35k nets
  - ~5 mm. x 5 mm.
- **Process**
  - 0.5 um– 0.35 um
  - 3 layer metal
- **Package**
  - 184 - 208QFPs
- **Program scale**
  - ~800K transistors
  - 1 development site
  - 5 - 15 engineers
  - 3 – 9 months
- **Design content**
  - Synthesized digital
  - Analog: Xtal, PLL, 1394, etc.
  - Asynchronous + static-timing-analyzable
- **~15 such designs**
- **First silicon success**

Cirrus Logic 3Ci™: 1st. SOC for MHDD electronics

- Mixed-signal SOC; 1.45M transistors
- ISSCC99: MP2.5
- 1998 EDN "Innovation of the Year"
- 1999 IDC "Top Ten"
- First silicon success
- VLSI → SOC: No degradation in analog performance







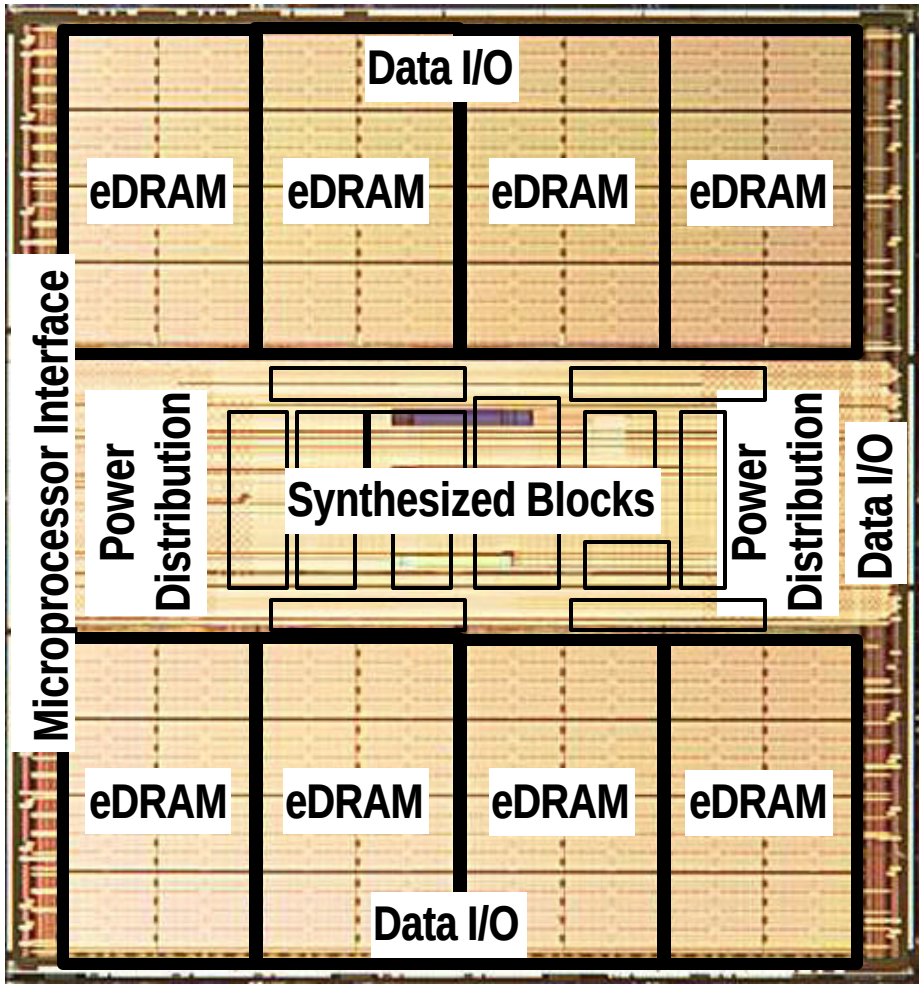
EDN INNOVATION '98 WINNER

3Ci™

CIRRUS LOGIC

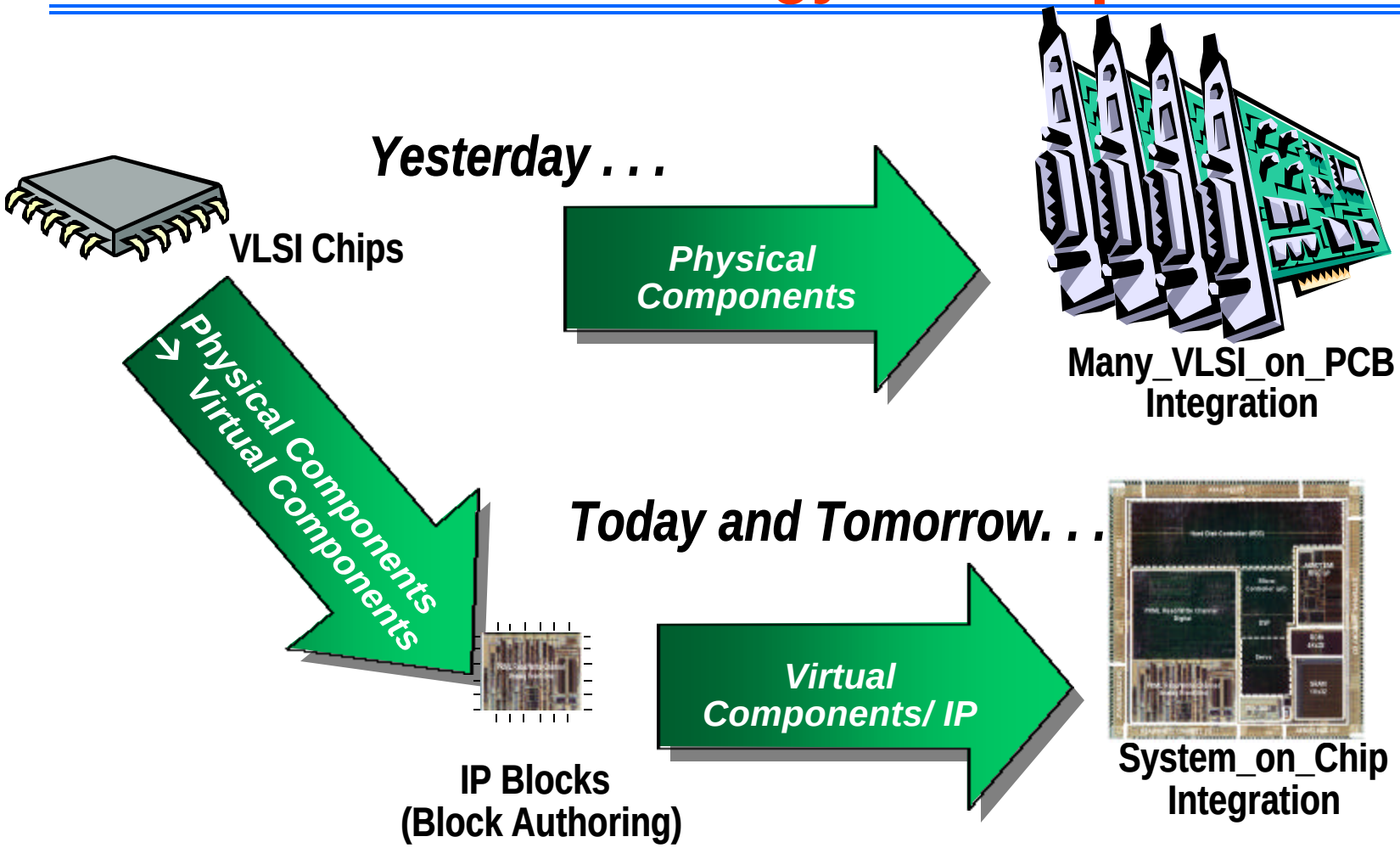
Sony Computer Entertainment: GS®I-32

- **Enhanced architecture: 8x higher eDRAM vs. PS®2 GS®**



- **Performance**
  - eDRAM Bandwidth = 48 GB/s
  - Buses >2K bits wide
  - Render 75M polygons/s
- **SOC integration**
  - 280M + 7.5M transistors
  - 21.7 x 21.3 mm^2
- **Scale**
  - >400K components
  - 11 blocks, 31K-218K gates
  - >68K flip-flops
  - >500K signal nets
  - >2K nets >10 mm. long
- **0.18 um, 6-metal CMOS**

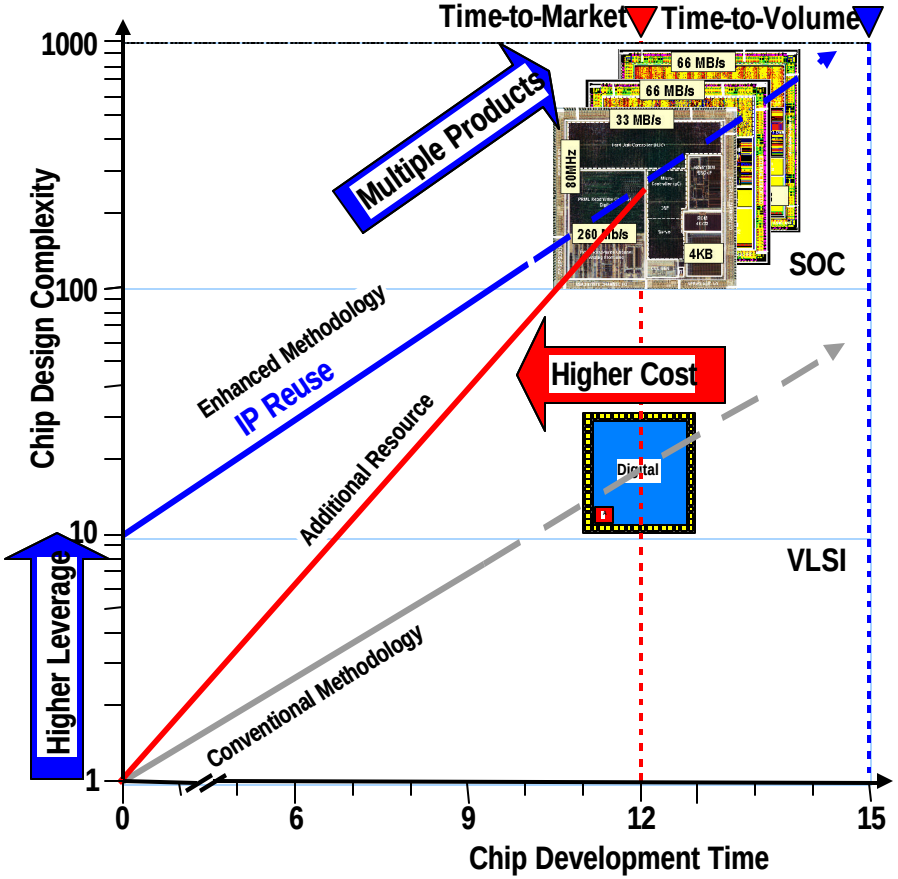
SoC Methodology is Complex



Need a fundamental enhancement to chip design methodology

System Design → SOC Design

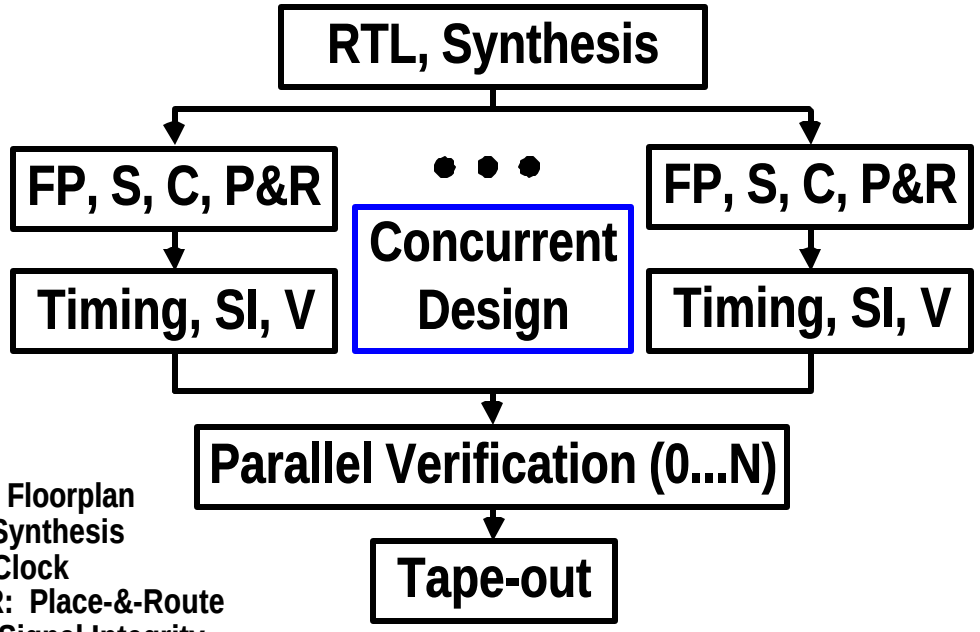
SOC Design = IP block creation + block integration



- **Enable concurrent engineering**
- **Reduce project complexity**
- **Simplify program management**
- **Leverage proven IP blocks**
  - Enhances quality
  - Enhance TTM and TTV
    - Reduce technical, schedule risks
- **Leverage platform infrastructure**
  - Verification, validation

Design Approach

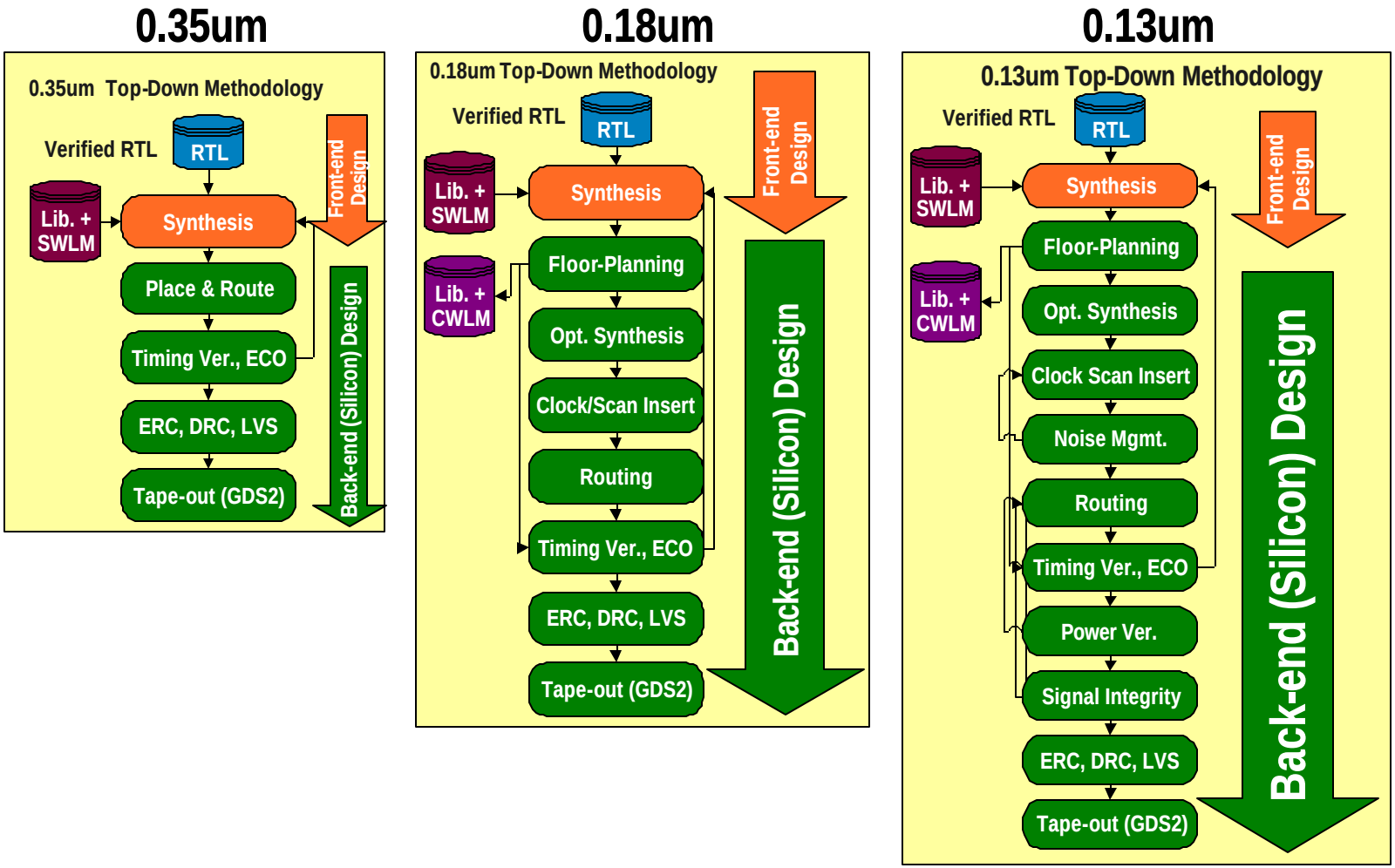
- **Hierarchical design**
  - Netlist to tape-out in 10 weeks
    - Includes I/O timing & SI, floorplanning, power distribution, clock circuit design, timing convergence, P&R, internal SI, ERC/DRC/LVS



FP: Floorplan
S: Synthesis
C: Clock
P&R: Place-&-Route
SI: Signal Integrity
V: ERC, DRC, LVS

- **Design challenges**
  - Power distribution
  - Clock architecture
  - Timing design
    - Load modeling
    - Delay calculation
  - Signal Integrity
    - Buffer insertion
    - Crosstalk

… DSM Design is Extremely Complex

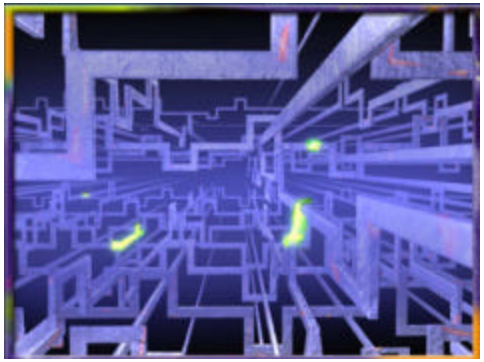


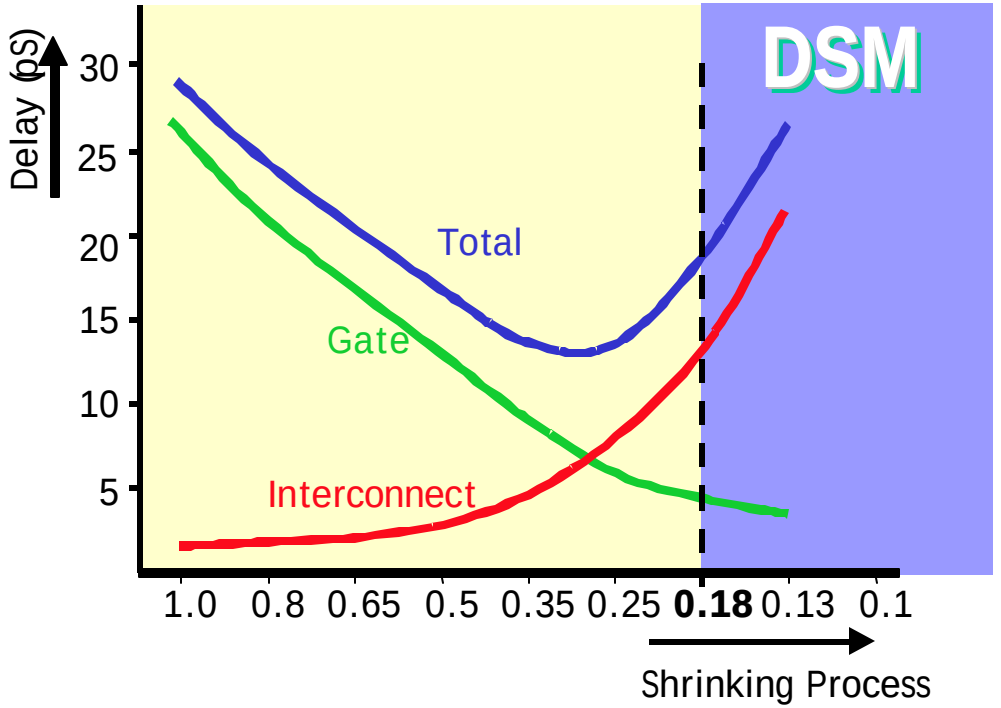
Requires Advanced Technologies and Methodologies

It's an Interconnect-Centric World ...

Above 0.18m

0.18m and Below

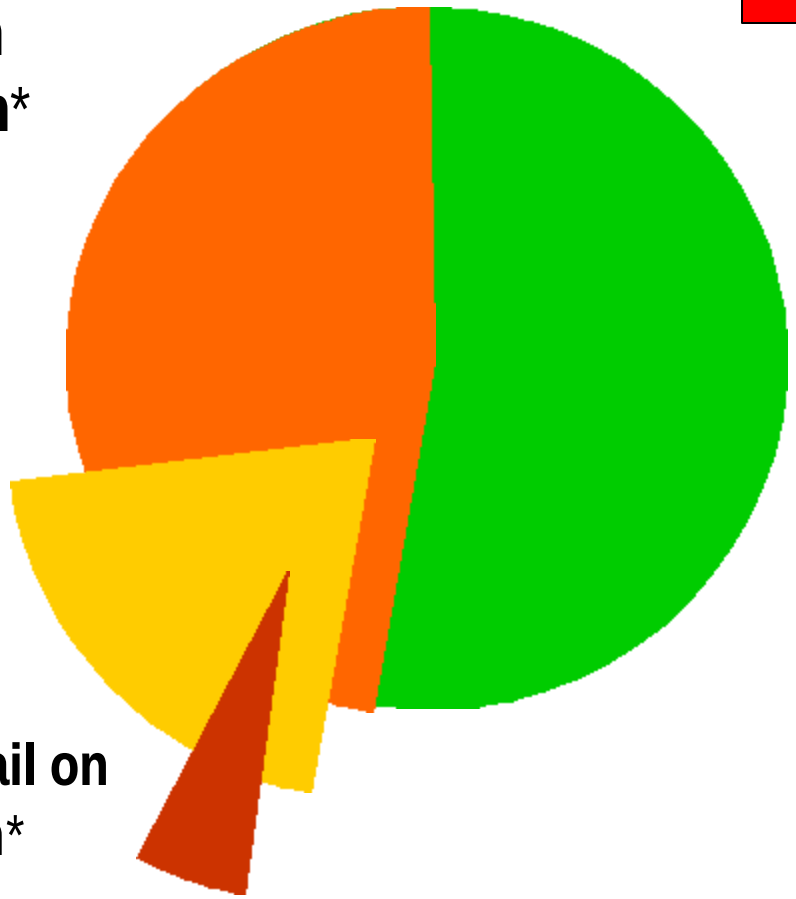




SoC Failures Cause Production Delays

One in Two Fails

48% fail on first silicon*



20% still fail on second spin*

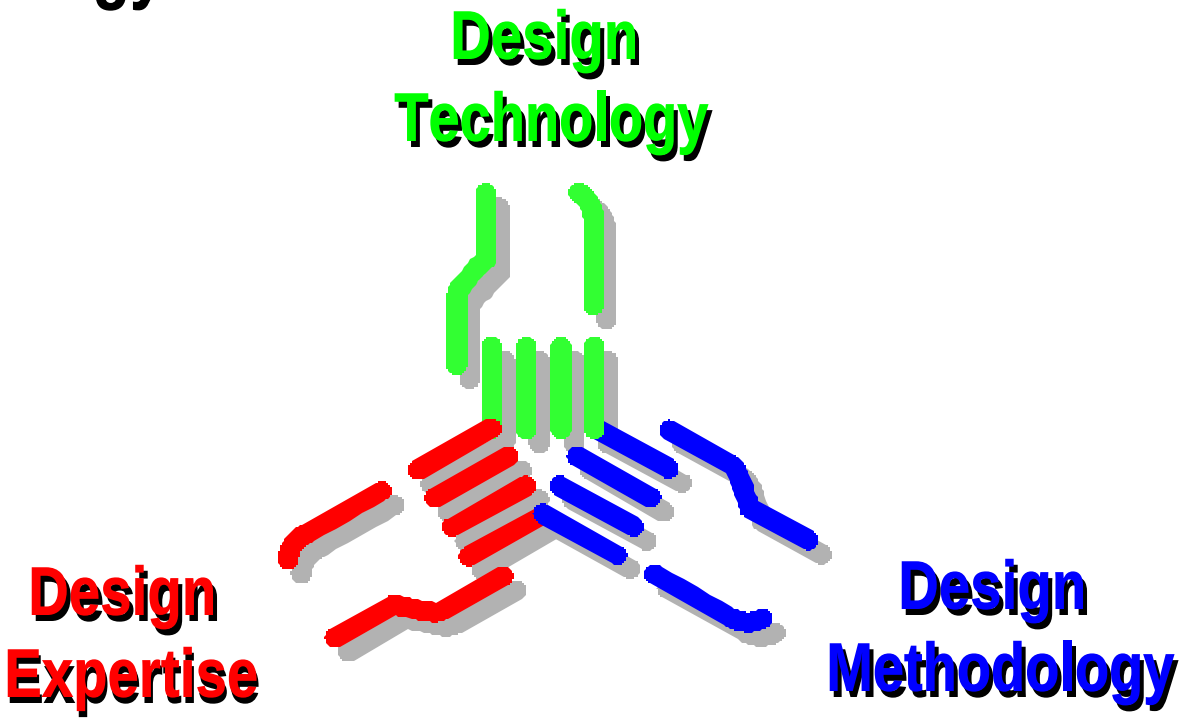
5% still fail on third spin*

- $500K manufacturing cost
- Up to $500 Million opportunity cost

*Source: Collet International - 2000

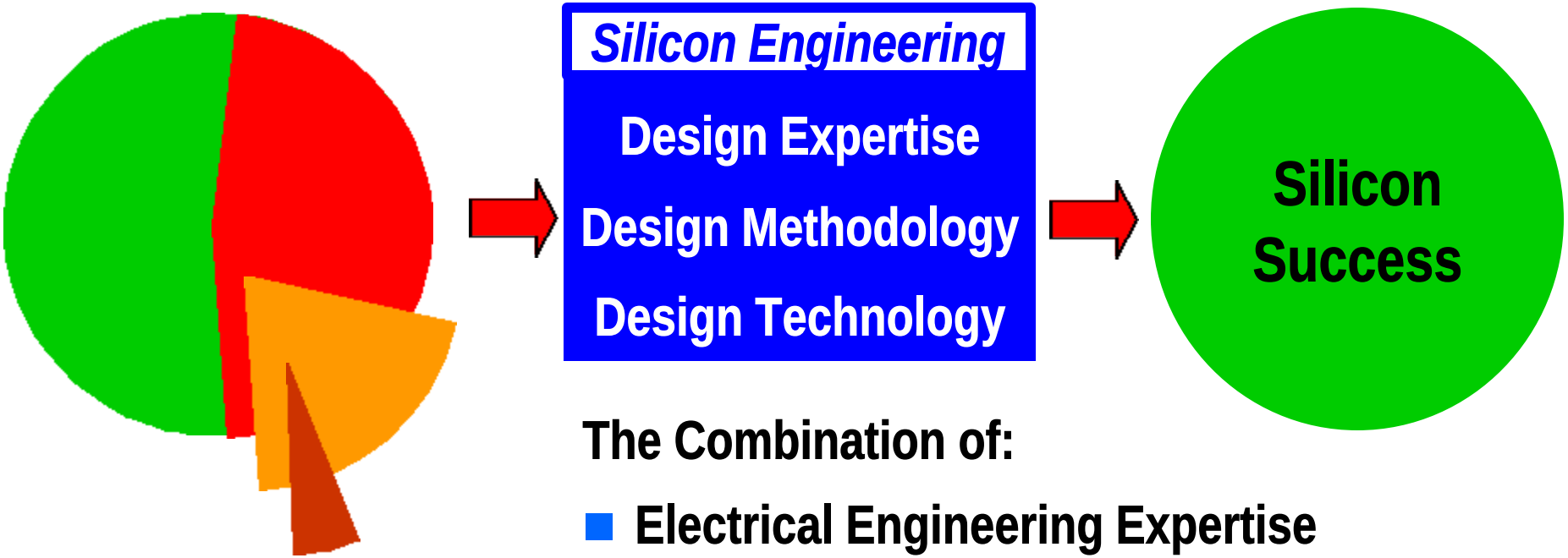
Bridging the Design Gap

- All of the most advanced chips in the world were created with a combination of design expertise, design methodology and innovative design technology



Expertise + Methodology + Technology

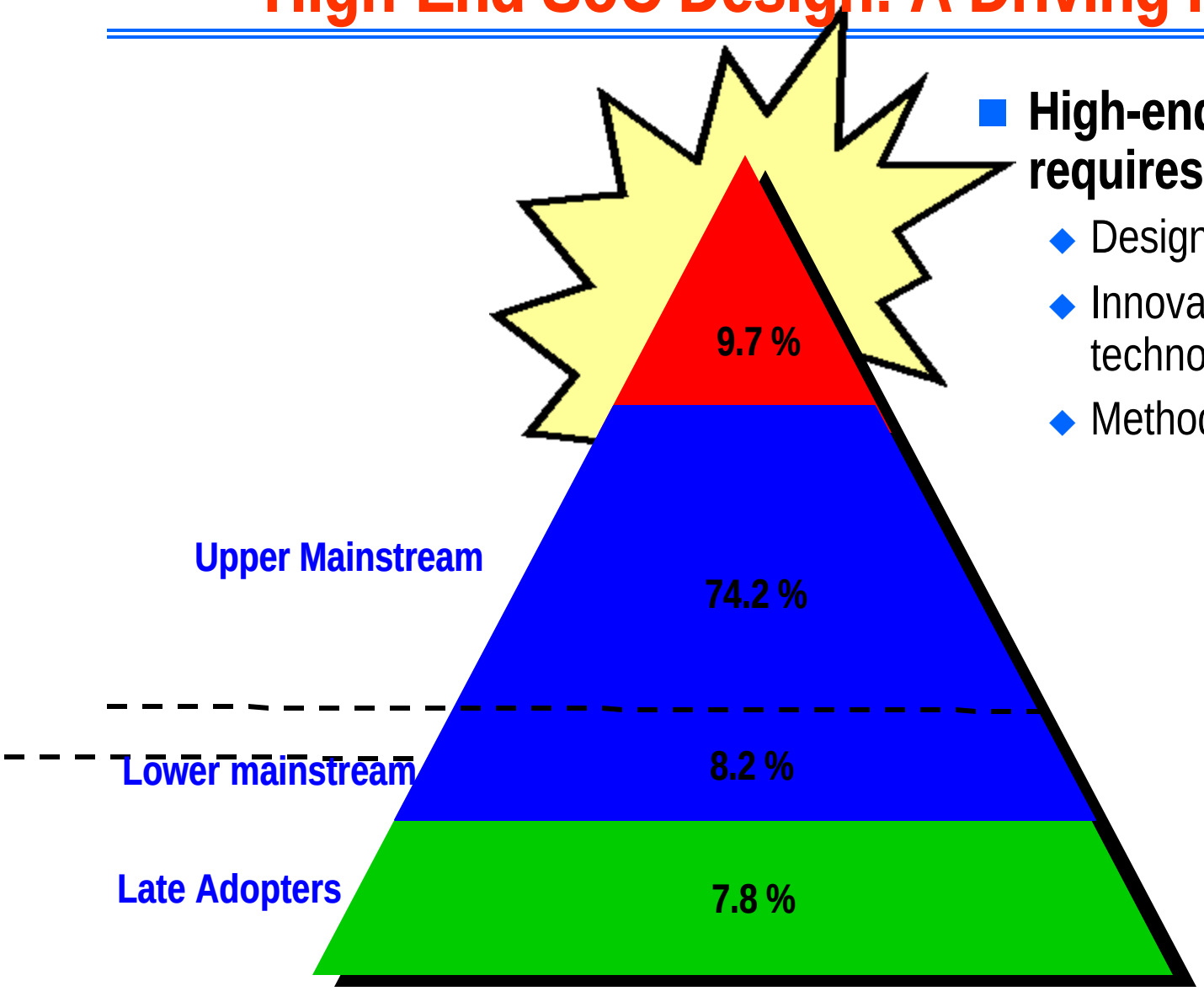
100% First-Time Silicon Success



The Combination of:

- **Electrical Engineering Expertise**
- **Scalable Methodology**
- **Innovative Design Technology**

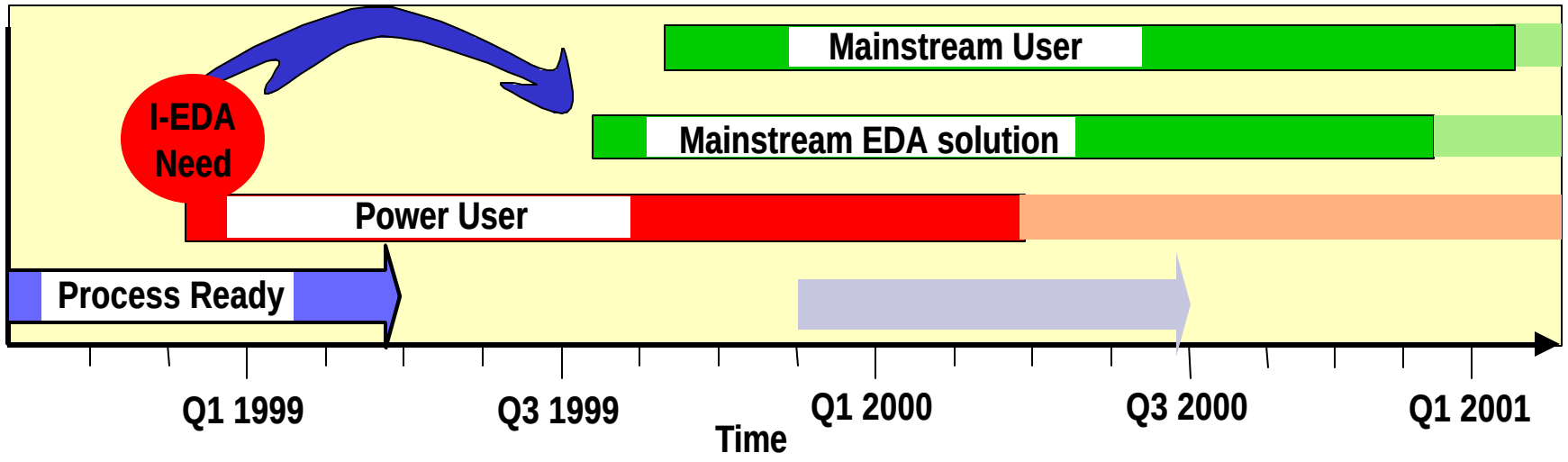
High-End SoC Design: A Driving Force



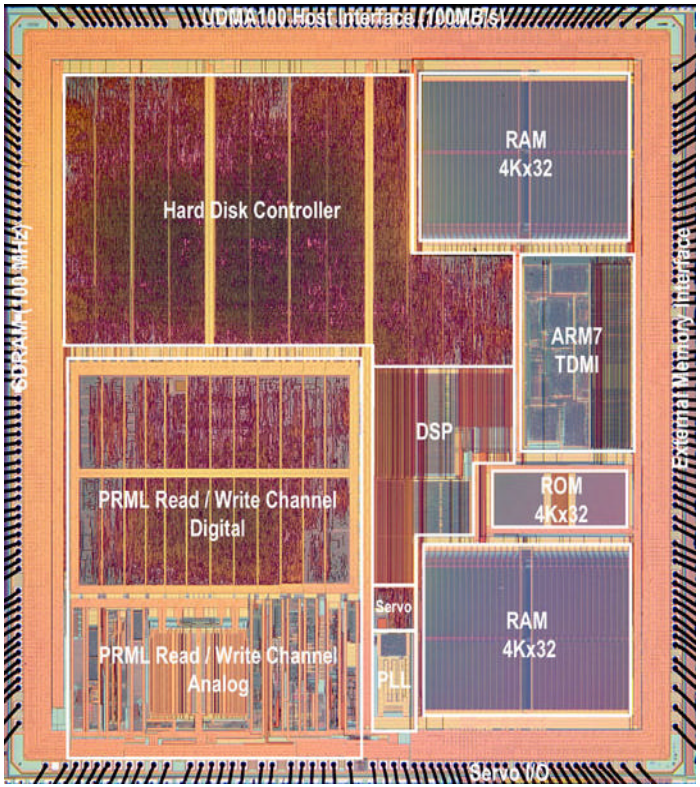
- **High-end SoC Design requires:**
  - Design expertise
  - Innovative design technology
  - Methodology expertise

Shortening the Innovation Cycles

- High-end design drives design technology, EDA evolution
- Combining chip design and innovative EDA provides focus
- Focus accelerates innovation
- Innovative-EDA & high-end chip design are symbiotic

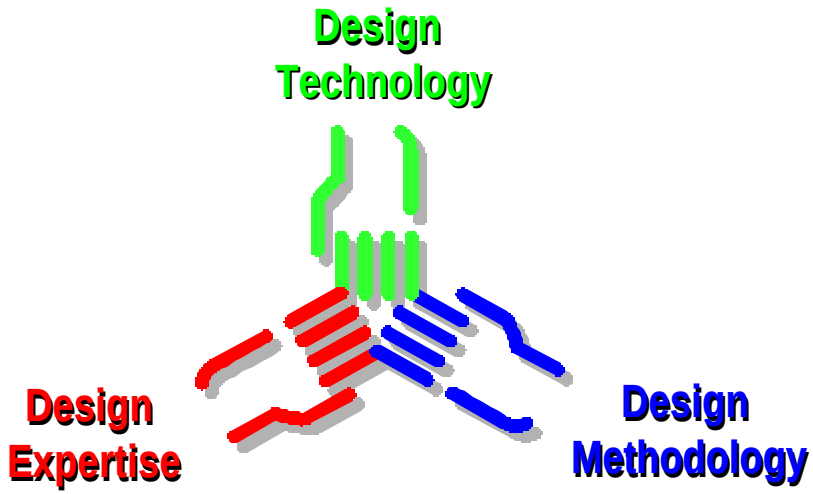


First-to-Market & Volume → Business Success



Cirrus Logic 3Ci™ 2.0
>500 MHz Mixed-Signal SOC

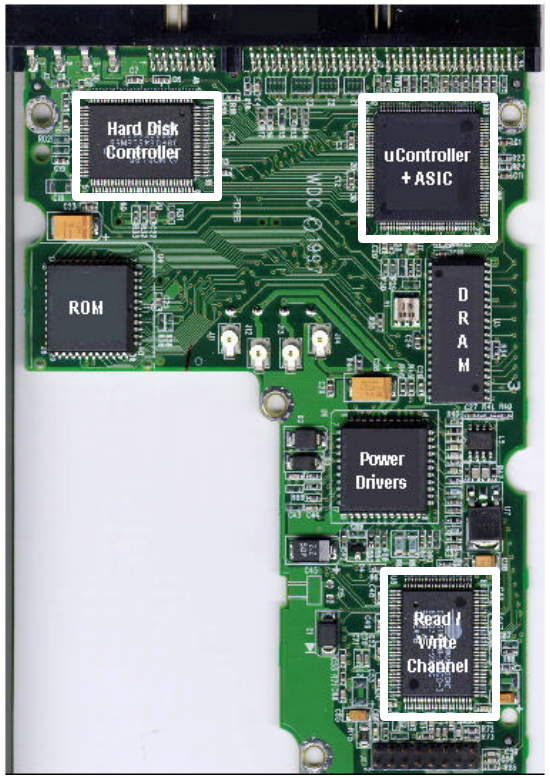
- Cirrus Logic 2nd Gen. 3Ci™
- First Silicon Success
- First to Market and Volume



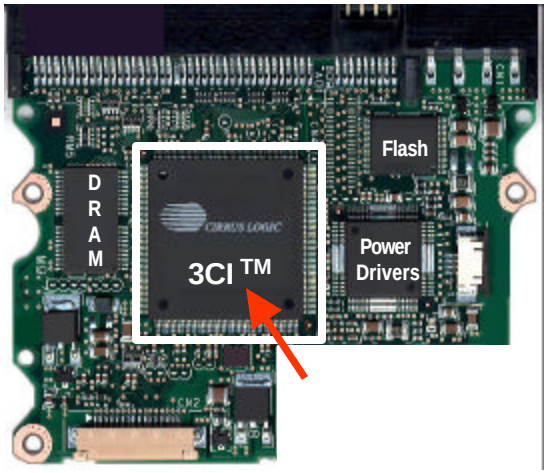
Cirrus Logic 3Ci™ - Impact on MHDD electronics

~1996

~1998

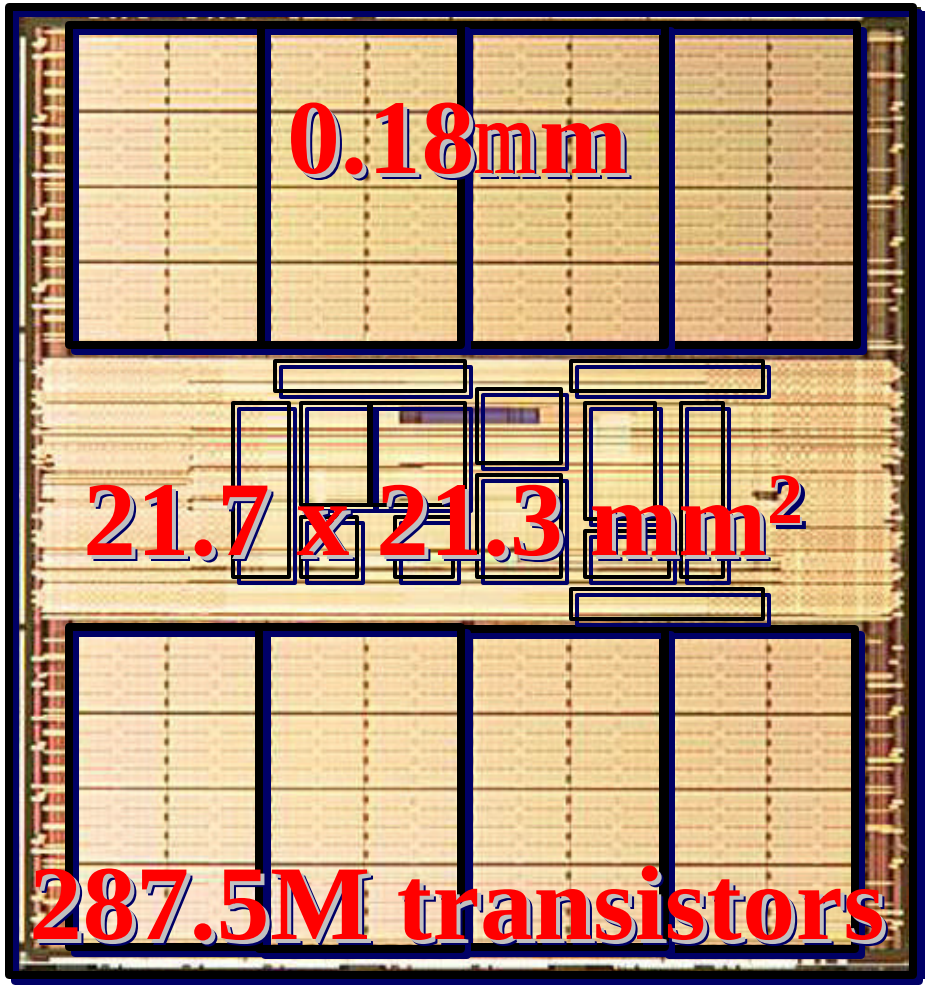


~1999

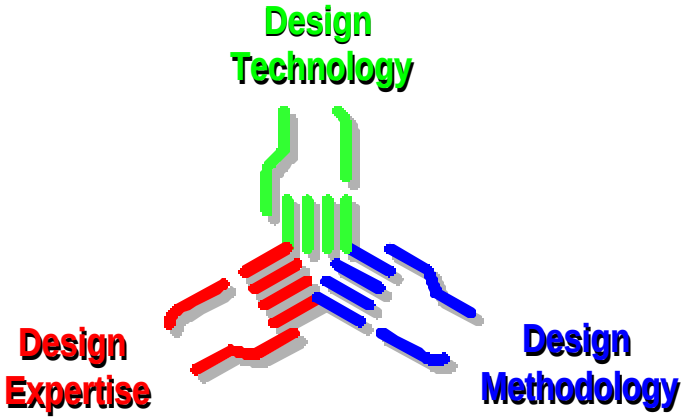


- Read/Write Channel (RDC)
- Micro-Controller (uC)
- Bus Controller
- Hard Disk Controller (HDC)
- Servo Assist

Sony Computer Entertainment: GS®I-32: Closing the Design Gap



- >280 M transistors
- 10 weeks
- First Silicon Success



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Presented at ISSCC2001; 9.6 - 2/6/01

Expertise + Methodology + Technology

- **Focus on silicon engineering**
- **IC design → design methodology, technology**
  - 0.35um: Mixed-signal integration, hierarchical design, CWLM, RC effects, “black-box” modeling
  - 0.25um: Signal integrity, transmission line effects
  - 0.18um: Fully-hierarchical timing convergence, nonlinear delay calculation technology, power distribution, signal integrity (crosstalk, buffer insertion, RC transmission lines)
- **0.15um – 0.13um work**
  - Technology validation, signal integrity, RLC, substrate, others

Rapid feedback and response between IC design and design technology → SOC design acceleration

For System on a Chip Designs:

Quality

=

First Silicon Success