PROGRAM

2002

2002
3rd International Symposium on

QUALITY ELECTRONIC DESIGN

MARCH 18, 19, 20, & 21, 2002

DoubleTree Hotel
San Jose, CA, USA

In cooperation with:

IEEE Computer Society (TTTC, Design Automation & VLSI TCs), IEEE Electron Device Society, ACM/SigDA, FSA

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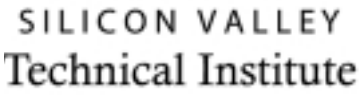
SILICON VALLEY
Technical Institute

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Ali Iranmanesh
Founder & Chair

On behalf of the ISQED 2002 conference and technical committees, we are pleased to welcome you to the 3rd International Symposium on Quality Electronic Design, ISQED 2002. The first two conferences held in 2000 and 2001 were extremely successful, and we expect this year to be even more successful. All the technical presentations, plenary sessions, panel discussions, tutorials, workshops, and other related events will take place on March 18-21 at the San Jose Double Tree Hotel. The hotel is located in the heart of Silicon Valley, near the San Jose International Airport, and is a very convenient location for all conference participants whether local, US or international attendees.

Tak Young
General Vice Chair

Over recent years we have witnessed extraordinary advances in semiconductor processing and manufacturing technologies giving rise to increasingly complicated designs. Due to these advances, we are in a situation of even greater dependencies between integrated circuit design, semiconductor technology development, manufacturing, and test. In addition, issues of modeling, verification, validation and characterization are taking on an increasingly important and critical role.

Furthermore, evolving business models making possible the availability of IP from a variety of sources and where questions of qualification, use/reuse, and integration exacerbate this complexity. This program will attempt to address these issues by bringing together industry practitioners and academics engaged in deep submicron integrated circuit design and development. The technical sessions will span the numerous disciplines that in total define the IC industry, including: design for process variation, power and noise management, and test, design tools and their interoperability, interconnect extraction and modeling, signal integrity, low power design issues, advanced device technology issues, and metrics to measure the quality of designs. This conference provides a unique opportunity to understand and discuss the key issues faced by industry in the next few years, highlight emerging areas of importance, and provide possible solutions to these challenges.

Res Saleh
Program Chair

The technical program for ISQED 2002 has been assembled by the technical program committee, which includes international experts from industry and academia. The technical program committee has selected papers for presentation from numerous excellent submissions.

This year, a total of 40 papers were accepted for oral presentation from 131 papers submitted to ISQED 2002. The technical program also includes 20 invited papers from leading experts in the field. Additionally, 21 papers were accepted for poster presentation. The ISQED 2002 Best Paper Award ceremony will be held prior to the lunch on Tuesday.

The conference will commence with our popular tutorial sessions, organized by Tuna Tarim, and will be held on Monday, March 18. There are four parallel tracks, with a total of 14 sessions, featuring experts from around the world. The tutorial sessions cover a variety of exciting and timely topics such as Test Methodologies for Quality Design, Design for Reliability in UDSM, Interconnect and Device Modeling, and Design Flows and Methodologies. Topics to be presented include platform-based SOC design, DFT for SOCs, IDDx testing, ESD protection methods, ultra-thin oxide, hot-carrier and electromigration reliability, device modeling, SOI circuit design, power/ground design, RLCK extraction and analysis, HDLs for mixed-signal and optimization in physical design flows. Tutorials at ISQED 2002 offer a truly outstanding opportunity to catchup with the latest areas of research and development.

Kaustav Banerjee
Technical Program Chair

In keeping with ISQED tradition, we are pleased to offer two plenary sessions, this year organized by Kris Verma, and Lech Jozwiak. The first plenary session is on Tuesday and the second one is on Wednesday, with 4 speakers in each session. The first keynote by John Chilton, Sr. VP and GM of Synopsys, will address the question "IP Reuse Quality: Intellectual Property or Intense Pain?" In the second keynote speech, David Lepejian, CEO of HPL will describe "Why Integrated Yield Management is a Necessity" in the area of LSI/SOCs in coming years. Next, Jim Kupec President of UMC (USA) will explore emerging business models in the semiconductor industry "Design Success: A Foundry Perspective." Finally a talk by Buno Pati, CEO of Numerical Technologies maintains "What you don't know CAN hurt you: Designing for Survival in a Subwavelength Environment." The second plenary session on Wednesday will start with the first keynote speech by Atiq Raza, CEO of Raza Foundries entitled "The Role of ICs in the creation of connected World and Importance of Product Quality." The second talk by Bob Brodersen of UC Berkeley will address the issues on "Wireless Systems-on-a-chip Design." Following that, Chan Shin Wu CEO of WIN Semiconductors will then discuss "Microwave III-V Semiconductors for Telecommunications and Prospective of the III-V Industry." Finally a paper by Ulf Schlichmann, Sr. Director of Infineon will address critical memory issues in his talk entitled "Tomorrows High Quality SoC Require high–density Embedded Memories Today."

Bharath Rajagopalan
Technical Program Vice Chair

The ISQED 2002 program also includes two evening panel sections on Monday and Tuesday evenings, organized by Gabriele Eckert. These panels will tackle two important issues in the industry: Tool Interoperability and Process Variation. The first panel on Monday night, organized by Pallab Chatterjee and moderated by Richard Goering, asks the question: "Are the interoperability

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standards for EDA too little/too late for real SOC designs?" The second evening panel on Tuesday night, organized by Siva Narendra and Vivek De, and moderated by Ron Wilson, poses the challenge "Process Variation: Is it too much to handle?" We invite you to attend and hear the opinions of the leaders in the field, and voice your opinion during the audience participation phase for these two controversial topics.

Following up from prior years, we continue to offer the Ph.D. student forum, which allows Ph.D. students to present and discuss their thesis work with experts in the IC industry. The forum organized by Kaushik Roy is in poster format and provides Ph.D. students, who are active in the research in the electronic design automation, and design-related areas, with the opportunity to gain visibility and get feedback on their work, and for the industry to gain insight into the academic work-in-progress.

Due to the overwhelming response to the call for papers, as well as the outstanding quality of the submissions, we will continue to include in this years program a special poster session on the afternoon of Wednesday, March 20, where the authors will summarize their research results on a poster format. Attendees of the poster session will be able to discuss issues directly with the authors and view the research results on the prepared posters. A new addition to ISQED event this year is a series of practical workshops on Thursday March 21st. The ISQED workshops are intended to supplement the conference by providing in depth, practical and proven design solutions for practicing design professionals. Workshops will be taught by experts in the field, who are intimately involved with the issues and solutions in their perspective areas, from both the industry and academia. We have organized three workshops in the following subjects: RF Integrated Circuit Design for Wireless Communications, Selection of Embedded Processor and Memory IPs, and Device and Interconnect Modeling for VDSM era.

In summary, we have assembled an excellent program for practicing engineers and managers in the IC industry, as well as academicians to learn the latest on quality electronic design so that functional integrated circuits, with expected performance, acceptable yield and reliability, can be designed and manufactured within the frame work of the desired cycle time. This conference provides a forum for you to learn and share and exchange insight and knowledge with your peers. We look forward to seeing you in March 2002.

Sincerely,

Ali Iramanesh
ISQED Founder & General Chair

Tak Young
ISQED General Vice Chair

Res Saleh
ISQED Program Chair

Kaustav Banerjee
ISQED Technical Program Chair

Bharath Rajagopalan
ISQED Technical Program Vice-Chair

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Professor, Electrical Engineering
University of Las Palmas, Spain

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Carnegie Mellon University

Edward Wan
Vice President
Worldwide Field Engineering,
UMC Group (USA), Sunnyvale, CA

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Design for Testability

George Alexiou, *Chair*
University of Patras/CTI, Greece

Jayashree Saxena, *Co-Chair*
Texas Instruments

Fadi Maamari
LogicVision

Marcel Jacomet
University A.S. Berne, Switzerland

Daniela De Venuto
Politecnico di Bari, Italy

Raimund Ubar
Tallinn Technical University, Estonia

Sreejit Chakravarty
Intel

Physical Design, Methodologies and Tools

Charlie Chung-Ping Chen, *Chair*
University of Wisconsin

Amit Narayan. *Co-Chair*
EDA Consultant

Marco Casale-Rossi
STMicroelectronics

Eileen You
Broadcom

Patrick Groeneveld
Magma Design

Li-Pen Yuan
Avant!

Jun-Dong Cho
SKKU

Rajeev Murgai
Fujitsu Laboratories

Khosrow Lashkari
NTT Docomo

Methodologies and Metrics for Design Quality

Andrew Kahng, *Chair*
University of California, San Diego

Jay Michlin, *Co-Chair*
EDA Consultant

Tak Young
Monterey Design

David Overhauser
Simplex

Sani Nassif
IBM

Justin Harlow
SRC

Don Cottrell
S12

Design and Abstraction Methods for SoCs, IP Blocks and Libraries

Miodrag Potkonjac, *Chair*
University of California, Los Angeles

Michael Reinhardt, *Co-Chair*
RubiCAD

Antonio Nunez
Univ. of Las Palmas, Spain

Vamsi Srikantam
Agilent

Kris Verma
Seagate

Jeanne Mechler
IBM

James Lei
Cirrus Logic

Low Power Design and Test

Massoud Pedram, *Chair*
University of Southern California

Vivek De, *Co-Chair*
Intel

Kaushik Roy
Purdue University

Norman Chang
Apache Solutions

Lei He
University of Wisconsin

Michael Zelikson
IBM

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EDA Tools, Interoperability and Implications

Lech Jozwiak, *Chair*
Eindhoven University
The Netherlands

Steven Start, *Co-Chair*
American Microsystems Inc.

Tom Chen
Hewlett Packard/CSU

Adam Postula
University of Queensland, Australia

Charlie Huang
Cadmos

Wolfgang Rosentiel
FZI Forschungszentrum Informatik,

Mely Chen
CYC University, Taiwan

Frank Lee
Avant!

Olivier Sentieys
Enssat

Krzysztof Kuchcinski
Lund Institute of Technology, Sweden

Device, Interconnect and Circuit Level Modeling and Analysis

Amit Mehrotra, *Chair*
University of Illinois, Urbana

Rajendran Panda, *Co-Chair*
Motorola

Ram Krishnamurthy
Intel

David Goren
IBM

Keith Green
Texas Instruments

Dennis Sylvester
University of Michigan

Narain Arora
Simplex

Ibrahim Hajj
American Univ. of Beirut

Olof Tornblad
Ericsson

Daniel Foty
Gilgamesh

Junjiang Lei
Numerical Technologies

Design for Manufacturability / Package-Design Interactions and Co-Design

Lukas van Ginneken, *Chair*
Magma Design

Pranav Ashar, *Co-Chair*
NEC Laboratories

Aswin Mehta
Texas Instruments

Jeong-Taek Kong
Samsung, Korea

Vinod Malhotra
Numeritech

Madhavan Swaminathan
Georgia Institute of Technology

Tuna Tarim
Texas Instruments

Enrico Malavasi
PDF Solutions

Frank Marazita
ATI

Effects of Technology on IC Design, Performance, Reliability, and Yield

Ken Shepard, *Chair*
Columbia University

Ajith Amerasekera, *Co-Chair*
Texas Instruments

Steve Voldman
IBM

Farid Najm
University of Toronto, Canada

Siva Narendra
Intel

Chune-Sin Yeh
Celestry

Adrian Ionescu
EPFL, Switzerland

Saila Ponnapalli
Cadence

Hirokazu Yonezawa
Matsushita, Japan

Shiro Kamohara
Hitachi, Japan

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ISQED 2002 GENERAL INFORMATION

March 18-21, 2002

DoubleTree Hotel
2050 Gateway Place
Tel: 1-408-453-4000
Fax: 1-408-437-2898

TUTORIALS

Monday, March 18, 8:30am–5:15pm
Features four Parallel Tracks with 14 tutorials. Includes lunch and coffee breaks.

PLENARY SESSIONS

Sponsored by Tavanza Inc.

Plenary Session I:
Tuesday, March 19, 8:30am–11:50am
Features keynote speeches by **John Chilton** (Sr. VP/GM, Synopsys), **David Lepejian** (President/CEO HPL), **Jim Kupec** (President, UMC USA), **Buno Pati** (President/CEO Numerical Technologies).

Plenary Session II:
Wednesday, March 20, 8:30am–11:50am
Features keynote speeches by **Atiq Raza** (Chairman/CEO, Raza Foundries), **Bob Brodersen** (Professor, UC Berkeley), **Chan Shin Wu** (President/CEO WIN Semiconductors), **Ulf Schlichtmann** (Sr. Director, Infineon Technologies AG).

BEST PAPER AWARDS

Sponsored by TSMC

The ISQED 2002 Best Paper Award ceremony will be held prior to the ISQED luncheon on Tuesday.

PANEL DISCUSSIONS

Evening Panel Discussion EP1
Monday March 18, 6:30pm–8:30pm

Are the interoperability standards for EDA too little/ too late for real SOC designs?

Moderator:
Richard Goering
Managing Editor Design Automation, EETimes.

Evening Panel Discussion EP2:
Sponsored by Numerical Technologies

Tuesday March 19, 6:30pm-8:30pm

Process Variation: Is it too much to handle?

Moderator:
Ron Wilson
Editor in Chief, ISD magazine

TECHNICAL SESSIONS

There are 12 technical sessions, featuring 40 papers accepted for oral presentation from 131 papers submitted to ISQED 2002. The program also includes 20 invited papers from leading experts in the field, and 21 papers accepted for poster presentation.

PH.D. STUDENT FORUM

Ph.D. student's posters will be on display on 12:30pm–2:00pm on Tuesday, March 19. Student authors will be available to discuss their work and to answer questions.

POSTER SESSION

Poster papers will be on display on 12:30pm–3:30pm on Wednesday, March 20. Authors will be available to discuss their work and to answer questions.

WORKSHOPS

Thursday, March 21, 8:30am - 5:30pm. ISQED has added three interactive workshops for those who desire in-depth, interactive, and focused insight into the various aspects of electronic design. These workshops are as follows:

- RF IC Design For Wireless Communications
- Selection of Embedded Processor And Memory IPs
- Device And Interconnect Modeling For VDSM Era

REGISTRATION INFORMATION

ADVANCE REGISTRATION
For advanced registration, using the on-line registration process, visit the ISQED web site at http://www.isqed.org.

To qualify for the discounted advance registration rate, all the registrations must be carried out on-line prior to March 10th, or if done by mail, postmarked before March 10th, 2002. After March 10th, you can register on site. Please note that the tutorial registration is only available to the conference attendees. Workshop registration is available without restrictions.

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ON-SITE REGISTRATION

Due to limited space, you are encouraged to register in advance. Nevertheless, the on-site conference registration is available at the DoubleTree hotel as follows:

TUTORIAL REGISTRATION

Sunday, March 17, 2002	*5:00pm-8:00pm*
Monday, March 18, 2002	*8:00am-5:00pm*

TECHNICAL SESSIONS & WORKSHOPS REGISTRATION

Sunday, March 17, 2002	*5:00pm-8:00pm*
Monday, March 18, 2002	*8:00am-5:00pm*
Tuesday March 19, 2002	*8:00am-5:00pm*
Wednesday March 20, 2002	*8:00am-12:00pm*
Thursday March 21, 2002	*8:00am-12:00am*

HOTEL REGISTRATION

A block of rooms has been reserved at the DoubleTree Hotel for ISQED participants. To make reservations please complete the hotel reservation form, attached in the centerfold of this booklet and send the form directly to the DoubleTree hotel, by fax or mail. The special rate will apply to all the registrations made before or on March 3, 2002 before 5pm. Please refer to the hotel registration form for details. It is recommended to make your reservation as soon as possible since the hotel rooms are limited. Please immediately report any problem with the hotel and/or conference registration to:

Conference Manager
Melissa Widerkehr
Tel: (301) 527-0900 Ext. 101, Fax: (301) 527-0994
Email: widerkehr@isqed.org

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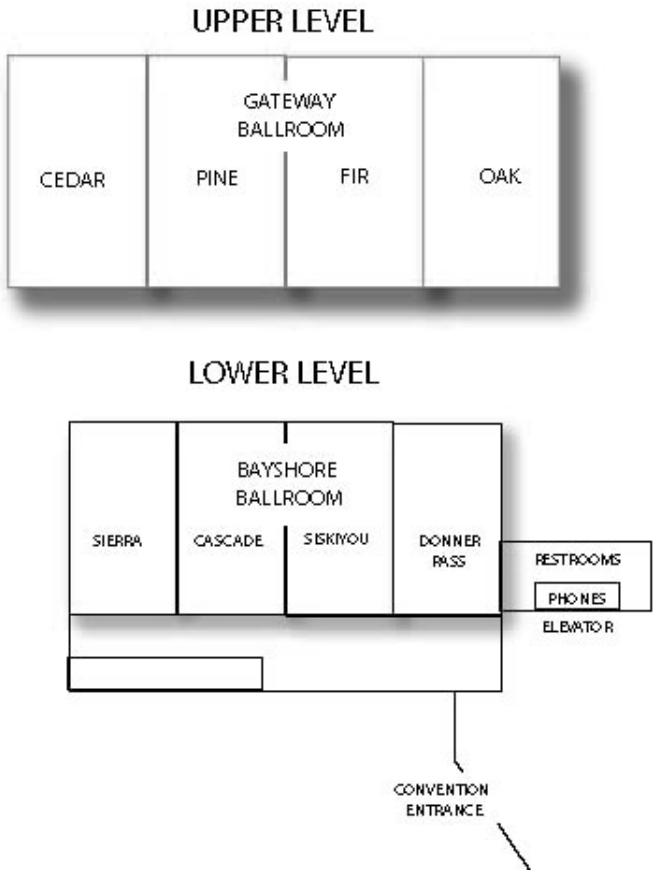

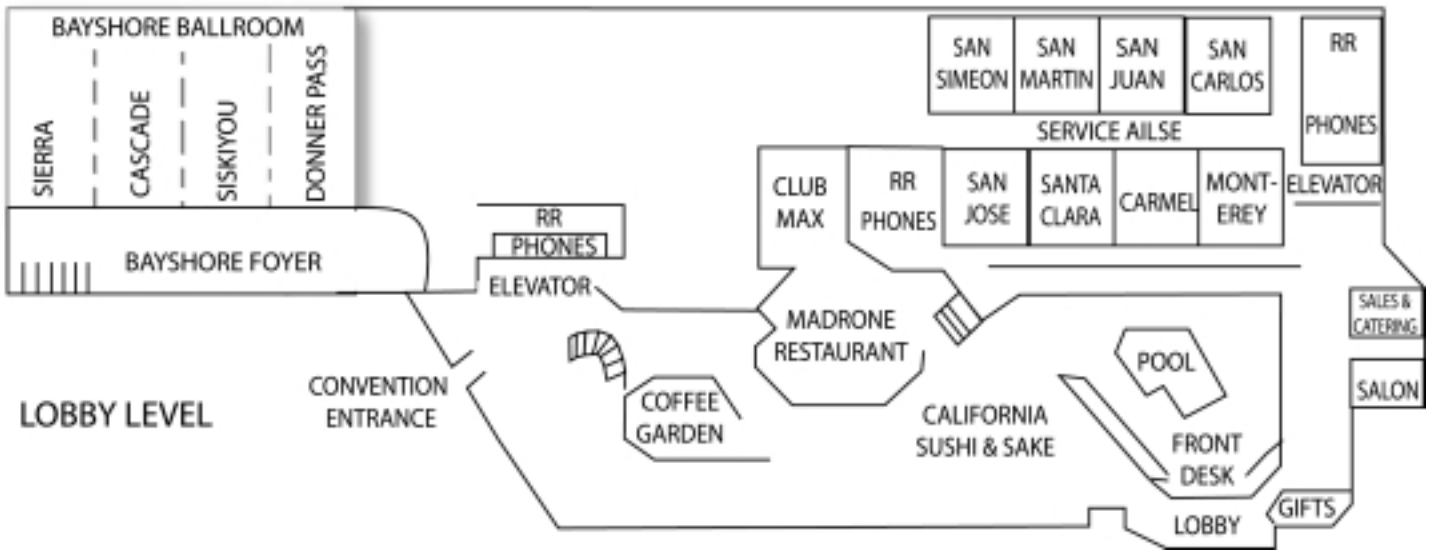

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IEEE ISQED 2002
Program at a glance

Date	Time	Room 1	Room 2	Room 3	Room 4
Monday 3/18/02	8:30 am-5:15 pm	**Tutorial Track A** Test Methodologies for Quality Designs *Room: Monterey*	**Tutorial Track B** Design for Reliability in UDSM: Issues and Solutions *Room: Carmel*	**Tutorial Track C** Interconnect and Device Modeling for Quality Design *Room: Santa Clara*	**Tutorial Track D** Design Flows and Methodologies *Room: San Jose*
	6:30 pm-8:30 pm	**Evening Panel Discussion EP1 and Dinner** **Are the Interoperability Standards for EDA too little/too late for Real SOC Designs?** *Room: Cascade/Sierra*			
Tuesday 3/19/02	8:30 am-12:00 pm	**Plenary Session I** Keynote speeches by: **John Chilton, David Lepejian,Jim Kupec, Buno Pati** Followed by **ISQED Best Paper Awards** *Room: Donner/Siskiyou*			
	12:00 pm-1:00 pm	**ISQED Luncheon** *Room: Sierra*			
	1:00-3:10 pm	**Session 1A** Interconnect Extraction and Modeling *Room: Donner*	**Session 1B** Quality and Interoperability of EDA Tools *Room: Siskiyou*	**Session 1C** Design for Test *Room: Oak*	**PhD Student Forum** (poster session) 12:30-3:30 *Room: Bayshore Foyer*
	3:10 pm-3:30 pm	**Break**			
	3:30 pm-5:40 pm	**Session 2A** Design for Process Variations *Room: Donner*	**Session 2B** Power, Signal, and EMI Analysis and Optimization *Room: Siskiyou*	**Session 2C** Methods and Metrics for Design Quality *Room: Oak*	**Speakers Practice** *Room: Riesling*
	6:30 pm-8:30 pm	**Evening Panel Discussion EP2** **Process Variation: Is it too much to handle?** *Room: Cascade/Sierra*			
Wednesday 3/20/02	8:30 am-11:50 am	**Plenary Session II** Keynote Speeches by: **Atiq Raza, Bob Broderson, Chan Shin Wu, Ulf Schlichtman** *Room: Donner/Siskiyou*			
	12:00 pm-1:00 pm	**Lunch Break**			
	1:00 pm-3:10 pm	**Session 3A** Design Issues for Power and Noise Management *Room: Donner*	**Session 3B** Verification in Achieving Design Quality *Room: Siskiyou*	**Session 3C** Signal Integrity *Room: Oak*	**Poster Session** 12:30-3:30 *Room: Bayshore Foyer*
	3:10 pm-3:30 pm	**Break**			
	3:30 pm-5:15 pm	**Session 4A** Low Power Design Techniques *Room: Donner*	**Session 4B** Advanced Device Technology Issues in Circuit Design *Room: Siskiyou*	**Session 4C** Design, Planning, and Closure *Room: Oak*	**Speaker Practice** *Room: Riesling*
Thursday 3/21/02	8:30 am-5:15 pm	**Workshop I** RF IC Design for Wireless Communication *Room: San Jose*	**Workshop II** 1st Workshop on Selecting Embedded Processor & Memory IPs *Room: Santa Clara*	**Workshop III** Device and Interconnect Modeling for VDSM Era *Room: Carmel*	

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Tutorial Track A

Test Methodologies for Quality Designs*

Monterey Room

Chair & Moderator: Yervant Zorian, LogicVision

8:30am-12:15pm
Tutorial A.1:

Design-for-Test Techniques for SoC Designs

Organizer: Janusz Rajski, Mentor Graphics Corporation
Presenter1: Janusz Rajski, Mentor Graphics Corporation
Presenter2: Geir Eide, Teseda Corporation

This tutorial aims to jump start the designer to new levels of practical test expertise by presenting DFT methodologies, solutions, and technological advancements for addressing today's toughest DFT issues. The tutorial briefly introduces basic DFT concepts and techniques, and focuses on practical issues such as: IP core design guidelines that enable test reuse, DFT for complex SoC designs, embedded memory test, at-speed test, and DFT integration into the design flow. The tutorial presents in detail structural Design-for-Test methodologies based on scan, i.e. scan cell design, scan operation, scan chain optimization, multiple clock domains, test logic, test points, basic concepts of Logic BIST, Embedded Deterministic Test (EDT) and boundary scan. The highlights of the section addressing ATPG include: design rules checking, random and deterministic test pattern generation, pattern compression techniques, test pattern verification, combinational and sequential pattern types, at-speed test. Special section of the tutorial is devoted to testing of embedded memories. It reviews: memory types, fault models, test algorithms, and test methods (Memory BIST and Vector translation).

1:30pm-5:15pm
Tutorial A.2:

Supplemental Test Methods

Organizer: Sreejit Chakravarty, Intel Corporation
Presenter: Sreejit Chakravarty, Intel Corporation

The shorter design cycle time – to meet time to market, aggressive designs – to meet performance targets in order to keep ahead of the competition etc. are resulting in a host of quality issues that the manufacturing community is faced with. For ASICS, the traditional approach of relying on structural testing and the classical s@ fault model leaves quality holes. For testing high-end processors, use of expensive functional testers is inevitable. This raises the question of how to ensure quality products while using low cost testers. Among many, two ideas are being explored by the test community viz. current based testing, referred to here as IDDx testing, and defect based testing. The commonality of these two distinct testing techniques is that both take into account the kind of defects that occur during manufacturing and proactively target them. Both can be used in conjunction with low cost structural testing. This tutorial provides an overview of these two important areas of test research that will only grow in importance with time.

Tutorial Track B

Design for Reliability in UDSM: Issues and Solutions

Carmel Room

Chair & Moderator: Ken Shepard, Columbia University

8:30am-10:15am
Tutorial B.1:

Issues in Deep Submicron State-of-the-Art ESD Design

Organizer: Charvaka Duvvury, Texas Instruments, Inc.
Presenter: Charvaka Duvvury, Texas Instruments, Inc.

Electrostatic Discharge (ESD) has been one of the major reliability concerns for IC technologies. In the development of protection circuits against ESD the role of the designers is becoming increasingly important. This tutorial will address the important issues for the design of IC protection circuits built with state-of-the-art deep submicron technologies. The tutorial will present the fundamental aspects of the ESD protection design as well as the latest novel clamps. The effects of process technologies on the protection device performance and the effective choice of the protection scheme for different design applications, including RF circuits, will be discussed. In addition to low voltage CMOS, SOI, BiCMOS, and High Voltage MOS will also be considered. All aspects of the current design techniques and the simulation methods to optimize the protection schemes will be discussed. Finally, the CAD tools available for ESD design will be reviewed.

10:30am-12:15pm
Tutorial B.2:

Electromigration Reliability Issues in High Performance Circuit Design

Organizer: J. Joseph Clement, Sandia National
Presenter : J. Joseph Clement, Sandia National

This tutorial aims to provide circuit designers, CAD and reliability engineers with a common framework they can use in order to achieve the desired circuit performance and reliability goals. The first part of this tutorial will start with a review of the physical mechanisms underlying the electromigration phenomenon, the driving forces, and the effects of the thin-film metal material properties and the surrounding insulating dielectric. Next common accelerated testing procedures and the model generally used to extrapolate test results to predict interconnect lifetimes will be presented. The relationship between constant current life tests and the pulsed currents found in an operating circuit environment will be addressed. The second part of the tutorial will focus on design procedures and CAD tools that can be used to assess and assure the electromigration reliability of a circuit design. The concept of a "reliability budget" will be introduced. Finally, promising directions for future work will be explored.

* This tutorial is part of the IEEE Computer Society TTTC Test Technology Educational Program (TTEP) 2002.

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1:30pm-3:15pm
Tutorial B.3:

Ultra-Thin Gate Oxide Reliability and Implications for Design

Organizer: John S. Suehle, National Institute of Standards & Technology
Presenter: John S. Suehle, National Institute of Standards & Technology

New observations of a voltage dependent voltage acceleration parameter and non-Arrhenius temperature dependence will be presented. The current understanding of soft breakdown will be discussed and proposed techniques for detecting breakdown presented. The implications of soft breakdown on circuit functionality and the applicability of applying current reliability characterization and analysis techniques to project the reliability of future alternative gate dielectrics will be discussed. An overview of past and present thin oxide reliability characterization techniques will be presented. A special emphasis will be placed on issues relating to the characterizing and understanding of breakdown in current technology ultra-thin gate oxides where excessive tunneling currents and soft breakdown complicate reliability assessment.

3:30pm-5:15pm
Tutorial B.4:

Hot Carrier Reliability and Design Considerations

Organizer: Shian Aur, Texas Instruments, Inc.
Presenter: Shian Aur, Texas Instruments, Inc.

In this tutorial, hot carrier effects will be first demonstrated using device I-V characteristics before and after DC stress. Then, the hot carrier mechanism will be reviewed and the hot carrier lifetime prediction methodology be discussed. In circuit operation, device is under AC stress. The circuit hot carrier effects will be discussed in an inverter example. Then, a three-stage inverter chain will be demonstrated to compare the DC and AC stress cases. In real circuits, the circuit performance degradation is the concern, not necessarily the individual transistors. The circuit hot carrier simulator (HOTRON) is used to discuss several circuit examples. The mechanism in HOTRON simulator will be discussed. Some design guidelines for checking the circuit design reliability will be provided.

Tutorial Track C

Interconnect and Device Modeling for Quality Design

Santa Clara Room

Chair & Moderator: Amit Mehrotra , University of Illinois, Urbana

8:30am-10:15am
Tutorial C.1:

Power/Ground Integrity Issues for Sub-130nm IC Designs

Organizer: Norman Chang, Apache Design Solutions, Inc.
Presenter: Norman Chang, Apache Design Solutions, Inc.

This tutorial introduces Power-Ground integrity, addressing its importance, verification methodology, and problem solution. Special focus will be given to inductance related L di/dt noise and LC resonance, which has been over-looked and will become significant in the near future. The impacts of these issues and methods to tame their effects will also be presented in this tutorial.

10:30am-12:15pm
Tutorial C.2:

A General and Comparative Study of $RC^{(0)}$, RC, RCL and RCLK Modeling of Interconnects and their Impact on the Design of Multi-Giga Hertz Processors

Organizer: Ersed Akcasu, OEA International, Inc.
Presenter: Ersed Akcasu, OEA International, Inc.

This tutorial presents a complete step-by-step methodology for achieving the complicated task of $RC^{(0)}$, RC, RCL and RCLK modeling of interconnects and their impact on the design of multi-giga hertz processors. A comparative study of interconnect model complexity is shown through simulated waveforms. Issues in clock circuit design such as shielding, why it is important and how is should be routed and tied, are explained through simulations rather than relying solely on previous practical experiences. The validation is that these methodologies and the simulations shown in this work have been instrumental in a multi-Giga Hertz processor design.

1:30pm-3:15pm
Tutorial C.3:

MOS Modeling, Design Quality, and Modern Analog Design

Organizer: Daniel Foty, Gilgamesh Associates
Presenter: Daniel Foty, Gilgamesh Associates

The first part of this tutorial will examine the present "infrastructure" of MOS modeling for circuit simulation, with particular emphasis on how history has played a role at least as large as that of engineering. The viewpoint will be that of an analog design "consumer" of MOS models who must make the best possible use of a badly flawed infrastructure. In recent years, the entire structure of MOS models has been evolving into continually more complicated and empirical forms, opening up a "reality gap" between a model's mathematical structure and circuit design usage. The need for extensive model "binning" to provide accuracy over a large range of channel geometry is causing present-day MOS models to more closely approach table-lookup methods, rather than a design-useful description of the underlying MOS technology. Among the many severe consequences of the present situation, the MOS models have become completely removed from good circuit design practices, particularly for analog design; many common analog circuits cannot even be simulated properly using "modern" MOS models! The final part of this tutorial will describe a new direction for MOS modeling, based on the use gms/Id over the range weak, moderate, and strong inversion. This approach provides a more modern grounding for understanding the MOSFET, and also leads directly into simple and powerful techniques for effective analog circuit design using modern deep-submicron technology.

3:30pm-5:15pm
Tutorial C.4:

RLCK Extraction and Simulation in High-Speed SoC Designs

Organizer: Li-Fu Chang & Keh-Jeng Chang, Sequence Design, Inc.
Presenter: Li-Fu Chang, Sequence Design, Inc.

Signal integrity is becoming essential in today's advanced System-on-Chip (SoC) designs. According to recently published statistics for advanced VLSI/SoC design projects, more than 50% of design closure time is spent on chip verifications, especially those above

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500 MHz. One key area to achieve reliable signal integrity modeling and prediction is to extract SoC's RLCK accurately and efficiently for coupling noise analysis. Innovative software architecture is needed so that PEEC method can be used in solving Maxwell equations while distributed RLCK netlists can be extracted for critical on-chip interconnects. In this tutorial, a PEEC-based SoC design software is presented. With the advent of SPICE-level full-chip simulation tools, the software must take into account the capacity of those simulators. Since the software extracts mutual inductance (K), the impact of K on signal integrity will be explained using an advanced 8-metal nanometer technology.

Tutorial Track D

Design Flows and Methodologies

San Jose Room

Chair & Moderator: Resve Saleh, University of British Columbia

8:30am-10:15pm

Tutorial D.1

nVHDL: A Hardware Design Language for Modeling Discrete and Analog Designand Simulation of Mixed-Signal Electronic Systems

Organizer: Sumit Ghosh, Stevens Institute of Technology
Presenter: Sumit Ghosh, Stevens Institute of Technology

The tutorial will focus on the fundamental principles and concepts that underlie every hardware description language invented to-date. It will begin with a quick survey of the classical HDLs for digital systems, discuss Verilog, and then focus heavily on VHDL. HDLs for analog systems such as VHDL-AMS and their basic weaknesses, starting from the fundamental requirements of mixed-signal electronic designs will be examined. Next, the tutorial will concentrate, through meaningful and real-world examples, on how to accurately model hardware so as to get reliable results from HDL simulations. The issues of concurrent simulation of VHDL models on parallel processors and new transport delay semantics that will enable the modeling of PCI and other sophisticated buses based on electromagnetic reflections will be addressed. Finally, in the tutorial, the present problems with VHDL will be examined and current research in "mixed signal" modeling and simulation, that may constitute the basis for a future evolution in HDL technology, namely nVHDL will be reviewed. Time permitting, the tutorial will also explain how to design HDL simulators.

10:30am-12:15pm

Tutorial D.2

Platform-Based Design: A Tutorial

Organizer: Grant Martin, Cadence Design Systems
Presenter1: Grant Martin, Cadence Design Systems
Presenter2: Henry Chang, Cadence Design Systems

This tutorial is an introduction and overview of platform-based design and its key issues. First, the concept will be defined and the platform taxonomy will be illustrated with a number of industrial examples. A brief overview of the basic methodology elements involved in platform-based design will be given. This will concentrate on the key differences from hardware-based design flows: system-level design and embedded software. Finally, key emerging areas in platform-based design, including co-design across design disciplines, the rise of AMS SOCs, and the opportunities offered by emerging programmable fabrics will be discussed.

1:30pm-3:15pm

Tutorial D.3:

Quality Aspects of SOI Circuit Design

Organizer: Andrew Marshall, Texas Instruments, Inc.
Presenter: Andrew Marshall, Texas Instruments, Inc.

This tutorial focuses on challenges of SOI design and test. With the switch from bulk to SOI, combined with technology scaling, new issues are being raised about IC quality and reliability. Design and testing techniques for ICs built on SOI material are explained. This tutorial covers the following topics: Basic analog, digital and memory design techniques for SOI applications. Floating body effects. Differences between design of SOI and bulk – active and passive component performance. Low-voltage low-power SOI CMOS design style, Cross-talk and local heating issues, Simulation of SOI designs, layout techniques for SOI, Testing of SOI circuits to ensure quality product.

3:30pm-5:15pm

Tutorial D.4

Optimization in an Integrated Physical Design Flow

Organizer: Olivier Coudert, Monterey Design Systems, Inc.
Presenter: Olivier Coudert, Monterey Design Systems, Inc.

The purpose of a physical design flow is to take a netlist with a set of constraints (timing, area, power, etc.), and to produce a production worthy layout. This cannot be achieved without considering all the interdependencies between placement, timing, logic optimization, routing, etc. Traditional optimization methods that have been used more or less independently: for example, placement optimization did not interact with logic optimization. Today's need for integrated physical design flows requires these methods to be more "educated" about each other and to work simultaneously. This tutorial will present a physical design flow and describe how different optimization methods (placement, logic, routing) cooperate together.

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Session EP1

Evening Panel Discussion

Cascade/Sierra Room

6:30pm:8:30pm

Are the interoperability standards for EDA too little/too late for real SOC designs?

Organizer: *Pallab Chatterjee, President SiliconMap LLC*
Moderator: *Richard Goering , Managing Editor EE Times*

Description

The panel will examine the emerging interoperability standards and contrast them to the time to market requirements for current designs. There are supporting statements for interoperability standards. However, there are concerns about the results and the delayed delivery. The proposed interoperability standards may not address features of the process technology at the time standards are adopted A second issue facing the design community is the impact on the product specific design methodologies used and the cost in time/money to shift to new methodologies required for these tools that may be more homogenized than optimized for particular types of SOC. Additional issues include support issues for the flow for the standards vs custom flows, point tools vs sub-flow tools, data reuse and migration vs new data creation for use in the current tools, and tool directions and roadblocks for advanced (sub 0.10um) DSM processes. The panel is comprised of EDA, Foundry, Semiconductor Manufacturers, and Design Centers who will discuss their experiences with in-house developed flows, multi-vendor flows based on multiple APIs and the time-to-market tradeoffs of these solutions as an alternative to the 2-3 year delay waiting for committee based standards.

Panelists:

Andrew Moore
Design Services Marketing (EDA)
TSMC
North America

Greg Spirakis
VP, Architecture Group, Director
Design Technology
Intel

Noel Strader
Technical Marketing
Avant! Corporation

Pallab Chatterjee
President
SiliconMap LLC

Joe Hutt
Vice President Technical Sales,
Magma Design Automation

Sunil Joshi
Vice President
Design Automation and
Computer Resources
Sun Microelectronics

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Plenary Session I

Donner/Siskiyou Room

Sponsored by Tavanza

8:30am-12:00pm

Co-Chairs: Res Saleh, ISQED Conference Chair
Kris Verma, ISQED Plenary Chair

8:45am

Welcome and Introduction

8:45am-9:25am

1P.1 IP REUSE QUALITY: "Intellectual Property" or "Intense Pain"?

John Chilton, Sr. VP and
General Manager, Synopsys, Inc.

As systems on a chip become more complex, reuse of third-party intellectual property (IP) becomes more necessary to meet time-to-market deadlines. However, issues surrounding IP quality are very much unresolved. Poor IP quality is the key reason why many IP users feel that "IP" is actually an acronym for "Intense Pain." There are major inconsistencies surrounding basic quality, including fully synchronous design, registered inputs and outputs for IP blocks, and completion of full specifications before design. All these inconsistencies contribute to difficulties in using the IP and integrating it into a chip design. One of the key reasons why quality is still such an issue within the IP community is the issue of "reuse" versus "salvaging." Much of the IP sold over the last few years wasn't really designed for reuse. Instead, it was designed for use in a single chip, then later repackaged (i.e., salvaged) as IP. There has also been tremendous interest in creating IP repositories—fancy Java-based, Web-accessed, and multi-featured custom products meant to hold the wealth of IP. Along the way, though, we forgot to create enough fully reusable IP to warrant these repository investments. Although the challenges in the IP business may seem daunting (and there are many more besides just those that concern quality), they are well worth the effort when you consider the rewards. There's a tremendous need for IP to address the growing productivity gap, which represents a great opportunity for the third-party IP industry.

9:25am-10:05am

1P.2 Why Integrated Yield Management is a Necessity

Y. David Lepejian, President,
CEO and Chairman, HPL

Improving semiconductor yield is a multi-facetted process that must include design, manufacturing, and test. An integrated approach enables companies to rapidly reach higher levels of revenue and profitability. Incorporating design-for-yield concepts early, improving the quality of the test programs, and applying new technology to accelerate the measurement and correction of failure sources in the production process combine to have powerful effect upon company profits, product quality, and time to volume.

Plenary Session I

Continued

10:05am-10:30am

Break

10:30am-11:10am

1P.3 Design Success: Foundry Perspective

Jim Kupec,
President, UMC USA

Leading edge foundries are rolling out new process technologies every two years with today's advance processes capable of producing a quarter billion transistor on a thumb-nail sized chip. The growth of the fabless business model has enabled many companies to organize and build value with the strength of their design capabilities. Quality is often reflected by the continued success of design practices resulting in market success. The many styles of design implementations provided by a large number of companies sharing a common process helps provide a Darwinian view of quality practices. The interaction with design flows, libraries, special purpose IP, memory types are important considerations. This talk will address the trade-offs and successful design technologies used in foundries.

11:10am-11:50am

1P.4 What you don't know CAN hurt you: Designing for survival in a sub-wavelength environment

Y.C. (Buno) Pati,
President and CEO,
Numerical Technologies

The semiconductor industry's promise to deliver an endless array of chip designs to match the voracious appetite for smaller, faster, cheaper devices is in danger of ringing hollow. We could make this commitment with confidence up to recently. But, lately we've hit the wall. We're crashing through the sub-wavelength barrier and we're feeling our way toward designing and manufacturing chips in a challenging new environment without benefit of some key process technologies. Now, to survive and thrive, chipmakers are turning to phase shifting—just a novel, clever concept a few short years ago—as a critical and necessary enabler of producing integrated circuits at dimensions of 0.13 micron and below. Inevitably, chip designers are following suit, not just to match the chipmakers in their march to smaller feature sizes, but to polish their own competitive edge with high-performance chip designs that are easy to produce. They're breaking out of a somewhat isolated mold, knowing that shrinking design times and increasing layout complexity call for new tools and expertise. Most acknowledge that the success of their designs, and indeed, their future viability depends on quickly adopting the tools and expertise that their chip making customers are using so effectively.

Ph.D. Student Forum
Bayshore Foyer
12:30pm-3:30pm

Chair: Kaushik Roy, Purdue University

PhD-1 **AMLETO: A multi-Language Environment for Funtional Test Generation,** Alessandro Fin, Franco Fummi, Graziano Pravadelli, University of Verona, Verona, Italy

PhD-2 **Dependency Preserving Probalistic Modeling of Switching Activity using Bayesian Networks,** Sanjukta Bhanja, N. Ranganathan, University of South Florida, Tampa, FL

PhD-3 **Turn-On Mechanisms of CMOS Devices During ESD Stress with Gate-Driven or Substrate-Triggered Designs,** Tung-Yang Chen, Ming-Dou Ker, National Chiao-Tung University, Taiwan

PhD-4 **A Real Delay Switching Activity Simulator Based on Petri Net Modeling,** Ashok Murugavel, N. Ranganathan, University of South Florida, Tampa FL

PhD-1 **Contribution to Mixed-Signal Design Methodologies Using VHDL-AMS,** Richard Perdriau, University Catholique de Louvain, Louvain-la-Neuve, Belgium

Session 1A
Donner Room
1:00pm - 3:10pm

Interconnect Extraction and Modeling

Co-Chairs: *Rajendran Panda, Motorola*
Sammy Lee, Numerical Technology

1:05pm

1A-1 **Fabrication Technologies for Three-Dimensional Integrated Circuits (Invited),** Rafael Reif, Andy Fan, Kuan-Neng Chen, Shamik Das, Massachusetts Institute of Technology, Cambridge, MA

1:30pm

1A-2 **Coupled Electromagnetic-Circuit Simulation of Arbitrarily-Shaped Conducting Structures Using Triangular Meshes,** Vikram Jandhyala, Yong Wang, Dipanjan Gope, Richard Shi, University of Washington, Seattle, WA

1:55pm

1A-3 **Inductance Aware Interconnect Scaling,** Kaustav Banerjee and Amit Mehrotra[1], Stanford University, Stanford, CA and [1]University of Illinois, Urbana, IL

2:20pm

1A-4 **Accurate Model of Metal-Insulator-Semiconductor Interconnects,** Gaofeng Wang[1], Xiaoning Qi[2], Zhiping Yu[3] and Robert W. Dutton[3], [1]Intpax, Inc., Cupertino, CA, [2]Sun Microsystems, Palo Alto, CA, [3]Stanford University, Stanford, CA

2:45pm

1A-5 **Transition Aware Global Signaling (TAGS),** Himanshu Kaul and Dennis Sylvester, University of Michigan, Ann Arbor, MI

Session 1B
Siskiyou Room
1:00m - 3:10pm

Quality and Interoperability of EDA Tools

Co-Chairs: *Tom Chen, Colorado State University*
Lech Jozwiak, University of Eindhoven, The Netherlands

1:05pm

1B-1 **Using the Open Library Architecture (OLA) Open Source API in Heterogeneous Design Flows (Invited),** Daniel Moritz, LSI Logic, Inc., Bloomington, MN

1:30pm

1B-2 **The OpenAccess Coalition — The Drive to Open Industry Standard Information Model, API, and Reference Implementation for IC Design Data (Invited),** Terry Blanchard, Rick Ferreri and Jim Wilmore, Hewlett-Packard Co.

1:55pm

1B-3 **A Qualification Platform for Design Reuse,** R Seepold, N.Martinez Madrid, A. Vorg, W. Rosenstiel[1], M. Radetzki[2], P. Neumann[2], and J. Haase[2], Forschungszentrum Informatik, Karlsruhe, Germany, [1]University of Tuebingen, Tuebingen, Germany and [2]sci-worx GmbH, Hannover, Germany

2:20pm

1B-4 **Advancing Quality of EDA Software (Invited),** Giora Ben-Yaacov, Pramod Suratkar, Marsha Holliday, and Karen Bartleson, Synopsys, Inc.

2:45pm

1B-5 **Interoperability and Quality of New EDA Tools for Sequential Logic Synthesis,** Aleksander Slusarczyk and Lech Jozwiak, Eindhoven University of Technology, Eindhoven, The Netherlands

Session 1C

Oak Room

1:00m - 3:10pm

Design for Test

Co-Chairs: *George Alexiou, University of Patras & CTI, Greece*
Jayashree Saxena, Texas Instruments

1:05pm

1C-1 **Test Generation and Fault Modeling for Stress Testing (Invited)**
Robert C. Aitken, Agilent Technologies

1:30pm

1C-2 **Extending the Viability of I_{DDQ} Testing in the Deep Submicron Era,** Y. Tsiatouhas, Th. Haniotakis[1], D. Nikolos[2], and A. Arapoyanni[3], Integrated Systems Development S.A., Athens, Greece, [1]Southern Illinois University, Carbondale, IL, [2]University of Patras, Patras, Greece, and [3]University of Athens, Athens, Greece

1:55pm

1C-3 **Design of Reconfigurable Access Wrappers for Embedded Core Based SOC Test,** Sandeep Koranne, Tanner Research, Inc. Pasadena, CA

2:20pm

1C-4 **Testing of Analogue Circuits via (Standard) Digital Gates,** Daniela De Venuto, Michael J. Ohletz[1] and Bruno Ricco[2], Politecnico di Bari, Bari, Italy, [1]Alcatel Microelectronics, Zaventem, Belgium and [2]Universita di Bologna, Bologna, Italy

2:45pm

1C-5 **Automatic Test Program Generation from RT-Level Microprocessor Descriptions,** F. Corno, G. Cumani, M. Sonza Reorda, and G. Squillero, Politecnico di Torino, Torino, Italy

Session 2A

Donner Room

3:30pm - 5:40pm

Design for Process Variations

Co-Chairs: *Lukas van Ginneken, Magma Design*
Pranav Ashar, NEC Labs

3:35pm

2A-1 **Impact Analysis of Process Variability on Clock Skew,** Enrico Malavasi, Stefano Zanella, Min Cao, Julian Uschersohn, Mike Misheloff and Carlo Guardiani, PDF Solutions, Inc., San Jose, CA

4:00pm

2A-2 **Statistical Methods for the Determination of Process Corners,** Michael Kocher and Gerhard Rappitsch, Austriamicrosystems AG, Premstatten, Austria

4:25pm

2A-3 **Design Method and Automation of Comparator Generation for Flash A/D Converter,** Daegyu Lee, Jincheol Yoo and Kyusun Choi, Pennsylvania State University, University Park, PA

4:50pm

2A-4 **A Hybrid PPC Method Based on the Empirical Etch Model for the 0.14um DRAM Generation and Beyond,** Chul-Hong Park, Soo-Han Choi, Sang-Uhk Rhie, Dong-Hyun Kim, Jun-Seong Park, Tae-Hwang Jang, Ji-Soong Park, Yoo-Hyon Kim, Moon-Hyun Yoo and Jeong-Taek Kong, Samsung Electronics Co., Ltd., Yongin City, Korea

5:15pm

2A-5 **A Robust Digital Delay Line Architecture in a 0.13umCMOS Technology Node for Reduced Design and Process Sensitivities,** Prasun Raha, Scott Randall, Richard Jennings, Bob Helmick, Ajith Amerasekera and Baher Haroun, Texas Instruments, Dallas, TX

Session 2B

Siskiyou Room

3:30pm - 5:40pm

Power, Signal and EMI Analysis and Optimization

Co-Chairs: *Amit Narayan, EDA Consultant*
Marco Casale-Rossi, STMicroelectonics

3:35pm

2B-1 **Optimization of the Power/Ground Network Wire Sizing and Spacing based on Sequential Newtork Simplex Algorithm,** Ting-Yuan Wang, Charlie Chung-Ping Chen, University of Wisconsin, Madison, WI

4:00pm
2B-2 **Simultaneous Switching Noise and Resonance Analysis of On-Chip Power Distribution Network,** Geng Bai and Ibrahim N. Hajj[1] Nassada Corp., Santa Clara, CA and [1]American University of Beirut, Beirut, Lebanon

4:25pm
2B-3 **An EMI-Noise Analysis on LSI Design with Impedance Estimation,** Kenji Shimazaki, Shouzou Hirano and Hiroyuki Tsujikawa, Matsushita Electric Industrial Co., Ltd., Kyoto, Japan

4:50pm
2B-4 **Chip Level Signal Integrity Analysis & Crosstalk Prediction Using Artificial Neural Nets,** A. Ilumoka, University of Hartford, West Hartford, CT

5:15pm
2B-5 **On the Use of Windows for Accurate Analysis of Package Interconnects,** Wendemagegnehu T. Beyene and Chuck Yuan, Rambus, Inc., Los Altos, CA

Session 2C
Oak Room
3:30pm - 5:40pm

Methods and Metrics for Design Quality

Co-Chairs: *Tak Young, Monterey Design*
Jay Michlin, EDA Consultant

3:35pm
2C-1 **Productivity Optimization Techniques for the Proactive Semiconductor Manufacturer, (Invited),** Dan Maynard, IBM, Essex Junction, VT

4:00pm
2C-2 **A New Design Cost Model for the 2001 ITRS (Invited),** Andrew Kahng and Gary Smith, Dataquest, San Jose, CA

4:25pm
2C-3 **Optimal Sequencing Energy Allocation for CMOS Integrated Systems,** Martin Saint-Laurent, Vojin Oklobdzija[1] Simon S. Singh[2], Madhavan Swaminathan[3], Intel Corp., Austin, TX, [1]University of California, Davis, CA, [2]National Semiconductor Corp., Santa Clara, CA and [3]Georgia Institute of Technology, Atlanta, GA

4:50pm
2C-4 **Design, Manufacture and Test - Quality Test Estimation,** Jim Gilbert, David Johnson and Ian Bell, University of Hull, Hull, United Kingdom

5:15pm
2C-5 **Measurement of Inherent Noise in EDA Tools,** Andrew B. Kahng and Stefanus Mantik[1], University of California at San Diego, La Jolla, CA and [1]University of California, Los Angeles, CA

Session EP2
Evening Panel Discussion
Cascade/Sierra Room

6:30pm:8:30pm

Process Variation: Is it too much to handle?
Sponsored by Numerical Technologies

Organizers: *Vivek De, Intel*
Siva Narendra, Intel
Moderator: *Ron Wilson, Editor in chief, ISD magazine*

Description

The panel will discuss the impact of increasing process variation with technology scaling from the aspect of manufacturing, design, and design tools. Increase in process induced parameter variation makes it harder to understand the correlation between what was designed and what gets manufactured. To guarantee product quality this often results in the need for worst-case assumptions during design phase. Can we continue this? If not, should the manufacturing and process engineers get their act together and reduce variation? Or, should the circuit designers stop complaining and learn to live with the variation by building process tolerant circuits? How should the CAD community help in these endeavors?

Panelists

Duane Boning
Associate Professor and Associate Director of Microsystems Technology Labs,
MIT,
Cambridge, MA

Steve Duvall
Fellow and Director of Strategic Investments,
Intel Corporation,
Sydney, Australia

James Meindl
Professor and Director of Microelectronics Research Center,
Georgia Tech,
Atlanta, GA

Sani Nassif
Manager,
IBM Austin Research Lab,
Austin, TX

Jan Rabaey
Professor and Co-founder
Berkeley Wireless Research Council,
University of California – Berkeley, CA

Doug Verret
Fellow and Director of Yield,
Texas Instruments,
Austin, TX

Plenary Session II

Donner/Siskiyou Room

8:30am-11:50am

Co-Chairs: Kris Verma, ISQED Plenary Chair
Lech Jozwiak, ISQED Plenary Vice Chair

8:30am

Introduction

8:45am

2P.1 **The Role of ICs in the Creation of a Connected World and the importance of Product Quality**

Atiq Raza
Chairman and CEO,
Raza Foundries Inc.

Human Beings being social have had a need to communicate. The modern chapter in enabling large scale communication has been aided by intelligence in the transport, distribution, protection, traffic management, decoding, analyzing and displaying of communication content. The intelligence has been embedded in an explosive confluence of Software, Systems and Integrated Circuits. This has resulted in the most amazing transformation of the way we live our lives, work, and engage in all other necessary and capricious activity. It has also created a huge economic footprint on the Gross Domestic Product of the United States of America. With a massive transformation that has occurred in such a short time, this throbbing network across the planet has to operate reliably because of the precious payload it carries.

9:25am

2P.2 **Wireless Systems-on-a-Chip Design**

Bob Brodersen
Dept. of EECS,
University of California, Berkeley

There is a fundamental shift that is occurring in the implementation of wireless systems. Not only is the underlying technology shifting to mainstream CMOS technology, but the applications and specifications of the supported links is also rapidly evolving. The multiple inter-related technologies required for implementation of such wireless systems requires a co-design strategy in communication algorithms, digital architectures as well as the analog and digital circuits required for their implementation. Critical to good design of these chips is the definition of energy and area performance metrics that can facilitate the tradeoff of issues such as the cost of providing flexibility or the amount of parallelism to exploit. These design decisions can result in differences of orders of magnitude in the metrics between what is possible in the technology and what is often achieved if the costs are not fully understood. A design infrastructure which supports architectures, which optimizes the metrics, will be described for wireless systems that provides a fully automated chip design flow design flow from a high level system specification.

10:05am

Break

10:30am

2P.3 **Microwave III-V Semiconductors for Telecommunications and Prospective of the III-V Industry**

Chan Shin Wu
President and CEO, WIN
Semiconductors

The Microwave III-V semiconductor IC technology (Primarily GaAs) has emerged as a powerful, enabling, technology for the wireless and optical ommunications in the past 5 years. It has been dominating, or making substantial penetration into, the market for handset power amplifiers and switches, advanced wireless LAN RF front-ends and various other key RF components for broadband wireless, wireless infrastructure, satellite telecommunications, high data rate fiber optical communications and automotive radar applications. The Microwave III-V semiconductor IC industry has grown dramatically in the past 2-3 years. It is worth noting that the majority of the recently formed GaAs Fabs are located in Taiwan. Their intent is to provide pure-play foundry services following the silicon foundry business model developed by TSMC and UMC. In this presentation, we will discuss the key components of III-V microwave transistors (HBT, pHEMT and MESFET etc.) and their RFICs/MMICs, their electrical performance, major applications, market status, trends and opportunities. We will define the current status for the global III-V semiconductors industry, the rapidly growing GaAs MMIC Fab industry in Taiwan and its advantages for providing a one-stop, total solution for the wireless and optical communication components customers.

11:10am

2P.4 **Tomorrows High-quality SoCs Require High-quality Embedded Memories Today**

Ulf Schlichtmann
Senior Director,
Infineon Technologies AG

Embedded memories increasingly dominate SoC designs – whether chip area, performance, power consumption, manufacturing yield or design time are considered. ITRS data indicate that the embedded memory contents of ICs may increase from 20% in 1999 to 90% at the 50nm node by the end of the decade. Therefore, even more than today, the success of tomorrow's SoC design will depend on the availability of high-quality embedded memories. Advanced process technologies pose new challenges for meeting these quality criteria. Some of the challenges are: providing flexible redundancy solutions for embedded SRAMs; designing competitive memories despite ever increasing leakage currents; reducing SRAM susceptibility to soft-error rate (SER). These challenges are bringing about the need for significant innovations in design of embedded memories, much more so than in recent previous process generations. In the presentation, the challenges will be outlined and solutions will be proposed. The focus of the discussion will be on SRAM/ROM, but other technologies such as eDRAM and "1T SRAM" will also be addressed.

Poster Session

Bayshore Foyer

12:30pm - 3:30pm

Co-chairs: Enrico Malavasi, PDF Solutions
Daniela De Venuto, Polytechnic of Bari

P-01
Synthesis of Selectively Clocked Skewed Logic Circuits, Aiqun Cao, Naran Sirisantana, Cheng-Kok Koh and Kaushik Roy, Purdue University, West Lafayette, IN

P-02
Low Power VLSI Architecture of Viterbi Scorer for HMM-based Isolated Word Recognition, Bok-Gue Park, Koon-Shik Cho and Jun-Dong Cho, SungKyunKwan University, Kyunggi-do, Korea

P-03
On Dynamic Delay and Repeater Insertion in Distributed Capacitively Coupled Interconnects, Dinesh Pamunuwa and Hannu Tenhunen, Royal Institute of Technology, Kista, Sweden

P-04
A Comprehensive Layout Methodology and Layout-Specific Circuit Analyses for Three-Dimensional Integrated Circuits, Syed M. Alam, Donald E. Troxel and Carl V. Thompson, Massachusetts Institute of Technology, Cambridge, MA

P-05
Reliable Laser Programmable Gate Array Technology, Zhuo Gao, Ji Luo, Hu Huang, Wei Zhang, and Joseph Bernstein, University of Maryland, College Park, MD

P-06
VC Rating and Quality Metrics: Why Bother?, Pierre Bricaud, Mentor Graphics Corp., Sophia Antipolis, France

P-07
An Efficient Seeds Selection Method for LFSR-Based Test-per-Clock BIST, E. Kalligeros, X. Kavousianos, D. Bakalis, and D. Nikolos, University of Patras, Patras, Greece

P-08
An Integrated Tool for Analog Test Generation and Fault Simulation, Sule Ozev and Alex Orailoglu, University of California, San Diego, La Jolla, CA

P-09
A Hybrid BIST Architecture and its Optimization for SoC Testing, Gert Jervan, Zebo Peng, Raimund Ubar[1], and Helena Kruus[1], Linkoping University, Linkoping, Sweden and [1]Tallinn Technical University, Estonia

P-10
Native Mode Functional Self-Test Generation for Systems-on-Chip, Kamalnayan Jayaraman, Vivekananda M. Vedula[1] and Jacob A. Abraham, Intel Corporation, Chandler, AZ and [1]University of Texas, Austin, TX

P-11
Incorporating Fault Tolerance in Analog-to-Digital Converters (ADCs), Mandeep Singh and Israel Koren[1], Advanced Micro Devices, Austin, TX and [1]University of Massachusetts, MA

P-12
Human Immune System Inspired Architecture for Self-Healing Digital Systems, P.K. Lala and B. Kiran Kumar, University of Arkansas, Fayetteville, AR

P-13
Impact of Low-K on Crosstalk, G. Serval, D. Deschacht, F. Saliou[1], J.L. Mattei[1], and F. Huret[1], UMR C.N.R.S., Montpellier, France and [1]Universite de Bretagne Occidentale, Brest, France

P-14
Improving the Efficiency and Quality of Simulation-Based Behavioral Model Verification Using Dynamic Bayesian Criteria, Amjad Hajjar and Tom Chen, Colorado State University, Fort Collins, CO

P-15
In Search of the Origin of VHDL's Delta Delays, Sumit Ghosh, Stevens Institute of Technology, Hoboken, NJ

P-16
Inductive Characteristics of Power Distribution Grids in High Speed Integrated Circuits, Andrey V. Mezhiba and Eby G. Friedman, University of Rochester, Rochester, NY

P-17
Characterizing the Current Degradation of Abnormally Structured MOS Transistors Using a 3D Poisson Solver, Jin-Kyu Park, Keun-Ho Lee, Chang-Sub Lee, Gi-Young Yang, Young-Kwan Park and Jeong-Taek Kong, Samsung Electronics, Co., Ltd., Kyungki-Do, Korea

P-18
AC Analysis of Thin Gate Oxide MOS with Quantum Mechanical Corrections, Tae-Young Oh, Zhiping Yu and Robert W. Dutton, Center for Integrated Systems, Stanford, CA

P-19
ESD Protection Design for Mixed-Voltage I/O Circuit with Substrate-Triggered Technique in Sub-Quarter-Micron CMOS Process, Ming-Dou Ker, Chien-Hui Chuang, Kuo-Chun Hsu, and Wen-Yu Lo[1], National Chiao-Tung University, Hsinchu, Taiwan and [1]Silicon Integrated Systems (SiS) Corp., Hsinchu, Taiwan

P-20
Design of ESD Protection Device Using Statistical Methods, Naoyuki Shigyo, Hirobumi Kawashima and Seiji Yasuda, Toshiba Corporation Semiconductor Company, Yokohama, Japan

P-21
Economic Analysis of a Stopping- Rule in Branch Coverage Testing, Mehmet Sahinoglu, Scott Glover, Troy State University, Montgomery, AL

Session 3A
Donner Room
1:00pm - 3:10pm

Design Issues for Power and Noise Management

Co-Chairs: *Ajith Amerasekera, Texas Instruments*
Farid Najm, University of Toronto, Canada

1:05pm
3A-1 **Device Physics Impact on Low Leakage, High Speed DSP Design Techniques (Invited),** David Scott, Shaoping Tang, Song Zhao, and Mahalingam Nandakumar, Texas Instruments, Dallas, TX

1:30pm
3A-2 **Power Supply Noise Suppression via Clock Skew Scheduling,** Wai-Ching Lam, Cheng-Kok Koh and Chung-Wen Tsao[1], Purdue University, West Lafayette, IN and [1]Celestry Design Technologies, Inc., San Jose, CA

1:55pm
3A-3 **Trading off Reliability and Power-Consumption in Ultra-Low Power Systems,** Atul Maheshwari, Wayne Burleson and Russell Tessier, University of Massachusetts, Amherst, MA

2:20pm
3A-4 **Asynchronous Circuits: An Increasingly Practical Design Solution (Invited),** Peter Beerel, Fulcrum Microsystems and University of Southern California, Los Angeles, CA

2:45pm
3A-5 **Trends in Low Power Digital Systems on Chip Design (Invited),** R. Saleh, G. Lim, T. Kadowaki[1], K. Uchiyama[2], University of British Columbia, Canada, [1]Sony Corp. Japan, [2]Hitachi, Ltd., Japan

Session 3B
Siskiyou Room
1:00pm - 3:10pm

Verification in Achieving Design Quality

Co-Chairs: *Lech Jozwiak, University of Eindhoven, The Netherlands*
Olivier Sentieys, ENSSAT, France

1:05pm
3B-1 **Promising Directions in Hardware Design Verification (Invited),** Shaz Qadeer, Serdar Tasiran, Compaq Systems Research Center, Palo Alto, CA

1:30pm
3B-2 **Behavioral IP Specification and Integration Framework for High-Level Design Reuse,** Sebastien Pillement, Daniel Chillet, [1]Olivier Sentieys,University of Rennes, Lannion France and [1]IRISA-INRIA, Rennes, France

1:55pm
3B-3 **On the Relation Between SAT and BDDs for Equivalence Checking,** Sherief Reda, Rolf Drechsler[1] and Alex Orailoglu, University of California at San Diego, La Jolla, CA and [1]University of Bremen, Bremen, Germany

2:20pm
3B-4 **Integrated Inductors Modeling and Tools for Automatic Selection and Layout Generation,** Jose Sendra[1,2], Javier del Pino[1,2], Antonio Hernandez[1,2], Javier Hernandez[2], Jaime Aguilera[2,4] and Andres Garcia-Alonso[3], Antonio Nunez[1,2], [1]University of Las Palmas de Gran Canaria, Spain, [2]INCIDE, Canary S.L., [3]CEIT, Spain, and [4]University of Navarra, Spain

2:45pm
3B-5 **Organization of Microprocessor Design Process Using Internet-Based Interoperable Workflows,** Nguyen Quang Trung, Artur Kokoszka, Krystyna Siekierska, Adam Pawlak, Dariusz Obrebski, and Norbert Lugowski, Institute of Electron Technology, Warsaw, Poland

Session 3C
Oak Room
1:00pm - 3:10pm

Signal Integrity

Co-Chairs: *Narain Arora, Simplex*
Dennis Sylvester, University of Michigan

1:05pm
3C-1 **Pre-route Noise Estimation in Deep Submicron Integrated Circuits,** Murat R. Becer, David Blaauw[1], Rajendran Panda, and Ibrahim N. Hajj[2], Motorola, Inc., Austin, TX, [1]University of Michigan, Ann Arbor, MI, and [2]American University, Lebanon

1:30pm
3C-2 **Time-Domain Simulation of Variational Interconnect Models,** Emrah Acar, Sani Nassif, Ying Liu, and Lawrence T. Pileggi[1], IBM Austin Research Labs., Austin, TX and [1]Carnegie Mellon University, Pittsburgh, PA

1:55pm
3C-3 **Noise Injection and Propagation in High Performance Designs,** Vladimir Zolotov, David Blaauw[1], Rajendran Panda and Chanhee Oh, Motorola, Inc., Austin, TX and [1]University of Michigan, Ann Arbor, MI

2:20pm
3C-4 **Efficient Closed-Form Crosstalk Delay Metrics,** Lauren Hui Chen and Malgorzata Marek-Sadowska[1], Avant! Corp., Fremont, CA and [1]University of California, Santa Barbara, CA

2:45pm
3C-5 **False-Noise Analysis Using Resolution Method,** Alexey Glebov, Sergey Gavrilov, David Blaauw[1], Vladimir Zolotov[2], Rajendran Panda[2], and Chanhee Oh[2], MicroStyle, Moscow, Russia, [1]University of Michigan, Ann Arbor, MI and [2]Motorola, Inc., Austin, TX

Session 4A
Donner Room
3:30pm - 5:40pm

Low Power Design Techniques

Co-Chairs: *Vivek De, Intel Corporation*
Michael Zelikson, IBM

3:35pm
4A-1 **Low-Power and High-Speed VLSI Design with Low Supply Voltage Through Cooperation Between Levels (Invited),** Takayasu Sakurai, University of Tokyo, Tokyo, Japan

4:00pm
4A-2 **Does Q=MC^2? (On the Relationship Between Quality in Electronic Design and the Model of Colloidal Computing) (Invited),** Radu Marculescu and Diana Marculescu, Carnegie Mellon University, Pittsburgh, PA

4:25pm
4A-3 **Mixed RTL/Static Logic Synthesis Using Genetic Algorithms for Low-Power Applications,** Geun Rae Cho and Tom Chen, Colorado State University, Fort Collins, CO

4:50pm
4A-4 **Structural Decomposition with Functional Considerations for Low Power,** Chih-Hung Lee, Yu-Chung Lin, Hsin-Hsiung Huang, and Tsai-Ming Hsieh, Chung-Yuan Christian University, Chung-Li, Taiwan

5:15pm
4A-5 **ALBORZ: Address Level Bus Power Optimization,** Yasdan Aghaghiri, Farzan Fallah[1] and Massoud Pedram, University of Southern California, Los Angeles, CA and [1]Fujitsu Labs of America, Sunnyvale, CA

Session 4B
Siskiyou Room
3:30pm - 5:40pm

Advanced Device Technology Issues in Circuit Design

Co-Chairs: *Ken Shepard, Columbia University*
Chune-Sin Yeh, Celestry

3:35pm
4B-1 **Megagate ASICs for the Thuraya Satellite Digital Signal Processor, (Invited)** David Sunderland, Gary Duncan, Brad Rasmussen, Harry Nichols, Dan Kain, Lawrence Lee, Brian Clebowicz, Rick Hollis, Larry Wissel[1], and Tad Wilder[1], Boeing Satellite Systems, El Segundo, CA and [1]IBM Microelectronics, Essex Junction, VT

4:00pm
4B-2 **Studying the Impact of Gate Tunneling on Dynamic Behaviors of Partially-Depleted SOI CMOS Using BSIMPD,** Pin Su, Samuel K.H. Fung[1], Weidong Liu, and Chenming Hu, University of California, Berkeley, CA and [1]IBM SRDC, Hopewell Junction, NY

4:25pm
4B-3 **High Performance Double-Gate Device Technology Challenges and Opportunities (Invited),** Meikei Leong, H.S. Philip Wong[2], Edward Nowak[1], Jakub Kedzierski[2] and Erin Jones[2], IBM SRDC, Hopewell Junction, NY, [2]IBM Microelectronics, Essex Junction, VT and [2]IBM-TJ Watson Research Center, Yorktown Heights, NY

4:50pm
4B-4 **Modeling and Design of a Low-Voltage SOI Suspended-Gate MOSFET (SG-MOSFET) with a Metal-Over-Gate Architecture**, Adrian Ionescu, Vincent Pott, Raphael Fritschi, Kaustav Banerjee[1], Michel Declercq, Philippe Renaud, Cyrille Hibert, Philippe Fluckiger and Georges Racine, Swiss Federal Institute of Technology, Lausanne, Switzerland and [1]Stanford University, Stanford, CA

5:15pm
4B-5 **Single Electronics - How it Works. How it's Used. How it's Simulated (Invited),** Christoph Wasshuber, Texas Instruments, Dallas, TX

Session 4C
Oak Room
3:30pm - 5:40pm

Design, Planning and Closure

Co-Chairs: *Charlie Chen, University of Wisconsin*
Eileen You, Broadcom

3:35pm
4C-1 **Timing and Design Closure in Physical Design Flows (Invited),** Olivier Coudert, Monterey Design, Sunnyvale, CA

4:00pm
4C-2 **A Thermal-Aware Superscalar Microprocessor (Invited),** Chee How Lim, W. Robert Daasch and George Cai[1], Portland State University, Portland, OR and [1]Intel Corp., Austin, TX

4:25pm
4C-3 **Formulate for Performance Optimization and Their Applications to Interconnect-Driven Floorplanning,** Nicholas Chia-Yuan Chang, Yao-Wen Chang[1] and Iris Hui-Ru Jiang[1], Global Unichip Corp., Hsinchu, Taiwan and [1]National Chiao-Tung University, Hsinchu, Taiwan

4:50pm
4C-4 **Hierarchical Front-End Physical Design Solution Drives Modified Hand-Off (Invited),** Wei-Jin Dai and Michael Courtoy, Silicon Perspective, Santa Clara, CA and Mitsubishi Electric Corp.

5:15pm
4C-5 **Future SOC Design Challenges and Solutions (Invited),** Charlie Chung-Ping Chen[1], Ed Cheng[2], [1]University of Wisconson, Madison, WI, [2]Synopsys, Mountain View, CA

Workshop I

San Jose Room

RF IC Design for Wireless Communication

Organizer & Moderator
Antonio Nunez, University of Las Palmas, Spain

8:30am-10:15pm
Session I.1:

CMOS Multistandard Transceivers for Wireless Communication
Presenter: Mohammed Ismail, Ohio-State University, OH

The Challenge of Passive Component Design on Silicon
Presenter: Antonio Hernandez, University of Las Palmas, Spain

10:15am-10:30am BREAK

10:30am-12:15pm
Session I.2:

Automatic Integrated Inductor Design
Presenter: José R. Sendra, University of Las Palmas, Spain

Key Issues in Integrated PLL-VCO Design for Wireless Standards
Presenter: Javier Hernandez, INCIDE, San Sebastian, Spain

12:15pm-1:15pm LUNCH

1:15pm-3:00pm
Session I.3:

Design Practice for CMOS RF Circuits at 5GHz and Beyond?
Presenter: Tom Lee, Stanford University, CA

SOI for RFIC Design
Presenter: Jean-Pierre Raskin, UCL, Louvain-la-Neuve, Belgium

3:00pm-3:15pm COFFEE BREAK

3:15pm-5:00pm
Session I.4:

Power Amplifier Design
Presenter: Hamid Rategh, Tavanza, Sunnyvale, CA

On Wafer RFIC Measurement Techniques
Presenter: Tariq Alan/Antony Lord, Cascade Microtech, Beaverton. OR

Workshop II

Santa Clara Room

1st Workshop on Selecting Embedded Processor and Memory IPs

Organizer & Moderator:
Yervant Zorian, Virage Logic, Inc.

8:30am-10:15pm
Session II.1:

Where are High Density Embedded Memories Needed?
Presenter: Piotr Sidorowicz, ATMOS, Canada
Mike Briner, SST, USA

10:15am-10:30am BREAK

10:30am-12:15pm
Session II.2:

Selecting Embedded SRAM Cores with High Quality and Yield
Presenter: Alex Shubat, Virage logic, Fremont, CA
Yervant Zorian, Virage Logic, Fremont, CA

12:15pm-1:15pm LUNCH

1:15pm-3:00pm
Session II.3:

Using Optimized Processor Cores
Presenter: Larry Hudepohl, MIPS Technologies, Mountain View, CA

3:00pm-3:15pm COFFEE BREAK

3:15pm-5:00pm
Session II.4:

Where to use Configurable Processor Cores?
Presenter: Kaushik Sheth, Tensilica, Santa Clara, CA
Chen Chung, 3DSP, Irvine, CA

Workshop III
Carmel Room
Device and Interconnect Modeling for VDSM Era

Organizer & Moderator:
Narain D. Arora, Simplex Solutions

8:30am-10:15pm
Session III.1:

Circuit Simulation and Device Modeling for New Generations to Come
Presenter: Mansun Chan, University of California at Berkeley, CA

10:15am-10:30am BREAK

10:30am-12:15pm
Session III.2:

The 100nm-MOSFET Model HiSIM and its Extension to RF Applications
Presenter: Hiroo Masuda, M. Miura-Mattausch, STARC and University of Hiroshima, Japan

12:15pm-1:15pm LUNCH

1:15pm-3:00pm
Session III.3:

Challenges of VLSI Interconnect Modeling in the DSM Era
Presenter: Narain Arora, Simplex Solutions, Sunnyvale

3:00pm-3:15pm COFFEE BREAK

3:15pm-5:00pm
Session III.4:

A Practical Approach of Chip Level Interconnect Inductance Extraction
Presenter: Kenneth L. Shepard, Columbia University, New York