Design Success: Foundry Perspective

Jim Kupec
CEO of AmmoCore Technology, Inc.
Previous President of UMC-USA
“It is not the strongest of the species to survive, nor the most intelligent, but rather the one most responsive to change.”

Technology is Rapidly Advancing

SIA ROADMAP

1999 2000 2001 2002 2003 2004 2005

0.18µm → 0.13µm Cu → 0.09µm Cu

* Courtesy of ITRS

UMC ROADMAP

1999 2000 2001 2002 2003 2004 2005

0.18µm → 0.13µm Cu → 0.10µm Cu → 0.07µm Cu

* Courtesy of UMC
Technology is Rapidly Accelerating

ITRS Roadmap Acceleration Continues…Half Pitch

Technology Node – DRAM Half-Pitch (nm)

Year of Production

* Courtesy of ITRS
Disintegration Allows More Advanced Resources But...

...Coordination is Critical

Example
The Big Hard Chips

Usable Gates in Different Technologies and Die Sizes

Usable Gates in Millions

Technologies

180nm 130nm 100nm 70nm

14x14mm 12x12mm 10x10mm 8x8mm
Big Chips are Real

* Chip courtesy of Xilinx*
The Big Hard Chip

Usable Gates in Millions

Technologies

180nm 130nm 100nm 70nm

8 x 8mm 10x10mm 12x12mm 14x14mm 20x20mm

* From ITRS/ AmmoCore Estimates
Chip Size Estimates

Design Gap
- EDA Methodology
  - DSM
  - Complexity
- IP
  - Memory
  - Analogue
  - Integration of Logic

% = Silicon consumed by various chip sizes

Chip Dimensions
12 x 12mm
8 x 8mm
Rapidly Expanding Design Gap

• New systems will need to take advantage of advances in IC manufacturing technology

• Finer process geometries provide ability to manufacture >30M gates on a single die

• Ability to implement large Systems in silicon will decline due to physical design limitations

**Physical design methodologies will not scale**

<table>
<thead>
<tr>
<th></th>
<th>1997</th>
<th>1999</th>
<th>2001</th>
<th>2003</th>
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<tbody>
<tr>
<td>IC Physical Size (cm²)</td>
<td>4.8</td>
<td>8.0</td>
<td>8.5</td>
<td>9.0</td>
</tr>
<tr>
<td>Area after Mem (cm²)</td>
<td>2.9</td>
<td>4.8</td>
<td>5.1</td>
<td>5.4</td>
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<tr>
<td>Auto-layout Tx (M)</td>
<td>23.0</td>
<td>67.2</td>
<td>81.6</td>
<td>129.6</td>
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<tr>
<td>Equivalent Gates (M)</td>
<td>5.8</td>
<td>16.8</td>
<td>20.4</td>
<td>32.4</td>
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</tbody>
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Sources: SIA, Dataquest
Design Gap Creates Opportunity… If Early Adoption is Successful

Sensitivity of Profits over Product Life

* From Accelerating Innovation
Challenges of Big Multi-Million Gate Chips

- Deep Submicron Effects Are Critical
- Physical Methodologies Do Not Scale
- Engineering Team Coordination Raises Overhead Factors
- IP Integration
DSM Challenges

Metal Modeling

- Coupling
- Antenna
- Electro Migration

* Courtesy of UMC
Modularized Technology

<table>
<thead>
<tr>
<th>Passivation, Fuse, RDL</th>
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<tbody>
<tr>
<td>Multi-layer Interconnect</td>
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<tr>
<td>MIM Capacitor</td>
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<td>RF Inductor</td>
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<tr>
<th>Devices</th>
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<tr>
<td>Core</td>
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<tr>
<td>I/O</td>
</tr>
<tr>
<td>Analog</td>
</tr>
<tr>
<td>Low Vt</td>
</tr>
<tr>
<td>Zero Vt</td>
</tr>
<tr>
<td>Resistor</td>
</tr>
<tr>
<td>Varactor</td>
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</table>

| HS, LL, MPU, LP |
|----------------
| e-SRAM |
| e-FLASH |
| SiGe-BiCMOS |

<table>
<thead>
<tr>
<th>Twin-well / Triple-well / well isolation</th>
</tr>
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<tbody>
<tr>
<td>e-DRAM Trench cell</td>
</tr>
</tbody>
</table>

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<tr>
<th>Starting Material</th>
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</thead>
<tbody>
<tr>
<td>Bulk, EPI, SOI, etc.</td>
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</tbody>
</table>

* Courtesy of UMC
Platform Technology

0.13um SOC Platform
Low-k Dielectrics (k =2.7)
8 Layers Cu Interconnect

- Logic Transistors
  - MPU
  - High Speed (HS)
  - Low Leakage (LL)
  - Very Low Leakage (VLL)

- Mixed Signal/RF CMOS
  - Zero Vt, Low Vt, 2.5V I/O, 3.3V I/O transistors
  - Spiral Cu Inductors, Metal-Metal Caps, Poly Resistor

- e-Memories
  - e-SRAM: 2.28um² bit cell
  - e-DRAM: 0.31um² cell

- EDA Partners
  - Technology Files: DRC, LVS, RC Extraction

- Gold IP Catalog
  - ARM, DAC’s, ADC’s, Advanced I/O’s

- Silicon Shuttle
  - 0.13um Prototyping

- Libraries
  - Memory Compilers
  - RF Design Kits

- =Technology Features

= Design Support Features
EDA: Challenges of Big Chips
(multi-million gates > 10M)

THEN

- Pre-Place IPs
- Place & Route
- Extraction
- Global + Local Optimization

NOW

- Top Level Design Planning
- Global Routing & Optimization

FUTURE

- Platform based Partitioning & Placement
- Top-level Routing & Verification

FLAT

- PRL & P&R

BLOCK/TILE

- B1, B2, B3, B4
- Global Routing & Optimization

PLATFORM

- Productivity
- Flat
- Block/Tile Based
- Gates

...
SRAM: Challenges

**THEN**

First 256 Bit SRAM
- Handcrafted
- Fixed Size
- Technology Bound
- Extremely Optimized

*Courtesy of Fairchild, circa 1970*

**NOW**

Compilation
- Auto-Compilation
- Various Sizes (smaller)
- Technology Sets
- Non-Optimized (limited range, cells, footprint)

**FUTURE**

SRAM Future
- Large Sizes
  - Redundancy
  - 1T, 2T Cells
  - MRAM Cells
- Bit Density Approach 50% DRAM
- ASIC Process Compatible
- Tolerable Process Cost
DRAM: Challenges

**THEN**
- Most Successful 16K DRAM
  - Handcrafted
  - Fixed Size
  - Technology Bound
  - Extremely Optimized

*Courtesy of Mostek, circa 1976*

**NOW**
- EDRAM
  - Place Macro
  - Limited Implementation
  - 8M – 256 Mbit
  - Process Complexity Adder
  - Non-evolved IP

**FUTURE**
- EDRAM Future
  - Technology lags ASICS
  - Process Cost Adder
  - Package Solution Competition
Summary

- Design must be able to coordinate multiple IP sets
  - “Trust but Verify”
- New EDA tools/methodologies required to cope with large densities and DSM
  - “Target Needs”
- Adaptation opportunities are accelerating
  - “Proverbial Inflection Point”