ISQED 2008 CONFERENCE AT A GLANCE

Date	Time					
Monday 3/17/08	9:00am-5:00pm	**TUTORIALS** **Advanced Technology & Design Solutions in Design for Manufacturing Era** Room: Monterey-Carmel				
	6:30pm-8:30pm	**Evening Panel Discussion & Dinner** (Room: Donner) Sponsored by Ponte Solutions **DFM: Is it Helping or Hurting?**				
Tuesday 3/18/08	8:30am-10:15am	**PLENARY SESSION 1P** (Room: Donner) Sponsored by Mentor Graphics **Keynote Speeches by:** **Drew Gude,** Microsoft, **Robert Hum,** Mentor Graphics				
	10:15am-10:30am	**Morning Break**				
	10:30am-12:00pm	**Session 1A** Embedded Tutorial SOC verification Room: San Jose	**Session 1B** Power Conscious Memories Room: Santa Clara	**Session 1C** Speed-up and Timing of Integrated Circuits Room: Monterey	**Session 1D** SER and noise tolerance Room: Carmel	
	12:00pm-1:30pm	**ISQED LUNCHEON** Sponsored by Synopsys **ISQED Quality Award (IQ Award 2008)** , Sponsored by Microsoft **Best Paper Awards,** Sponsored by Magma, and Synopsys **Committee Recognition Awards** (Room: Fir-Oak) Luncheon Keynote **EDA Is Truly Where Electronics Quality Begins!** Antun Domic, Synopsys				
	1:30pm-3:30pm	**Session 2A** Robust SRAM and analog circuits Room: San Jose	**Session 2B** Power and Thermal Management Room: Santa Clara	**Session 2C** Process Variations Room: Monterey	Embedded Sessions E1 2E	**EXHIBITS** Embedded Tutorial 2D
	3:30pm-3:45pm	**Afternoon Break**				
	3:45pm-5:45pm	**Session 3A** System and Circuit Synthesis Room: San Jose	**Session 3B** Process, Characterization and Temperature-aware Design Room: Santa Clara	**Session 3C** Processor Test Verification / Delay Diagnosis Room: Monterey	Embedded Session 3E	Embedded Panel 3D
Wednesday 3/19/08	8:30am-10:15am	**PLENARY SESSION 2P** (Room: Donner) **Keynote Speeches by:** **Sanjiv Taneja**, Cadence, **Chandu Visweswariah**, IBM, **Rich Goldman**, Synopsys				
	10:15am-10:30am	**Morning Break**				
	10:30am-12:00pm	**Session 4A** Co-design Applications for IC Packages Room: San Jose	**Session 4B** Embedded Tutorial Robust Design Methodologies Room: Santa Clara	**Session 4C** Tools and Interconnect Room: Monterey	**Session 4D** Sequential Analysis, Defect Modeling and At-speed Testing Room: Carmel	
	12:00pm-1:30pm	**Lunch and Panel Discussion LP2, Sponsored by Cadence Design Systems** **Statistical Design - Solutions Searching for Problems??** Room: Donner				
	1:30pm-3:30pm	**Session 5A** Modeling and analysis in physical design Room: San Jose	**Session 5B** Emerging Technologies and Novel Applications Room: Santa Clara	**Session 5C** Statistical timing Room: Monterey	**Session 5D** Modern Processor Design Room: Carmel	
	3:30pm-3:45pm	**Afternoon Break**				
	3:45pm-5:45pm	**Session 6A** Modeling and Design of Reliable Circuits Room: San Jose	**Session 6B** Design for Manufacturing Room: Santa Clara	**Session 6C** Structural test Room: Monterey	**Session 6D** Advance Design Methodologies Room: Carmel	

Notes

TUTORIALS
Carmel-Monterey

FULL DAY TUTORIAL
Monday, March 17, 2008
9:00am-5:30pm

Advanced Technology & Design Solutions in Design for Manufacturing Era

Chair & Moderator:
Rajiv Joshi, IBM T J Watson Research Center, NY

Presenters:
K. Maitra, AMD
Chris Kim, University of Minnesota
Robert Jones, Freescale
Subhasish Mitra, Stanford University
Hillary Hunter , IBM
Praveen Elakkumanan ,IBM

Tutorial 1
9:00am-10:15am

The promise of high-κ/metal gates – From electronic transport phenomena to emerging device/circuit applications

Presenter:
K. Maitra, AMD

Recent advancements of gate stack engineering have enabled the introduction of high-k/metal gates into mainstream CMOS device applications for 45 nm and beyond technology space. In this talk, we take a critical look back into the key steps which made this possible with primary focus on transport phenomena in transistors in presence of high-k/metal gates. Against this backdrop, the interaction of high-k/metal gates with end of roadmap devices would be thoroughly explored. High-k/metal gates have interesting ramifications in the circuit space-from NBTI (negative bias temperature instability) to high-field mobility, the high-k gate induced physical phenomena and their impact on device and circuit performance and reliability would be discussed. To conclude, this talk would also conjecture on the continued scalability of high-k gate stacks for futuristic CMOS device architectures.

Tutorial 2
10:15am-11:30am

Low Voltage Circuit Design Techniques for Sub-32nm Technologies

Presenter:
Chris Kim, University of Minnesota

In order to continue CMOS scaling towards the physical limit, care must be taken to account for each obstacle that is currently impeding our progress. Increased power consumption and faster current transients have deteriorated on-chip power supply integrity. Long term reliability issues such as Negative Bias Temperature Instability (NBTI) have become serious problems degrading the performance and yield of high performance systems. This talk will focus on circuit design techniques to deal with power supply noise and aging issues in sub-32nm technologies.

First, we will present modeling and design techniques for reliable on-chip power supply delivery. Next, an overview of several reliability mechanisms will be given followed by some recent developments on monitoring techniques to accurately measure and model the circuit aging impact.

Tutorial 3
11:30am-12:45pm

Process Technology Development and New Design Opportunities in 3D Integration Technology

Presenter:
Robert E. Jones, *Freescale*

3D integration offers inter-strata interconnect with high connectivity density, low parasitics, and shorter lengths. This bring advantages in increased interconnect bandwidth, reduced interconnect latency and reduced power consumption in comparison with individual packaged chips on a board or packages with wire bonded stacked die. 3D integration can compete with, or even surpass, SoC (system on a chip) integration in terms of interconnect performance while allowing for differentiated process technologies for the various strata.

The key process technologies for 3D integration are (1) bonding of strata, (2) inter-strata electrical connections, (3) through strata vias (TSVs), and (4) strata thinning and thin strata handling. A number of techniques had been explored for each of these key processes, and there various schemes for their order of integration. The major options for integration architecture are wafer-to-wafer, die-to-wafer, and die-to-die. The choice of architecture interacts with device application needs and device costs as well as the required process technologies. Wafer-to-wafer has the advantage of bonding a large number of die in parallel and in providing a planar surface for subsequent processing. Die-to-wafer (or die-to-die) has advantages in offering the ability to combine die of different areas and to integrate known good die while having the disadvantage of being a serial process

A number of design issues and opportunities arise for 3D integration. A primary design architecture decision is how to partition the overall system between strata. A simple partitioning strategy is to have a different circuit on each stratum (e.g. memory on logic). Finer partitioning is required at the IP block level which generally are connected by global interconnect. More complex partitioning could be within an IP block or even within the logic, memory or imager cell level. In addition to requiring higher TSVs and inter-strata connections, a finer partitioning will usually require more advanced 3D design tools including routing, layout, and verification. Additionally, it will also tend to make testing of individual die more difficult. By its nature 3D integration reduces the overall surface area/circuit area, and thus can further constrain thermal and electrical connectivity to the package. Thermal aware design tools may be needed to minimize stacking of hot spots on top of each other. 3D integration can reduce overall power requirements by reducing interconnect lengths and parasitics. In comparison with SiP integration, 3D can utilize lower voltages for circuit-to-circuit signals to further reduce power and latency. Adding the third dimension to layout opens up new opportunities for the design to reduce critical signal path lengths. When 3D integration is used to fabricate complex systems there will be an additional emphasis on improving built-in self-test and repair. 3D integration is expected to move to volume production in the near future for imagers and stacked memories and later to memory on logic applications. While some applications may select 3D for performance advantages or for reduced form factor, most product applications will be interested in 3D integration which is cost effective. 3D integration by its nature involves additional process costs for the 3D specific features and bonding. However, 3D offers potential savings over SoC integration through (1) process differentiation, and (2) ability to assemble known good die. The most advantageous systems for 3D integration will be those for which these savings outweigh the added process costs.

Tutorial 4
1:15pm-2:30pm

Robust System Design in Scaled CMOS

Presenter:
Subhasish Mitra, *Stanford University*

Our central vision is: Develop enabling technologies and tools spanning multiple abstraction levels to design globally optimized robust systems without incurring the high cost of traditional redundancy. Specific ideas that will be discussed include:

- Built-In-Soft-Error Resilience: An architecture-aware circuit design technique corrects radiation-induced soft errors in latches, flip-flops, and combinational logic at extremely low-cost compared to redundancy techniques;

- Circuit failure prediction and self-correction: A new design technique, distinct from error detection, predicts failures before they actually create errors in system data and states. Circuit failure prediction is ideal for reliability mechanisms such as transistor aging and early-life failures, and can enable close to best-case design by minimizing traditional worst-case speed guard bands.

Tutorial 5
2:30-3:45pm

Caches in the Many-Core Era: What Purpose Might eDRAM Serve?

Presenter:
Hillary Hunter , *IBM*

Choosing data storage arrays for a microprocessor design is driven by a delicate balance of technology readiness, circuit-level design factors, and system-level performance, power, and scaling implications. Recently, CMOS technologists have warned of the "end of scaling," and cite particular concern for six-transistor SRAM. This is a startling forecast, since easily 50% of microprocessor silicon area is commonly occupied by SRAM caches. A particularly long-standing debate has surrounded one dense, resilient, on-chip storage alternative: embedded DRAM. This tutorial will provide background on eDRAM, and show how its circuit and technology properties translate to metrics used to make decisions at the chip and architecture levels: cache capacity, cache access latency, and cache distance from the CPU.

Tutorial 6
4:00pm-5:15pm

Enhancing Yield through Design for Manufacturability (DFM)

Presenter:
Praveen Elakkumanan, Rajiv Joshi, IBM

This part of the tutorial will discuss in detail the manufacturing challenges in nanoscale VLSI and consequent Design for Manufacturability (DFM) approaches by taking a holistic approach in analyzing and addressing different process variability effects. We review the dominant process variations in semiconductor manufacturing process that affect the design yield, show their impact on layout quality, and present currently practiced DFM techniques to mitigate the effect of these variations. We also discuss various manufacturing-aware physical and circuit design methodologies and techniques for parametric yield improvement. This includes correct-by-construction methodologies such as Restricted Design Rules (RDRs) as well as manufacturing aware design approaches. In addition, we will briefly mention some of the many accepted and possible mitigation techniques in design post processing (after tape-out) and will introduce the concept of Manufacturing for Design (MFD) through design-intent processing.

Evening Panel Discussion
Sponsored by Ponte Solutions

Monday March17, 2008
6:30pm-8:30pm

DFM: Is it Helping or Hurting?

Moderator
Ron Wilson
Executive Editor, EDN

Organizer
Michael Buehler Garcia
Ponte Solutions

Description
No question, DFM adds to designer's workload, generating reams of data that point to possible errors, but doesn't directly fix them. What does a designer do with all that information? Can it be used as a competitive 'lever,' telling designers how far they can push a design without a creating manufacturing disaster? Or is DFM ignorance bliss?

Panelists:
Dr. Ara Markosian, *CTO, Ponte Solutions*
Walter Ng, Vice President, *Design Enablement Alliances. Chartered Semiconductor Manufacturing*
Dr. Yervant Zorian, *Vice President and Chief Scientist, Virage Logic Corporation*
Dr. Riko Radojcic, *Leader of Design-for-Si initiatives, Qualcomm CDMA Technologies*
Tim Horel, *Senior Director of Hardware Operation, M2000, Inc.*
Richard Brashears, *Corporate Vice President, Manufacturing Modeling and Implementation Technology, Cadence Design Systems*

KEYNOTE SPEECHES
Plenary Session 1P
Sponsored by Mentor Graphics
Tuesday March 18
9:00am-10:15am

Session Chairs:
Tanay Karnik
Intel

Kris Verma
Silicon Valley Technical Institute

Session Moderator:
Dr. Chi-Foon Chan
President& COO, Synopsys

Keynote Speech 1P.1
Tuesday, March 18
9:15am-9:45am

Shrinking time-to-market through global value chain integration

Drew Gude
Director, High Tech&Electronics Industry Solutions
Microsoft Corporation

The product development challenges for high-tech companies are even greater than most industries, thanks in large part to their dependence on an increasingly distributed and complex global value chain and extreme pressure to deliver innovation to market quicker than their fierce competition. That chain of frequently independent companies collaborating on these shrinking project timelines stretches from product conception to chip design, product development, production, assembly, testing, packaging, and delivery. Central to addressing these challenges are solutions and interoperable IT enterprise architectures that can streamline this innovation pipeline. In this presentation Drew Gude of Microsoft discusses the opportunities to shrink product time-to-market by more quickly, efficiently, and securely collaborating and integrating with product development value chain partners.

Keynote Speech 1P.2
Tuesday, March 18
9:45am-10:15am

Bounding the Endless Verification Loop

Robert Hum
Vice President & General Manager, Design Verification and Test Division
Mentor Graphics Corporation

Although more and more engineering resources are being focused on verification, most of the effort is expended on re-simulating what has already been simulated. And once the effort is through, only 20% of the state space has been verified, at best. Verification today is a frustrating, open-loop process that often doesn't end even after the integrated circuit ships. In response, the whole verification methodology infrastructure is undergoing major changes—from adoption of assertion-based verification, coverage-driven verification, to new approaches in test bench generation/optimization, integrated hardware acceleration and more. In this session, Robert Hum will explore these and other new solutions and innovations in functional verification technology, and discuss the impact of these changes on the EDA industry.

SESSION 1A
Embedded Tutorial
Tuesday March 18
10:30am-12:00noon
Room: San Jose

SOC verification

Moderator:
Diana Ragget -Javelin Design Automation

Overview:
The complexity of current SOCs requires extensive engineering manpower and schedule allocation if feasibility and verification is left to the end of the program cycle. This tutorial will address several methods of early design phase verification and the resulting tradeoffs in the design and verification flow.

Tutorial 1A.1
Tuesday, March 18
10:30am-11:15am

Managing early design feasibility issues through system physical prototyping

Koko Mihan
Javelin Design Automation

Tutorial 1A.2
Tuesday, March 18
11:15am-12:00pm

Innovations in Functional Verification Technology

Kenneth Larsen
Mentor Graphics

SESSION 1B
Tuesday March 18
10:30am-12:00noon
Room: Santa Clara

Power Conscious Memories

Chair: **Dinesh Somasekhar**
Co-Chair: **Haibo Wang**

10:30AM
1B.1
A Radiation Hardened Nano-power 8Mb SRAM in 130nm CMOS

Mark Lysinger[1], Francois Jacquet[2], David Mcclure[1], Philippe Roche[2], Mehdi Zamanian[1], Naren Sahoo[1], John Russell[1]
[1]STMicroelectronics, Carrollton, USA, [2]STMicroelectronics, Crolles, France

11:00AM
1B.2
Error-Tolerant SRAM Design for Ultra-Low Power Standby Operation

Huifang Qin[1], Animesh Kumar[1], Kannan Ramchandran[1], Jan Rabaey[1], Prakash Ishwar[2]
[1]University of California, Berkeley, [2]Boston University

11:20AM
1B.3
Error Protected Data Bus Inversion Using Standard DRAM Components

Maurizio Skerlj[1] and Paolo Ienne[2]
[1]Qimonda AG, [2]EPFL

11:40AM
1B.4
Process Variation Aware Bus-coding scheme for Delay Minimization in VLSI Interconnects

Raghunandan Chittarsu, Sainarayanan K S, Srinivas M B
IIIT Hyderabad

SESSION 1C
Tuesday March 18
10:30am-12:00noon
Room: Monterey

Speed-up and Timing of Integrated Circuits

Chair: **Masahiro Fujita**
Co-Chair: **Peter Oshea**

10:30AM
1C.1
Speed-up of ASICs derived from FPGAs by Transistor Network Synthesis Including Reordering
Tiago Cardoso[1], Leomar Rosa Jr.[1], Felipe Marques[1], Renato Ribas[1], Andre Reis[2]
[1]UFRGS, [2]Nangate

11:00AM
1C.2
Fast and Accurate Waveform Analysis with Current Source Models
Vineeth Veetil, Dennis Sylvester, David Blaauw
University of Michigan

11:20AM
1C.3
An Efficient Method for Fast Delay and SI Calculation Using Current Source Models
Xin Wang, Ali Kasnavi, Harold Levy
Synopsys Inc.

11:40AM
1C.4
Adaptive Stochastic Collocation Method (ASCM) for Parameterized Statistical Timing Analysis with Quadratic Delay Model
Yi Wang[1], Xuan Zeng[1], Wei Cai[2], Hengliang Zhu[1], Xu Luo[1]
[1]State Key Lab. of ASIC & System, Microelectronics Dept., Fudan University, [2]Depart. of Mathematics, University of North Carolina at Charlotte

SESSION 1D
Tuesday March 18
10:30am-12:00noon
Room: Carmel

SER and Noise Tolerance

Chair: **Keith Bowman**

Co-Chair: **Yu Cao**

10:30AM

1D.1

Combinational Logic Circuit Protection Using Customized Error Detecting and Correcting Codes

Avijit Dutta[1] and Abhijit Jas[2]

[1]Mentor Graphics, [2]Intel Corp

11:00AM

1D.2

Output Remapping Technique for Soft-Error Rate Reduction in Critical Path

Qian Ding, Yu Wang, Hui Wang, Rong Luo, Huazhong Yang

Tsinghua University, Beijing

11:20AM

1D.3

IR Drop Reduction via a Flip-Flop Resynthesis Technique

Tsung-Yi Wu, Jiun-Kuan Wu, Liang-Ying Lu, Kuang-Yao Chen, Meng-Lin Xie

National Changhua University of Education

11:40AM

1D.4

Noise Interaction Between Power Distribution Grids and Substrate

Daniel A. Andersson[1], Simon Kristiansson[2], Kjell O. Jeppson[2], Lars 'J' Svensson[2], Per Larsson-Edefors[2]

[1]Department of Computer Science and Engineering, Chalmers University of Technology, [2]

ISQED Luncheon
Sponsored by Synopsys
Tuesday March 18
12:00pm-1:30pm

ISQED'08 Award Ceremony
Best Paper Awards
Sponsored by Magma Design Automation, and Synopsys

ISQED Fellow Awards

ISQED Quality Award (IQ-Award 2008)
Sponsored by Microsoft Corporation

Luncheon Keynote Speech
Tuesday, March 18
12:45pm-1:30pm

EDA Is Truly Where Electronics Quality Begins!

Dr. Antun Domic
Senior VP and GM, Synopsys, Inc.

The trillion-dollar electronics industry is undoubtedly the fastest growing and most innovative industry in history. Two electronic products which illustrate well the dramatic growth and innovation over the last ten years are the cell phone and the personal computer. In 1996, cell phones were the third most commonly sold electronic product, after PCs and TVs. That year, the electronics industry sold 60 million cell phones, 65 million PCs, and 120 million TVs worldwide. In 2006, the electronics industry has sold a record one billion cell phones, 230 million PCs, and 180 million TVs. In 1996 a desktop PC running Windows 95 had a minimum system requirement of 33MHz of processor clock rate and 4 MB of memory. In 2006, to be Windows Vista ready, a PC had a minimum system requirement of 1GHz of processor clock rate and 1 GB of memory. From Pentium 5.5 millions of transistors at 350 nanometers to 291 million of Core 2 Duo at 65 nanometers, from 150 MHz to 3.7 GHz, and from 30 Watts to 115 Watts, eight generations of Intel's processors have happened in approximately 10 years—a new generation every 15 months. Electronic products and their core components, the integrated circuits, innovate at an amazingly, and increasingly rapid, pace, becoming exponentially more complex and feature rich with each new generation introduction. In order to keep up with this brisk pace, the electronics — and semiconductor — industries rely more and more heavily on electronic design automation (EDA) tools. The seemingly insatiable appetite of consumers for more fully featured, higher quality, faster, and yet cheaper electronic products drives the semiconductor industry to

produce increasingly smaller, faster, and complex ICs, and drives the EDA industry to produce increasingly ingenious tools to design them. The EDA industry is constantly striving to keep the pace of technology evolution, spending an average 25% of its revenue in research and development, far above the enterprise software and semiconductor industry sectors, even above the pharmaceutical sector, which is often used as a reference point. It provides its customers with always higher quality tools, both in terms of raw performance (capacity, runtime) and additional features required to address the smaller geometries of the newest technology generations. A good example of these tools' quality improvement is the performance improvement, qualitative and quantitative, undergone by logic synthesis from 1996 until today: in 2007, running the same RTL through logic synthesis not only requires less than half of 1% of the runtime and 3X less memory than it required in 1996, but it also leads to a 40% smaller and 40% faster implementation. In this keynote, like an epic by Virgil, Dr. Domic will guide today's Dantes through the realms of 45 and 32 nanometers, describing the enormous — and yet partly unexplored! — arsenal of weapons that EDA has made, and continues to make, available for the courageous users that are rushing to 45 and 32 nanometers and beyond, as well as for those who decide to stay at 90 and 130 nanometers or higher, also addressing the implications of reduced processor clock rates and the availability of affordable multi-processors.

SESSION 2A
Tuesday March 18
1:30pm-3:30pm
Room : San Jose

Robust SRAM and Analog Circuits

Chair: **Masanori Hashimoto**

Co-Chair: **David Pan**

1:30PM

2A.1

Fundamental Data Retention Limits in SRAM Standby -- Experimental Results

Animesh Kumar[1], Huifang Qin[1], Prakash Ishwar[2], Jan Rabaey[1], Kannan Ramchandran[1]
[1]EECS, University of California, Berkeley, CA, [2]ECE, Boston University, Boston, MA

2:00PM

2A.2

Quality of a Bit (QoB): A New Concept in Dependable SRAM

Hidehiro Fujiwara, Shunsuke Okumura, Yusuke Iguchi, Hiroki Noguchi, Yasuhiro Morita, Hiroshi Kawaguchi, Masahiko Yoshimoto
Kobe University

2:30PM

2A.3

Cache Design for Low Power and High Yield

Baker Mohammad[1], Martin Saint Laurent[1], Paul Bassett[2], Jacob Abraham[2]
[1]Qualcomm, [2]The University of Texas at Austin

2:50PM

2A.4

Projection-Based Piecewise-Linear Response Surface Modeling for Strongly Nonlinear VLSI Performance Variations

Xin Li[1] and Yu Cao[2]

[1]Carnegie Mellon University, [2]Arizona State University

3:10PM

2A.5

High Output Resistance and Wide Swing Voltage Charge Pump Circuit

Tian Xia[1], Stephen Wyatt[2]

[1]University of Vermont, [2]IBM

SESSION 2B
Tuesday March 18
1:30pm-3:30pm
Room*:* Santa Clara

Power and Thermal Management

Chair: **Mark Budnik**

Co-Chair: **Sarma Vrudhala**

1:30PM

2B.1

Interconnect Signaling and Layout Optimization to Manage Thermal Effects Due to Self Heating in On-Chip Signal Buses

Krishnan Sundaresan[1] and Nihar Mahapatra[2]

[1]Sun Microsystems, Inc., [2]Michigan State University

2:00PM

2B.2

A Low-Power Double_Edge_Triggered Address Pointer Circuit for FIFO Memory Design

Saravanan Ramamoorthy[1], Haibo Wang[1], Sarma Vrudhula[2]

[1]Southern Illinois University, Carbondale, [2]Arizona State University, Tempe

2:30PM

2B.3

Minimizing Offset for Latching Voltage-Mode Sense Amplifiers for Sub-threshold Operation

Joseph Ryan and Benton Calhoun

University of Virginia

2:50PM

2B.4

Dependence of Minimum Operating Voltage (VDDmin) on Block Size of 90-nm CMOS Ring Oscillators and Its Implications in Low Power DFM

Taro Niiyama[1], Piao Zhe[1], Koichi Ishida[1], Masami Murakata[2], Makoto Takamiya[1], Takayasu Sakurai[1]

[1]University of Tokyo, [2]STARC

3:10PM

2B.5

Accurate Temperature Estimation for Efficient Thermal Management

Shervin Sharifi, Chunchen Liu, Tajana Rosing

University of California, San Diego

SESSION 2C
Tuesday March 18
1:30pm-3:30pm
Room: Carmel

Process Variations

Chair: **Murat Becer**

Co-Chair: **He Jin**

1:30PM

2C.1

Process Variation Aware Timing Optimization through Transistor Sizing in Dynamic CMOS Logic

Kumar Yelamarthi and Henry Chen

Wright State University

2:00PM

2C.2

Compact Variation-Aware Standard Cell Models for Timing Analysis -- Complexity and Accuracy Analysis

Seyed-Abdollah Aftabjahani and Linda Milor

Georgia Institute of Technology

2:30PM

2C.3

A Statistical Characterization of CMOS Process Fluctuations in Subthreshold Current Mirrors

Lei Zhang, Zhiping Yu, Xiangqing He

Institute of Microelectronics, Tsinghua University

2:50PM

2C.4

Robust Estimation of Timing Yield with Partial Statistical Information on Process Variations

Lin Xie and Azadeh Davoodi

University of Wisconsin

3:10PM

2C.5

Variation Aware Spline Center and Range Modeling for Analog Circuit Performance

Shubhankar Basu, Balaji Kommineni, Ranga Vemuri

University of Cincinnati

SESSION 2D
Embedded Tutorial
Tuesday March 18
2:00pm-3:00pm
Room: Siskiyou-Cascade-Sierra

How to Determine Best DFM Practices

Moderator:
David Overhauser

Overview:
In this tutorial, there will be presentation of a methodology to ascertain the relative effectiveness of various DFM practices using results from volume diagnostics. Presently, rapid bring-up of semiconductor products is hampered by design and manufacturing interactions, commonly referred to as systematic defects. Moreover, today's designs and process technology present those responsible for yield ramp with the challenge of determining the root cause of complex failures caused by voltage drop, signal cross-coupling and parasitic variations. A typical 45nm and beyond design flow will primarily consist of 3 stages – build, verify and correct. From a DFM standpoint, the build stage incorporates manufacturing know-how and limitations such that performance and yield entitlement can be achieved. However, even with such a "correct-by-construction" mindset it is necessary to verify and detect potential areas of yield or functionality concerns. These detected "hot spots" can then be used to correct and optimize the design. Present day complex and demanding designs may go through this flow iteratively until an acceptable level of DFM-cleanliness is achieved. In spite of this design methodology, a product in silicon still demonstrates marginalities and consequently yields or performance issues due to undesirable design-process interactions. The tutorial will explain how correlating volume diagnostic results with DFM applications can be an effective and efficient means of locating such "problem areas" and can help provide design-specific marching orders to manufacturing for mitigating systematic defects.

Speakers

Tom Jackson
Product Marketing Director, Encounter Test
Cadence Design Systems, Inc.

Milind Weling
Engineering Director, Sign-off and Silicon Optimization
Cadence Design Systems, Inc.

SESSION E1
Tuesday March 18
1:30pm-5:30pm
Location: Bayshore Foyer

Embedded Technical Session
Poster Session

Chair: **He Jin**
Co-Chair: **Miroslav Velev**

E1.1
A Dual Oxide CMOS Universal Voltage Converter for Power Management in Multi-V_{DD} SoCs
Dhruva Ghai, Saraju Mohanty, Elias Kougianos
University of North Texas

E1.2
Dominant Substrate Noise Coupling Mechanism for Multiple Switching Gates
Emre Salman[1], Eby Friedman[1], Radu Secareanu[2], Olin Hartin[2]
[1]University of Rochester, [2]Freescale Semiconductor

E1.3
A Statistic-based Approach to Testability Analysis
Chuang-Chi Chiou, Chun-Yao Wang, Yung-Chih Chen
National Tsing Hua University

E1.4
Generic Carrier-Based Core Model for Undoped Four-Terminal Double-Gate MOSFET Valid for Symmetric, Asymmetric, SOI, and Independent Gate Operation Modes
feng liu[1], jin he[1], wei bian[1], yue fu[1], jie feng[1], xing zhang[1], mansun chan[2]
[1]institute of Microelectronics, peking university, [2]ECE, Hongkong university of Science and technology

E1.5
On the Feasibility of Obtaining a Globally Optimal Floorplanning for an L-shaped Layout Problem
Tsu-Shuan Chang[1], Manish Kumar[2], Teng-Sheng Moh[3], Chung-Li Tseng[4]
[1]University of California, Davis, [2]University of Missouri-Rolla, [3]San Jose State University, [4]University of New South Wales, Sydney

E1.6
Architecting for Physical Verification Performance and Scaling
John Ferguson and Robert Todd
Mentor Graphics

E1.7

Efficient Thermal Aware Placement Approach Integrated With 3D DCT Placement Algorithm

Haixia Yan, Qiang Zhou, Xianlong Hong

Computer Science and Technology Department,Tsinghua University

E1.8

CMOS based low cost Temperature Sensor

Neehar Jandhyala, Lili He, Morris Jones

San Jose State University

E1.9

An SSO Based Methodology for EM Emission Estimation from SoCs

Jairam S[1], Stalin S.M[1], Jean-Yves Oberle[2], Udayakumar H[1]

[1]TI India, [2]TI France

E1.10

Statistical Data Stability and Leakage Evaluation of FinFET SRAM Cells with Dynamic Threshold Voltage Tuning under Process Parameter Fluctuations

Zhiyu Liu, Sherif Tawfik, Volkan Kursun

UW-Madison

E1.11

Characterization of New Static Independent-Gate-Biased FinFET Latches and Flip-Flops under Process Variations

Sherif Tawfik and Volkan Kursun

University of Wisconsin-Madison

E1.12

A Low Energy Two-step Successive Approximation Algorithm for ADC design

Ricky Yiu-kee Choi and Chi-ying Tsui

The Hong Kong University of Science and Technology

E1.13

Automated Specific Instruction Customization Methodology for Multimedia Processor Acceleration

Kang Zhao[1], Jinian Bian[1], Sheqin Dong[1], Yang Song[2], Satoshi Goto[2]

[1]Tsinghua University, China, [2]Waseda University, Japan

SESSION 2E
Tuesday March 18
1:30pm-3:30pm
Room: Siskiyou-Cascade-Sierra

Embedded Technical Session
Poster session with oral presentation by authors

Chair: **Jayanta Bhadra**
Co-Chair: **Syed M Alam**

1:30PM
2E.1
Process Variability Analysis in DSM Through Statistical Simulations And Its Implications To Design Methodologies
Srinivasa R STG, Srivatsava Jandhyala, Tondamuthuru R Narahari
Intel

1:34PM
2E.2
Parasitic Aware Process Variation Tolerant Voltage Controlled Oscillator (VCO) Design
Dhruva Ghai, Saraju Mohanty, Elias Kougianos
University of North Texas

1:38PM
2E.3
Evaluation of the PTSI Crosstalk Noise Analysis Tool and Development of an Automated Spice Correlation Suite to Enable Accuracy Validation
Venugopal Chakravarthy[1], Jagganath Rao[1], Prashanth Soraiyur[2]
[1]S J College of Engg, Mysore-6, [2]TI (India), Banga;lore

1:42PM
2E.4
Hotspot Based Yield Prediction with Consideration of Correlations
Qing Su, Charles Chiang, Jamil Kawa
Synopsys

1:46PM
2E.5
A Randomized Greedy Algorithm for the Pattern Fill Problem for DFM Applications
Maharaj Mukherjee[1] and Kanad Chakraborty[2]
[1]IBM Corporation, [2]Cypress Semiconductor Corporation

1:50PM

2E.6

A Passive 915 MHz UHF RFID Tag

José Palma, César Marcon, Fabiano Hessel, Eduardo Bezerra, Guilherme Rohde, Carlos Reif, Luciano Azevedo, Carolina Metzler

PUCRS

1:54PM

2E.7

Crosstalk noise variation assessment and analysis for the worst process corner

Jae-Seok Yang and Andrew Neureuther

UC Berkeley

1:58PM

2E.8

DFM Based Detailed Routing Algorithm for ECP and CMP

Yin Shen, Yici Cai, Qiang Zhou, Xianlong Hong

Department of Computer Science and Technology, Tsinghua University

2:02PM

2E.9

Instruction Scheduling for Variation-originated Variable Latencies

Toshinori Sato[1] and Shingo Watanabe[2]

[1]Kyushu University, [2]Kyushu Institute of Technology

2:06PM

2E.10

Hotspot Prevention Using CMP Model in Design Implementation Flow

Norma Rodriguez[1], Li Song[2], Shishir Shroff[2], Kunanghan Chen[2], Taber Smith[2], Wilbur Luo[2]

[1]AMD, [2]Cadence

2:10PM

2E.11

The Statistical Failure Analysis for the Design of Robust SRAM in nano-scale Era

Young-Gu Kim, Soo-Hwan Kim, Hoon Lim, Sanghoon Lee, Keun-Ho Lee, Young-Kwan Park, Moon-Hyun Yoo

Samsung Electronics Co. Ltd

2:14PM

2E.12

Computation of Waveform Sensitivity using Geometric Transforms for SSTA

Ratnakar Goyal, Harindranath Parameswaran, Sachin Shrivastava

Cadence Design Systems

2:18PM

2E.13

On Efficient and Robust Constraint Generation for Layout Legalization

Sambuddha Bhattacharya[1], Shabbir Batterywala[1], Subramaniam Rajagopalan[1], Tony Ma[2], Narendra Shenoy[2]
[1]Synopsys (India) Pvt. Ltd., [2]Synopsys Inc.

2:22PM

2E.14

Feedback-Switch Logic (FSL): A High-Speed Low-Power Differential Dynamic-Like Static CMOS Circuit Family

Charbel Akl and Magdy Bayoumi
university of louisiana at lafayette

2:26PM

2E.15

Analysis of System-Level Reliability Factors and Implications on Real-time Monitoring Methods for Oxide Breakdown Device Failures

Eric Karl, David Blaauw, Dennis Sylvester
University of Michigan

2:30PM

2E.16

Characterizing the Impact of Substrate Noise on High-Speed Flash ADCs

Parastoo Nikaeen, Boris Murmann, Robert Dutton
Stanford University

2:34PM

2E.17

Analytical Noise-Rejection Model Based on Short Channel MOSFET

Vinay Jain[1] and Payman Zarkesh-Ha[2]
[1]IIT Kanpur, India, [2]University of New Mexico, Albitqueruqe, NM

2:38PM

2E.18

A High-Performance Bus Architecture for Strongly Coupled Interconnects

Michael N Skoufis[1], Kedar Karmarkaran[1], Themistoklis Haniotakis[2], Spyros Tragoudas[1]
[1]Southern Illinois University, [2]University of Patras

2:42PM

2E.19

A Fully Integrated 2.4 GHz Mismatch-Controllable RF Front-end Test Platform in 0.18μm CMOS

Zahra sadat Ebadi and Resve Saleh
University of British Columbia

2:46PM

2E.20

A Holistic Approach to SoC Verification

Alicia Strang[1], David Potts[1], Shankar Hemmady[2]

[1]Marvell Semiconductor, [2]Synopsys

2:50PM

2E.21

A Robust and Efficient Pre-Silicon Validation Environment for Mixed-Signal Circuits on ####### Test Chips

Nathaniel August

Intel Corporation

2:54PM

2E.22

Hybrid Integration of Bandgap Reference Circuits using Silicon ICs and Germanium Devices

Jae Wook Kim, Boris Murmann, Robert Dutton

Stanford University

2:58PM

2E.23

VERIFICATION OF IP-CORE BASED SoC's

Anil Deshpande

Conexant Systems

3:02PM

2E.24

Innovative Test Solutions for Pin-Limited Microcontrollers

Matthew Stout and Kenneth Tumin

Freescale Semiconductor

3:06PM

2E.25

XStatic: A Simulation based ESD Verification and Debug environment

Ganesh Shamnur and Rajesh Berigei

National Semiconductor Corporation

3:10PM

2E.26

Statistical Crosstalk Noise Analysis Using First Order Parameterized Approach for Aggressor Grouping

Sachin Shrivastava and Harindranath Parameswaran

Cadence Design Systems, India

SESSION 3A
Tuesday March 18
3:45pm-5:45pm
Room : San Jose

System and Circuit Synthesis

Chair: **Sao-Jie Chen**
Co-Chair: **Fadi Kurdahi**

3:45PM
3A.1
High-quality Circuit Synthesis for Modern Technologies
Lech Jozwiak[1], Artur Chojnacki[2], Aleksander Slusarczyk[1]
[1]Eindhoven University of Technology, [2]PDF Solutions Inc.

4:15PM
3A.2
ILP based Gate Leakage Optimization using DKCMOS Library during RTL Synthesis
Saraju Mohanty
University of North Texas

4:45PM
3A.3
Improving the Efficiency of Power Management Techniques by Using Bayesian Classification
Hwisung Jung and Massoud Pedram
University of Southern California

5:05PM
3A.4
An On-Demand Test Triggering Mechanism for NoC-Based Safety-Critical Systems
Jason Lee, Nikhil Gupta, Praveen Bhojwani, Rabi Mahapatra
Texas A&M University

5:25PM
3A.5
Constant Rate Dataflow Model with Intermediate PortsforEfficient Code Synthesis with Top-down design and Dynamic Behavior
Hyunok Oh
ARM Inc.

SESSION 3B
Tuesday March 18
3:45pm-5:45pm
Room: Santa Clara

Process, Characterization and Temperature-aware Design

Chair: **James Lei**
Co-Chair: **Mark Budnik**

3:45PM
3B.1
Thermal-aware IR drop analysis in large power grid
Yu Zhong and Martin D. F. Wong
Univ. of Illinois at Urbana-Champaign

4:15PM
3B.2
A methodology for characterization of large macro cells and IP blocks considering process variations
Amit Goel[1], Sarma Vrudhula[1], Feroze Taraporevala[2], Praveen Ghanta[2]
[1]Arizona State University, [2]Synopsys Inc.

4:45PM
3B.3
Investigation of Process Impact on Soft Error Susceptibility of Nanometric SRAMs using a Compact Critical Charge Model
Shah M. Jahinuzzaman, Mohammad Sharifkhani, Manoj Sachdev
University of Waterloo

5:05PM
3B.4
Characterization of Standard Cells for Intra-Cell Mismatch Variations
Savithri Sundareswaran[1], Jacob Abraham[2], Alexandre Ardelea[1], Rajendran Panda[1]
[1]Freescale Semiconductor, [2]University of Texas at Austin

5:25PM
3B.5
Full-Chip Leakage Verification for Manufacturing Considering Process Variations
Tao Li and Zhiping Yu
Institute of Microelectronics, Tsinghua University

SESSION 3C
Tuesday March 18
3:45pm-5:45pm
Room: Carmel

Processor Test Verification / Delay Diagnosis

Chair: **Tao Feng**
Co-Chair: **Patra Priyadarshan**

3:45PM
3C.1
Processor Verification with hwBugHunt
Sangeetha Sudhakrishnan, Liying Su and Jose Renau
University of California, Santa Cruz

4:15PM
3C.2
Enhancing the Testability of RTL Designs Using Efficiently Synthesized Assertions
Mohammad Reza Kakoee, Mohammad Riazati, Siamak Mohammadi
Tehran University, IRAN

4:45PM
3C.3
Efficient Selection of Observation Points for Functional Tests
Jian Kang[1], Sharad Seth[1], Yi-Shing Chang[2], Vijay Gangaram[2]
[1]University of Nebraska - Lincoln, [2]Intel Corporation

5:05PM
3C.4
A Novel Test Generation Methodology for Adaptive Diagnosis
Rajsekhar Adapa, Edward Flanigan, Spyros Tragoudas
Southern Illinois University

5:25PM
3C.5
Timing-Aware Multiple-Delay-Fault Diagnosis
Vishal Mehta[1], Malgorzata Marek-Sadowska[1], Kun-Han Tsai[2], Janusz Rajski[2]
[1]University of California Santa Barbara, [2]Mentor Graphics Corporation

SESSION 3D
Embedded Panel Discussion

Tuesday March17, 20088
3:45pm-5:30pm
Room: Siskiyou-Cascade-Sierra

ESL 2.0- Is Anybody Using It 2.0?

Moderator
John Blyler
Editor in Chief, Chip Design Magazine

Organizer
Mindy Palmer
CoWare

Description
For years, the expectation was for ESL to be the next HDL before DFM came along. Now it is back at the top of the expectation list, being called ESL 2.0. But real customers are hard to find. So the question once again is: Who is using ESL and does anyone provide a tool that solves a problem? Is system design actually an activity as opposed to a issue that needs a solution?

Panelists:
Marc Serughetti, *CoWare*
Bill Neifert, *CTO, Carbon Design Systems*
Grant Martin, *Chief Scientist, Tensilica*
Kees Vissers, *Principal Engineer, Xilinx*
Alain Raynaud, *Technology Center Director, EVE*
Robert Barker, *Vice President Business Development, ElementCXI*

SESSION 3E
Tuesday March 18
3:45pm-5:45pm
Room: Siskiyou-Cascade-Sierra

Embedded Technical Session
Poster session with oral presentation by authors

Chair: **Andre Reis**
Co-Chair: **Anand Iyer**

3:45PM
3E.1
Cell Swapping Based Migration Methodology for Analog and Custom Layouts
Shabbir Batterywala[1], Sambuddha Bhattacharya[1], Subramanian Rajagopalan[1], Tony Ma[2], Narendra Shenoy[2]
[1]Synopsys (India) Pvt. Ltd., [2]Synopsys Inc.

3:49PM
3E.2
a knowledge-based tool for generating and verifying hardware-ready embedded memory models
Paul Cheng
Cadence Design Systems

3:53PM
3E.3
"System Verilog for Quality of Results (QoR)"
Ravi Surepeddi
Magma Design Automation Inc

3:57PM
3E.4
Power Delivery System: Sufficiency, Efficiency, and Stability
Zhen Mu
Cadence Design Systems, Inc.

4:01PM
3E.5
Thermal Aware Global Routing of VLSI Chips for Enhanced Reliability
Aseem Gupta[1], Fadi Kurdahi[1], Nikil Dutt[1], Kamal Khouri[2], Magdy Abadir[2]
[1]University of California Irvine, [2]Freescale Seminconductor

4:05PM

3E.6

Clock Skew Analysis via Vector-Fitting in Frequency Domain

Ling Zhang[1], Haikun Zhu[2], Wanping Zhang[2], Wenjian Yu[3], Chung-Kuan Cheng[1]

[1]UCSD, [2]Qualcomm, [3]Tsinghua University

4:09PM

3E.7

An Approach for A Comprehensive QA methodology for the PDKs

Sridhar Joshi, Ravi Perumal, Kamesh Gadepally, Mark Young

National Semiconductor Corporation

4:13PM

3E.8

Strategies for Quality CAD PDKs

Kamesh Gadepally, Mark Young, James Lin, Andy Franklin, Ravi Perumal, Sridhar Joshi

National Semiconductor Corporation

4:17PM

3E.9

Variability Analysis for Sub-100 nm PD/SOI Sense-Amplifier

Saibal Mukhopadhyay[1], Rajiv Joshi[2], Keunwoo Kim[2], Ching-Te Chuang[2]

[1]Georgia Institute of Technology, [2]IBM T. J. Watson Research Center

4:21PM

3E.10

Predictive Delay Evaluation on Emerging CMOS Technologies: A Simulation Framework

Manuel SELLIER[1], Jean-Michel PORTAL[2], Bertrand BOROT[1], Steve COLQUHOUN[1], Richard FERRANT[1], Frédéric BŒUF[1], Alexis FARCY[1]

[1]STMicroelectronics, [2]L2MP

4:25PM

3E.11

Process Variation Characterization and Modeling of Nanoparticle Interconnects for Foldable Electronics

Rasit Onur Topaloglu

University of California at San Diego

4:29PM

3E.12

A Simplified Model of Carbon Nanotube Transistor with Applications to Analog and Digital Design

Saurabh Sinha, Asha Balijepalli, Yu Cao

Arizona State University

4:33PM

3E.13

Adaptive Branch and Bound using SAT to Estimate False Crosstalk

Murthy Palla[1], Jens Bargfrede[1], Klaus Koch[1], Walter Anheier[2], Rolf Drechsler[2]

[1]Infineon Technologies AG, Munich, [2]University of Bremen, Bremen

4:37PM

3E.14

Minimum Shield Insertion on Full-Chip RLC Crosstalk Budgeting Routing

Peng-Yang Hung, Ying-Shu Lou, Yih-Lang Li

National Chiao-Tung University

4:41PM

3E.15

Clock Skew Evaluation Considering Manufacturing Variability in Mesh-Style Clock Distribution

Shinya Abe, Masanori Hashimoto, Takao Onoye

Osaka University

4:45PM

3E.16

A Novel Cell-Based Heuristic Method for Leakage Reduction in Multi-Million Gate VLSI Designs

Sandeep Gupta, Jaya Singh, Abhijit Roy

Texas Instruments(India) Pvt Ltd

4:49PM

3E.17

Study on the Silicon-Germanium Nanowire MOSFETs with the Core-Shell Structure

Yue Fu, Jin He, Feng Liu, Jian Zhang, Lining Zhang, Xing Zhang

The Hub of Multi-Project-Wafer(MPW), School of Electronic Engineering and Computer Science, Peking University, Beijing 100871,P.R. China

4:53PM

3E.18

Elastic Timing Scheme for Energy-Efficient and Robust Performance

Rupak Samanta[1], Ganesh Venkataraman[2], Nimay Shah[1], Jiang Hu[1]

[1]Texas A&M University, [2]Magma

4:57PM

3E.19

Statistical Models and Frequency-Dependent Corner Models for Passive Devices

Ning Lu

IBM

5:01PM

3E.20

A thermal-friendly load-balancing technique for multi-core processors

Enric Musoll

ConSentry Networks

5:05PM

3E.21

Analytical Model for the Propagation Delay of Through Silicon Vias

DiaaEldin Khalil[1], Yehea Ismail[1], Muhammad Khellah[2], Tanay Karnik[2], Vivek De[2]

[1]EECS Department, Northwestern University, [2]Circuits Research Lab, Intel Corporation

5:09PM

3E.22

Sampling Error Estimation in High-Speed Sampling Systems Introduced by the Presence of Phase Noise in the Sampling Clock

Salam Marougi

Agilent Technologies

5:13PM

3E.23

A QoS Scheduler for Real-Time Embedded Systems

David Matschulat, César Marcon, Fabiano Hessel

PUCRS

5:17PM

3E.24

FPGA-Based 1.2 GHz Bandwidth Digital Instantaneous Frequency Measurement Receiver

Henry Chen

WSU

5:21PM

3E.25

A Tunable Clock Buffer for Intra-die PVT Compensation in Single-Edge Clock (SEC) Distribution Networks

Jeff Mueller and Resve Saleh

University of British Columbia

5:25PM

3E.26

Fast Timing Update under the Effect of IR Drop

muzhou shao

Synopsys Inc.

ISQED KEYNOTE SPEECHES
Plenary Session 2P
Wednesday March 19
8:30am-10:15am

Session Chairs
Kris Verma
Silicon Valley Technical Institute

Lech Jozwiak
Eindhoven University of Technology

Keynote Speech 2P.1
Wednesday, March 19
8:45am-9:15am

Consumerization of Electronics and Nanometer Technologies: Implications for Manufacturing Test

Sanjiv Taneja
Vice President and GM, Encounter Test business unit
Cadence Design Systems

Test has long been recognized as the bridge between Design and Manufacturing. However, innovation and deep integration in design and test tools has not kept pace with the consumerization of electronics and the rapidly evolving nanometer IC design and manufacturing. As a result, the full potential of Test has not been harnessed by the mainstream semiconductor community. The consumerization of electronics places significant new demands on low power, correctness and time-to-volume production. The rapid advances in nanometer technologies pose additional set of challenges due to the advanced physics effects and higher scales of transistor integration.
The EDA industry needs to establish a new paradigm and a "deep integration" to meet these challenges. During the design phase, a power-aware DFT architecture must integrate tightly with low power design and implementation flow. Later, during the manufacturing phase, the benefits of DFT must be seamlessly harnessed for rapid scan diagnostics based yield learning using not only logic information from the design database but also using layout timing and power information. This keynote will discuss these challenges and possible solutions and scenarios.

Keynote Speech 2P.2
Wednesday, March 19
9:15am-9:45am

Statistical Techniques to Achieve Robustness and Quality

Chandu Visweswariah
Research Staff Member
IBM Thomas J. Watson Research Center in Yorktown Heights, NY

Variability due to manufacturing, environmental and aging uncertainties constitutes one of the major challenges in continuing CMOS scaling. Worst-case design is simply not feasible any more. This presentation will describe how statistical timing techniques can be used to reduce pessimism, achieve full-chip and full-process coverage, and enable robust design practices. A practical ASIC methodology based on statistical timing will be described. Robust optimization techniques will be discussed. Variability makes post-manufacturing testing a daunting task. Process coverage is a new metric that must be considered. Statistical techniques to improve quality in the context of at-speed test will be presented. Key research initiatives required to achieve elements of a statistical design flow will be described.

Keynote Speech 2P.3
Wednesday, March 19
9:45am-10:15am

The Greening of the SoC - How Electrical Engineers Will Save the World

Rich Goldman
Vice-President, Strategic Alliances for Synopsys and CEO of Synopsys Armenia, USA

Global Warming is hot! Climate change is occurring all around us, and the scientific evidence is increasingly overwhelming pointing to man's hand in the phenomena. We are already seeing huge impacts of Climate Change, much faster than anybody predicted, only a few short years ago. What can we do about? How can we slow and even reverse our impact on Climate Change? The key man made contributing factor is carbon emissions, primarily from coal fired power plants. We need to reduce the number of plants that we building, then the number of power plants that we require. The key to this is a reduction in power consumption. There are many everyday actions we can take individually to help. Al Gore states that Global Warming is an engineering problem that will be solved by engineers, addressing the issue as an opportunity, rather than additional cost. We will explore how engineers will impact Climate Change. Low Power IC design techniques will play a role in this just as new powerful techniques are coming into vogue.

SESSION 4A
Wednesday March 19
10:30am-12:00noon
Room: San Jose

Co-design Applications for IC Packages

Chair: **Kamesh Gadepally**

Co-Chair: **Lalitha Immaneni**

10:30AM
4A.1
System-in-Package Technology: Opportunities and Challenges
Anna Fontanelli
Mentor Graphics Corporation

11:00AM
4A.2
Printed Circuit Board Assembly Test Process and Design for Testability
Thao Nguyen and Navid Rezvani
NetApp Inc.

11:20AM
4A.3
Fast Evaluation Method for Transient Hot Spots in VLSI ICs in Packages
Je-Hyoung Park[1], Ali Shakouri[1], Sung-Mo Kang[2]
[1]UC Santa Cruz, [2]UC Merced

11:40AM
4A.4
An Implementation of Performance-Driven Block and I/O Placement for Chip-Package Codesign
Ming-Fang Lai and Hung-Ming Chen
Dept of EE, NCTU, Taiwan

12:00PM
4A.5
Techniques for Early Package Closure in System-in-Packages
Santhosh Vaidyanathan, Amit Brahme, Jairam Sukumar
Texas Instruments, India

SESSION 4B
Embedded Tutorial
Wednesday March 19
10:30am-12:00noon
Room: Santa Clara

Robust Design Methodologies

Moderator
Mark Maurer - Silvaco International

Overview:
The current design trend is for the product lifecycle of SOCs and electronic systems to be very short (sub 18mos), There are still many applications, where 15+ year design life cycles are the norm. With the shift from pure consumer "line cord" applications to mobile and vehicle applications, this long operational lifetime and MTBF requirement is becoming much more common. This tutorial will provide an overview of the issues behind the long MTBF "crisis" and also solution directions for solving a number of the issues for specific design situations. Topics presented in this tutorial are:

Tutorial 4B.1
Wednesday, March 19
10:30am-11:00am

Mil/Aero/Vehicle High Reliability Design - Issues/challenges/solutions

Chris Nicklaw
L3 Communications

Tutorial 4B.2
Wednesday, March 19
11:00am-11:30am

An Overview of the High Reliability Design Space

Prof. Todd R. Weatherford
Naval Post Graduate School - Monterey

Tutorial 4B.3
Wednesday, March 19
11:30am-12:00pm

Modifications and Tradeoffs in the Creation and Characterization of High Reliability IP

Dr. André Reis
Nangate

SESSION 4C
Wednesday March 19
10:30am-12:00noon
Room: Carmel

Tools and Interconnects

Chair: **Bao Liu**
Co-Chair: **Soroush Abbaspour**

11:00AM
4C.2

Fast Shape Optimization of Metallization Patterns for DMOS Based Driver
BO YANG, Shigetoshi NAKATAKE, Hiroshi MURATA
The University of Kitakyushu, Japan

11:20AM
4C.3

MAISE: An Interconnect Simulation Engine for Timing and Noise Analysis
Frank Liu and Peter Feldmann
IBM

11:40AM
4C.4

Accelerating Clock Mesh Simulation Using Matrix-Level Macromodels and Dynamic Time Step Rounding
Xiaoji Ye[1], Min Zhao[2], Rajendran Panda[3], Peng Li[1], Jiang Hu[1]
[1]Texas A&M University, [2]Magma Design Automation, Inc., [3]Freescale Semiconductor, Inc.

SESSION 4D

Wednesday March 19
10:30am-12:00noon
Room: Monterey

Sequential Analysis, Defect Modeling and At-speed Testing

Chair: **Sreejit Chakravarty**

Co-Chair: **Li-C Wong**

10:30AM

4D.1

Sequential Path Delay Fault Identification Using Encoded Delay Propagation Signatures

Edward Flanigan, Arkan Abdulrahman, Spyros Tragoudas

Southern Illinois University

11:00AM

4D.2

2D Decomposition Sequential Equivalence Checking of System Level and RTL Descriptions

Dan Zhu, Tun Li, Yang Guo, Si-kun Li

School of Computer Science and Technology, National University of Defense Technology

11:20AM

4D.3

Automated Standard Cell Library Analysis for Improved Defect Modeling

Jason Brown and Shawn Blanton

Carnegie Mellon University

11:40AM

4D.4

A Novel Automated Scan Chain Division Method for Shift and Capture Power Reduction in Broadside At-Speed Test

Ho Fai Ko and Nicola Nicolici

McMaster University

Luncheon Panel Discussion
Sponsored by Cadence Design Systems
Wednesday March 19 2008
12:00 noon-1:30pm

Statistical Design - Solutions Searching for Problems?

Moderator
Michael Santarini
Senior Editor, EDN

Description
The EDA community has been pitching statistical design as the salvation for design variability issues in sub 130nm design for several years. Although progress has been made, it has yet to be widely used. It is needed at the front-end of the process, but the information to support it is hard to get. But once the data is available, it is no longer necessary. This distinguished group has a 75% chance of answering this question.

Panelists
Patrick Drennan, *CTO, Solido Design Automation Inc.*
Mustafa Celik, *CEO, Extreme DA*
Kishore Singhal, *Synopsys Scientist, Synopsys Inc.*
Rob Mathews, *VP Extraction Products, Sequence Design Inc.*
Sreedhar Natarajan, *VP TSMC Design Technology Canada Inc, TSMC*
Raul Camposano, *CEO, Xoomsys*
Vinod Kariat, *R&D Group Director, Cadence Design Systems*

SESSION 5A
Wednesday March 19
1:30pm-3:30pm
Room: San Jose

Modeling and Analysis in Physical Design

Chair: **Rajeev Murgai**
Co-Chair: **Martin Wong**

1:30PM
5A.1
Finite-Point Gate Model for Fast Timing and Power Analysis
Dinesh Ganesan[1], Alex Mitev[2], Yu Cao[1], Janet Wang[2]
[1]Arizona State University, [2]University of Arizona

2:00PM
5A.2
Noise-Aware On-Chip Power Grid Considerations Using a Statistical Approach
Daniel A. Andersson[1], Lars 'J' Svensson[2], Per Larsson-Edefors[2]
[1]Department of Computer Science and Engineering, Chalmers, [2]

2:30PM
<u>**5A.3**</u>
Simulation and Measurement of On-Chip Supply Noise in Multi-Gigabit I/O Interfaces
Hai Lan[1], Ralf Schmitt[1], Chuck Yuan[2]
[1]Rambus Inc., [2]Rambus Ins.

2:50PM
<u>**5A.4**</u>
Practical Clock Tree Robustness Signoff Metrics
Anand Rajaram, Raguram Damodaram, Arjun Rajagopal
DDSP, Texas Instruments, Dallas

3:10PM
<u>**5A.5**</u>
Hierarchical Soft Error Estimation Tool (HSEET)
Ramakrishnan Krishnan[1], Rajaraman Ramanarayanan[2], Vijaykrishnan Narayanan[1], Yuan Xie[1], Mary Jane Irwin[1]
[1]Pennsylvania State University, [2]Intel Corporation

SESSION 5B
Wednesday March 19
1:30pm-3:30pm
Room: Santa Clara

Emerging Technologies and Novel Applications

Chair: **Paul Tong**

Co-Chair: **Bao Liu**

1:30PM

5B.1

Design Margin Exploration of Spin-Torque Transfer RAM (SPRAM)

Yiran Chen, Xiaobin Wang, Hai Li, Hongyue Liu, Dimitar Dimitrov

Seagate LLC

2:00PM

5B.2

Investigating the Design, Performance, and Reliability of Multi-Walled Carbon Nanotube Interconnect

Arthur Nieuwoudt and Yehia Massoud

Rice University

2:30PM

5B.3

Micropipeline-Based Asynchronous Design Methodology for Robust System Design Using Nanoscale Crossbar

Rajat Subhra Chakraborty and Swarup Bhunia

Case Western Reserve University

2:50PM

5B.4

Statistical Evaluation of Split Gate Opportunities for Improved 8T/6T Column-decoupled SRAM Cell Yield

Rouwaida Kanj, Rajiv Joshi, Keunwoo Kim, Richard Williams, Sani Nassif

IBM

3:10PM

5B.5

High Resolution Read-out Circuit for DNA Label-Free Detection System

Daniela De Venuto

Politecnico di Bari, Italy

SESSION 5C
Wednesday March 19
1:30pm-3:30pm
Room: Carmel

Statistical Timing

Chair: **Kevin Brelsford**

Co-Chair: **Azadeh Davoodi**

1:30PM
5C.1
Fast and Accurate Statistical Static Timing Analysis with Skewed Process Parameter Variation
Lin Xie and Azadeh Davoodi
University of Wisconsin at Madison

2:00PM
5C.2
Characterizing Intra-die Spatial Correlation Using Spectral Density Method
Qiang Fu, Wai-Shing Luk, Xuan Zeng
Fudan University, China

2:30PM
5C.3
Investigating the Impact of Fill Metal on Crosstalk-Induced Delay and Noise
Arthur Nieuwoudt[1], Jamil Kawa[2], Yehia Massoud[1]
[1]Rice University, [2]Synopsys

2:50PM
5C.4
Process-Variation Statistical Modeling for VLSI Timing Analysis
Jui-Hsiang Liu[1], Lumdo Chen[2], Charlie Chung-Ping Chen[1]
[1]EE Department, National Taiwan University, Taiwan, [2]UMC, Taiwan

3:10PM
5C.5
A Design Model for Random Process Variability
Victoria Wang[1], Kanak Agarwal[2], Sani Nassif[2], Kevin Nowka[2], Dejan Markovic[1]
[1]UCLA, [2]IBM

SESSION 5D
Wednesday March 19
1:30pm-3:30pm
Room: Monterey

Modern Processor Design

Chair: **Arthur Chojnacki**

Co-Chair: **Lech Jozwiak**

1:30PM
5D.1
A Scratch-Pad Memory Aware Dynamic Loop Scheduling Algorithm
Ozcan Ozturk[1], Mahmut Kandemir[2], Sri Hari Krishna Narayanan[2]
[1]Marvell Semiconductors, [2]Pennsylvania State University

2:00PM
5D.2
Amplifying Embedded System Efficiency via Automatic Instruction Fusion on a Post-Manufacturing Reconfigurable Architecture Platform
Allen C. Cheng
University of Pittsburgh

2:30PM
5D.3
Runtime Validation of Transactional Memory Systems
Kaiyu Chen[1], Sharad Malik[1], Priyadarsan Patra[2]
[1]Princeton University, [2]Intel Corporation

2:50PM
5D.4
SEU Vulnerability of Multiprocessor Systems and Task Scheduling for Heterogeneous Multiprocessor Systems
Makoto Sugihara
Toyohashi University of Technology

SESSION 6A
Wednesday March 19
3:45pm-5:45pm
Room: San Jose

Modeling and Design of Reliable Circuits

Chair: **Xin Li**

Co-Chair: **Jose Silva Matos**

3:45PM

6A.1

Node Criticality Computation for Circuit Timing Analysis and Optimization under NBTI Effect

Wenping Wang[1], Shengqi Yang[2], Yu Cao[1]

[1]Arizona State University, [2]Intel Corporation

4:15PM

6A.2

Design for Reliability: A Novel Asynchronous Circuit Design with Fast Forwarding Technique at Advanced Technology Node

Chin-Khai Tang, Chun-Yen Lin, Yi-Chang Lu

Graduate Institute of Electronics Engineering, National Taiwan University

4:45PM

6A.3

Modeling of NBTI-Induced PMOS Degradation under Arbitrary Dynamic Temperature Variation

Bin Zhang and Michael Orshansky

University of Texas at Austin

5:05PM

6A.4

Reliability-Aware Optimization for DVS-Enabled Real-Time Embedded Systems

Foad Dabiri, Navid Amini, Mahsan Rofouei, Majid Sarrafzadeh

University of California Los Angeles

5:25PM

6A.5

A Basis for Formal Robustness Checking

Goerschwin Fey and Rolf Drechsler

University of Bremen

SESSION 6B
Wednesday March 19
3:45pm-5:45pm
Room: Santa Clara

Design for Manufacturing

Chair: **Jay Sivagnaname**
Co-Chair: **Jianliang Li**

3:45PM
6B.1
Quantified Impacts of Guardband Reduction on Design Process Outcomes
Kwangok Jeong, Andrew B. Kahng, Kambiz Samadi
University of California, San Diego

4:15PM
6B.2
Partitioning for Selective Flip-Flop Redundancy in Sequential Circuits
Uthman Alsaiari and Resve Saleh
The University of British Columbia

4:45PM
6B.3
A Root-Finding Method for Assessing SRAM Stability
Rouwaida Kanj, Zhuo Li, Rajiv Joshi, Frank Liu, Sani Nassif
IBM

5:05PM
6B.4
Cellwise OPC Based on Reduced Standard Cell Library
Hailong Jiao and Lan Chen
Department of Common Technology, Institute of Microelectronics, Chinese Academy of Sciences

5:25PM
6B.5
On-Chip Process Variation Detection and Compensation using Delay and Slew-Rate Monitoring Circuits
Amlan Ghosh[1], Rahul Rao[2], Ching-te Chuang[2], Richard Brown[1]
[1]University of Utah, Salt Lake City, UT 84112, [2]IBM TJ Watson Research Center, Yorktown Heights, NY 10598

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SESSION 6C
Wednesday March 19
3:45pm-5:45pm
Room: Carmel

Structural Test

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Chair: **George Alexiou**

Co-Chair: **Yiran Chen**

3:45PM
6C.1
Interval based X-masking for Scan Compression Architectures
Anshuman Chandra and Rohit Kapur
Synopsys, Inc.

4:15PM
6C.2
Two New Methods for Accurate Test Set Relaxation via Test Set Replacement
Stelios Neophytou and Maria Michael
University of Cyprus

4:45PM
6C.3
Embedded Deterministic Test Exploiting Care Bit Clustering and Seed Borrowing
Adam Kinsman and Nicola Nicolici
McMaster University

5:05PM
6C.4
A Built-In Test and Characterization Method for Circuit Marginality Related Failures
Alodeep Sanyal and Sandip Kundu
Univ. of Massachusetts

5:25PM
6C.5
On Chip Jitter Measurement through a High Accuracy TDC.
Akhil Garg and Prashant Dubey
STMicroelectronics Pvt Ltd

SESSION 6D
Wednesday March 19
3:45pm-5:45pm
Room: Monterey

Advanced Design Methodologies

Chair: **Vamsi Srikantam**
Co-Chair: **Sundareswaran Savithri**

3:45PM
6D.1
Robust Analog Design for Automotive Aplications by Design Centering with Safe Operating Areas
Karl-Heinz Rooch[1], Udo Sobe[1], Andreas Ripp[2], Michael Pronath[2]
[1]ZMD Zentrum Mikroelektronik Dresden AG, [2]MunEDA GmbH

4:15PM
6D.2
Compact FinFET Memory Circuits with P-Type Data Access Transistors for Low Leakage and Robust Operation
Sherif Tawfik and Volkan Kursun
University of Wisconsin-Madison

4:45PM
6D.3
Towards Uniform Temperature Distribution in SOI Circuits Using Carbon Nanotube Based Thermal Interconnect
Yu Zhou, Somnath Paul, Swarup Bhunia
Case Western Reserve University

5:05PM
6D.4
Statistic Analysis of Power/Ground Networks Using Single-Node SOR Method
Zuying Luo[1] and Sheldon Xiang Dong Tan[2]
[1]College of Information Science and Technology, Beijing Normal University,   Beijing, 100875, [2]Department of Electrical Engineering, University of California at Riverside, Riverside CA, 92521, USA

5:25PM
6D.5
IPOSA: A Novel Slack Distribution Algorithm for Interconnect Power Optimization
Xiang Qiu, Yuchun Ma, Xiangqing He, Xianlong Hong
Tsinghua University

Thanks for your participation and looking forward seeing you at ISQED 2009