Taming the Challenges of Advanced-Node Design

Tom Beckley
Sr. VP of R&D, Custom IC and Signoff, Silicon Realization Group
ISQED 2012 – March 20, 2012

cādence®

The custom design community

“Designers”
(“Relaxed” attitude on physical rules and methodology)

“CAD” Engineers
(Not relaxed about rules. Whole different attitude, too)

© 2012 Cadence Design Systems, Inc. All rights reserved.
cadence®

Agenda

1. Market trend and overview
2. The 20nm custom challenges
3. What do we need to do?
4. Open decisions: color and patterns
5. Summary

© 2012 Cadence Design Systems, Inc. All rights reserved.

cadence®

Evolving industry custom design trend

Mobility rules: very short time before next generation

More connected devices per person: 6x in next 10 years

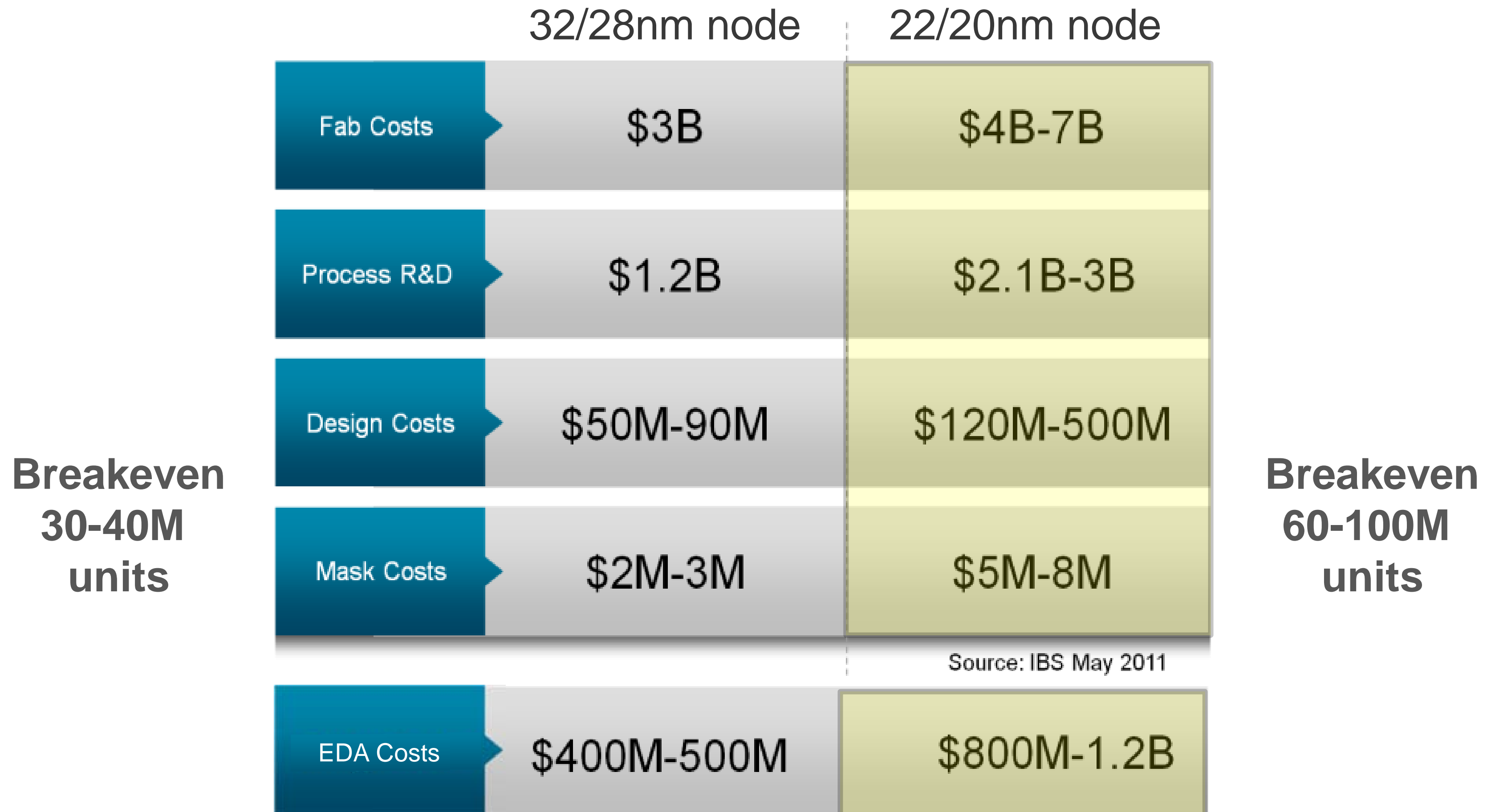
Mobility is the driver and 20nm/14nm nodes will be key

- ✓ **Expected 25-30% improvement in power consumption**
- ✓ **Desired 15-18% improvement in performance**
- ✓ **Predicted ~2x in density**

© 2012 Cadence Design Systems, Inc. All rights reserved.

cadence®

Challenge: investment in 20nm technology



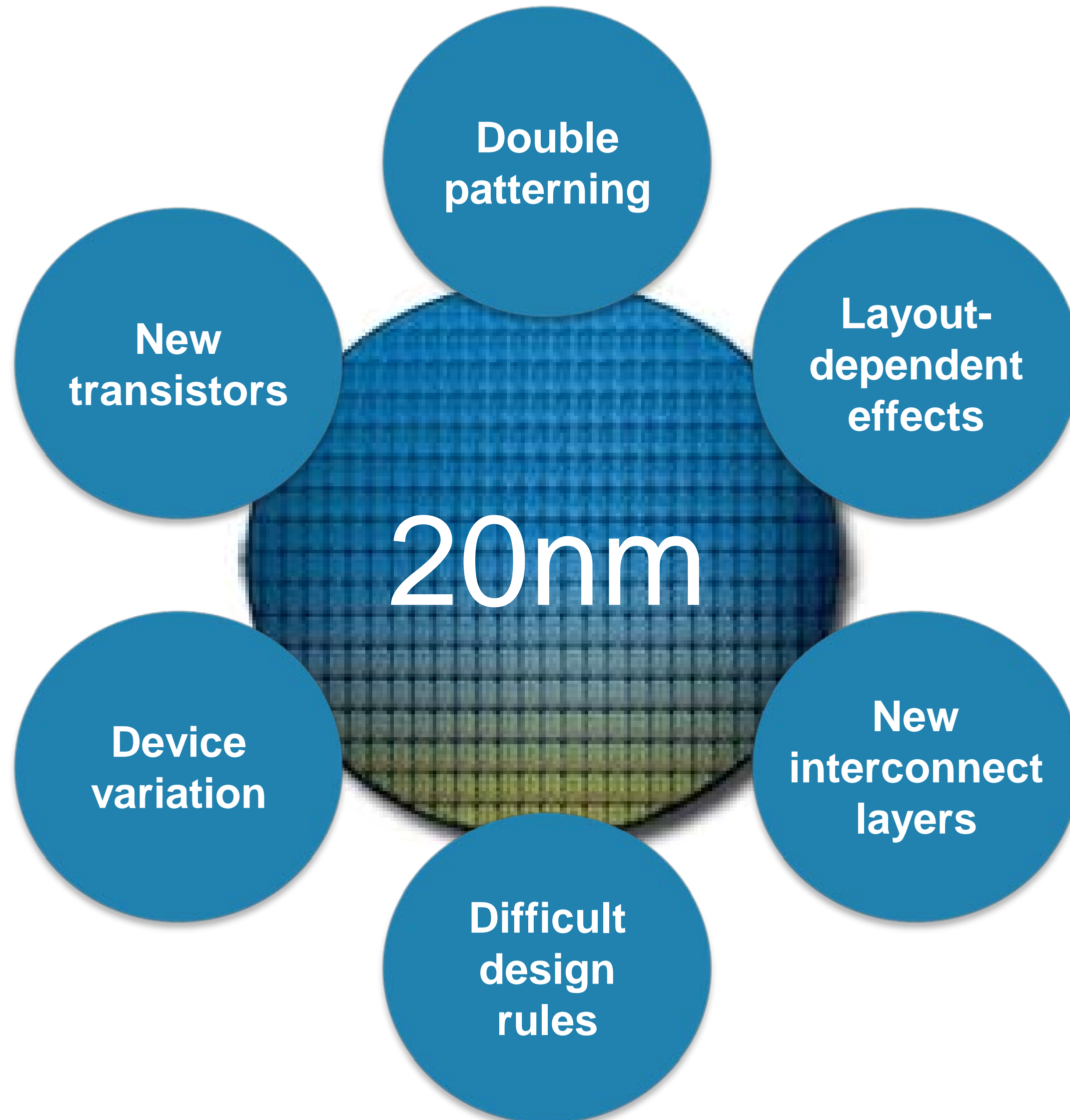
Finances mandate careful "risk" considerations

© 2012 Cadence Design Systems, Inc. All rights reserved.

cadence®

Challenge: manufacturing complexity

It's all new again compared to 28nm design

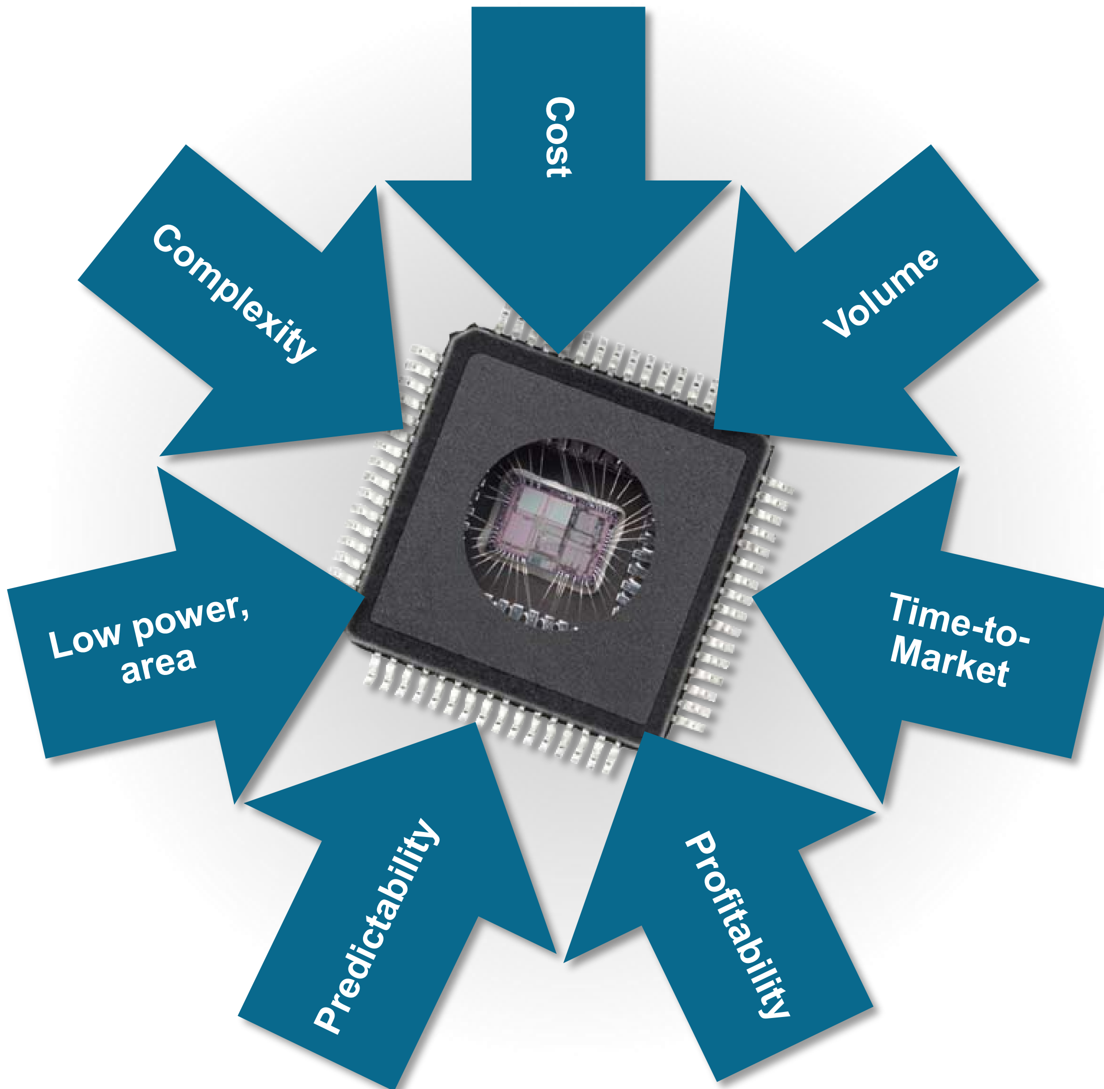


© 2012 Cadence Design Systems, Inc. All rights reserved.

cadence®

Challenge: design enablement

All the usual suspects are still present and causing trouble



And don't forget:

- Multi-source IP
- Mixed-signal and RF
- 3D-IC methods
- System-in-package

© 2012 Cadence Design Systems, Inc. All rights reserved.
cādence®

Agenda

1. Market trend and overview
2. The 20nm custom challenges
3. What do we need to do?
4. Open decisions: color and patterns
5. Summary

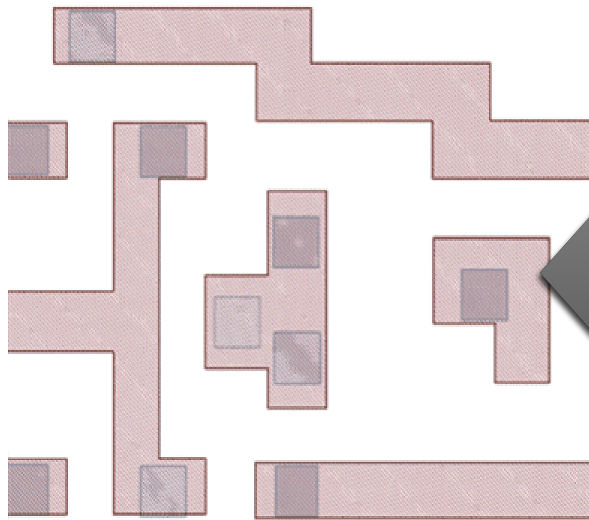
© 2012 Cadence Design Systems, Inc. All rights reserved.

cadence®

Double patterning technique

A must-have at wire pitches smaller than 80nm

Geometry features disappearing due to lithography distortion

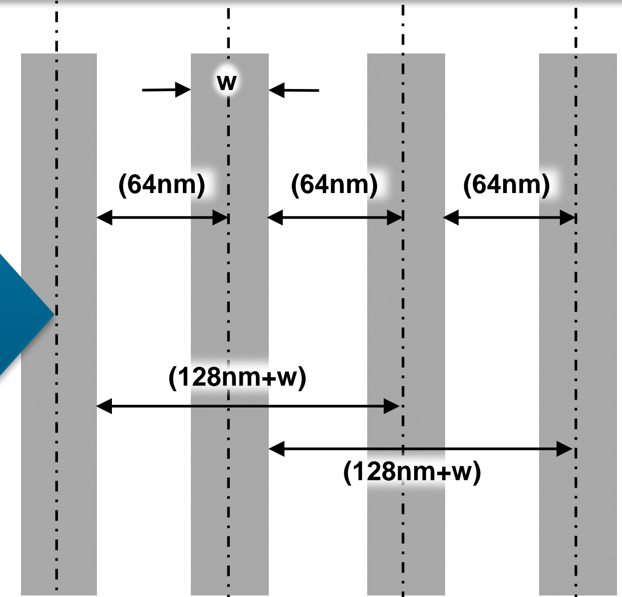


Not feasible due to optical resolution limits

Conventional Lithography

Double Patterning

Enables printing of images below minimum spacing design rules



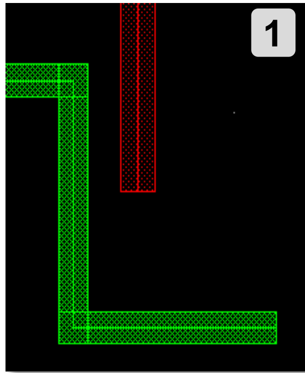
Pitch between images is effectively doubled by printing alternately

© 2012 Cadence Design Systems, Inc. All rights reserved.

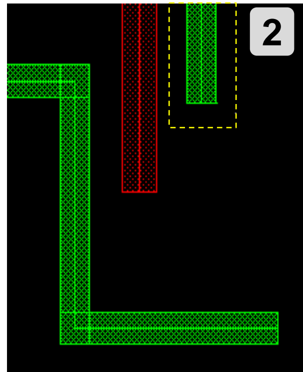
cadence®

Double patterning problems

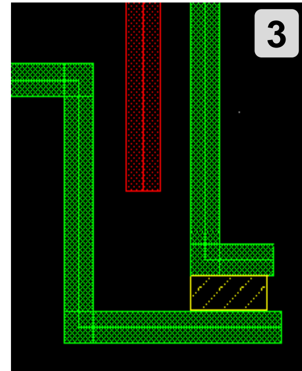
It's easy to create design rule violations without even trying



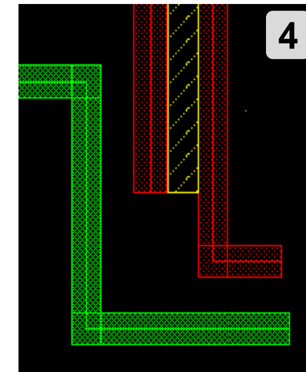
Two nets, colored for double pattern



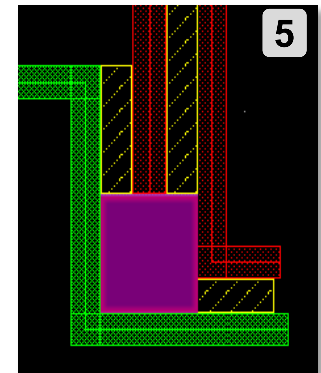
Create three wires



Conflict created



Re-colored conflict remains



DPT DRC

- It isn't just a matter of flipping a shape
- THINK about the ripple effect throughout the entire design

© 2012 Cadence Design Systems, Inc. All rights reserved.

cadence®

Layout-dependent effects at adv custom nodes

Layout-dependent effects		45nm	32nm	20nm and below
WPE	Well proximity effect	x	x	x
PSE	Poly spacing effect		x	X
LOD	Length of diffusion	x	X	X
OSE	OD to OD spacing effect		x	X
LPC	Layout patterning check		x	x
OP/PO Density	OD/poly density		X	X

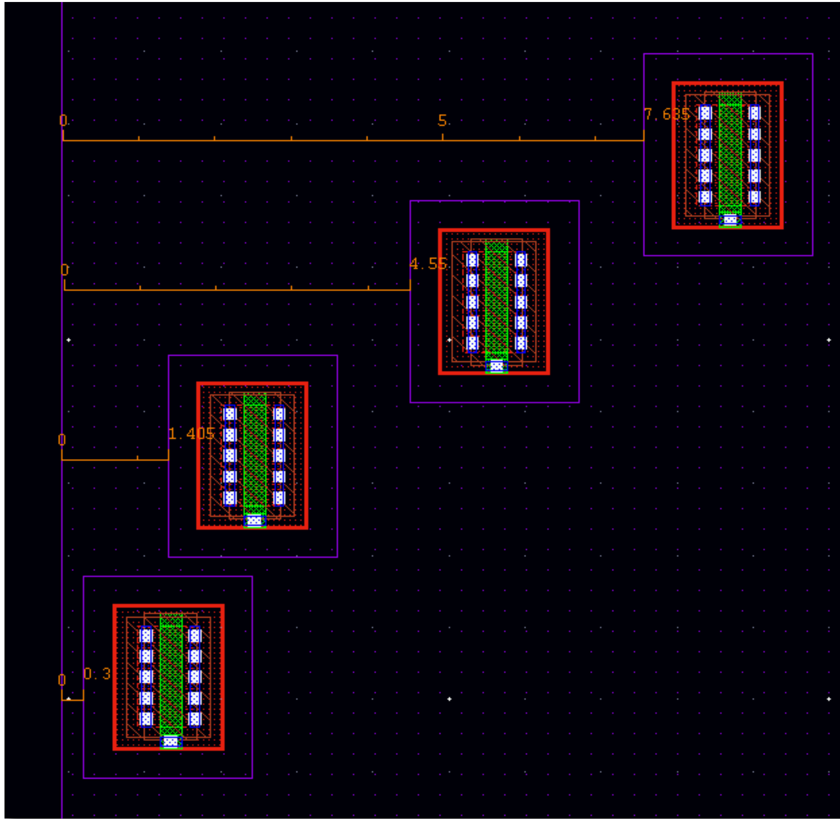
Foundries insist that new verification standards are met by the customer prior to agreeing to manufacture

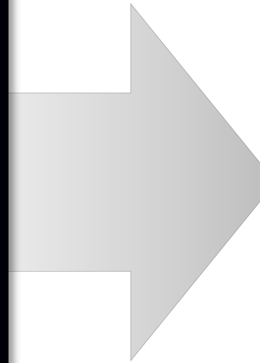
© 2012 Cadence Design Systems, Inc. All rights reserved.

cādence®

LDE example: well proximity effect

Threshold voltages aren't what they use to be





Now the layout is the design

- Additional physical effects:
  - Shallow trench isolation
  - Interconnect parasitics
  - Dummy fill usage
  - Lithography

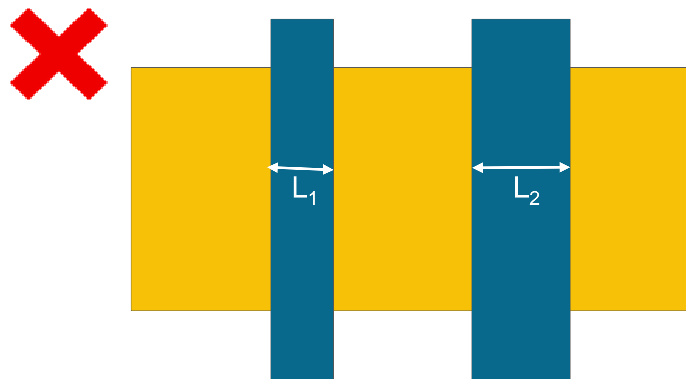
© 2012 Cadence Design Systems, Inc. All rights reserved.

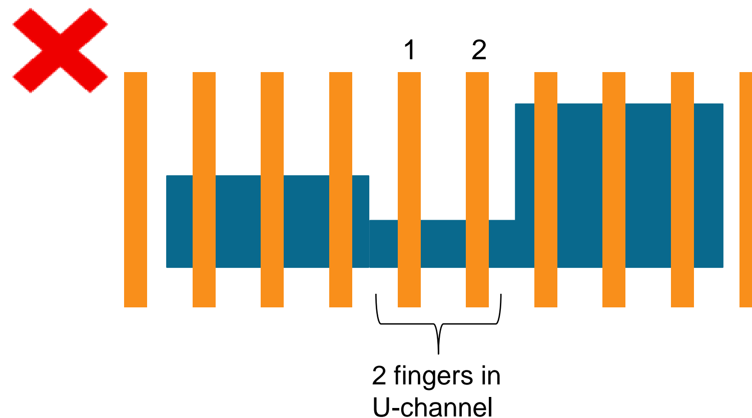
cādence®

Increased device-rule complexity

For custom design: ~4x new rules vs 90nm

- What we know so far:
  - Total of about 5000 DRC checks for 20nm
    - Double patterning alone requires 30-40 checks
  - Layout directional orientation rules
  - Very specific rules governing L/W and varying transistor proximity
  - New rules regarding legal interdigitation patterns





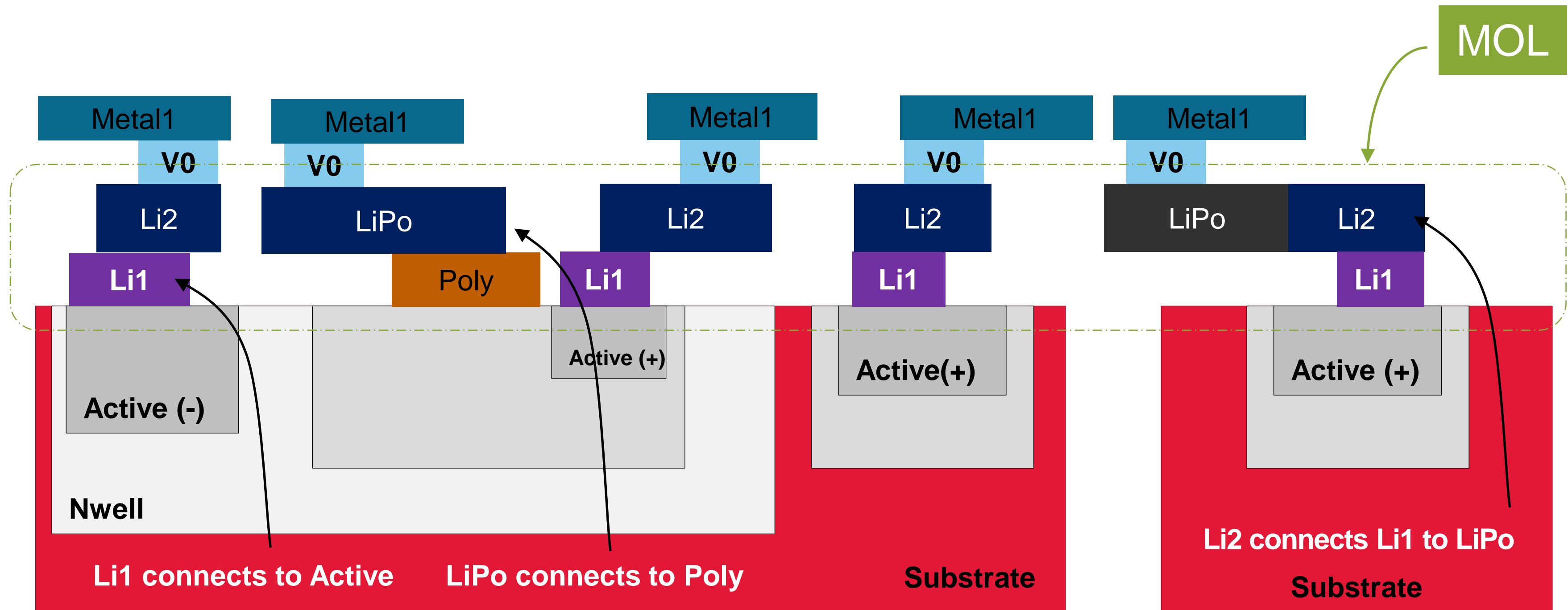
 © 2012 Cadence Design Systems, Inc. All rights reserved.

cādence®

New routing layers (local interconnect / middle-of-line)

Allows very dense local routing below 1st metal

- Local Interconnect (Li) layers are contactless metal layers that connect by shape overlap without need of a cut layer



 © 2012 Cadence Design Systems, Inc. All rights reserved.

cādence®

Agenda

1. Market trend and overview
2. The 20nm custom challenges
3. What do we need to do?
4. Open decisions: color and patterns
5. Summary

© 2012 Cadence Design Systems, Inc. All rights reserved.

What do we need to do?

A mixture of tools and techniques

New custom methodology

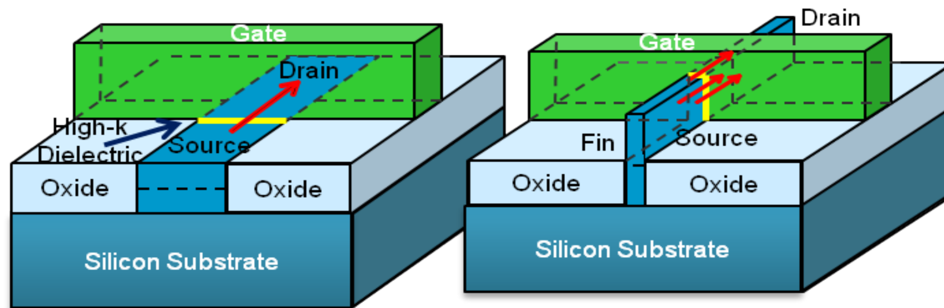
 © 2012 Cadence Design Systems, Inc. All rights reserved.

cadence

New Devices and Tools

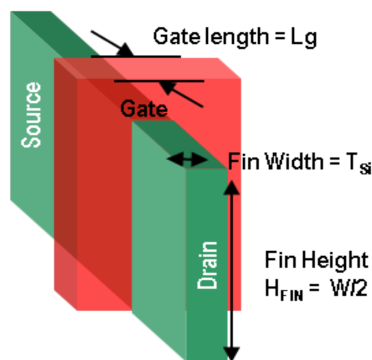
New 3D devices (FinFET, Tri-gate)

Alternative to planar

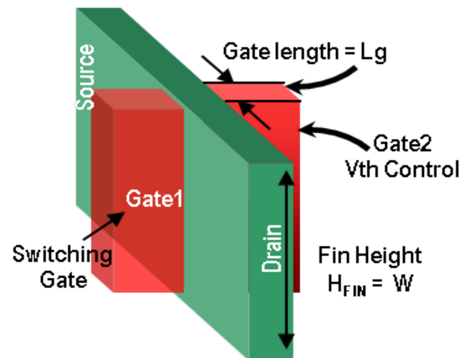


Planar FET

Tri-gate, FinFET



Tri-gate, FinFET



Independent
double-gate FinFET

- FinFET advantages:
  - Smaller area (50%)
  - Higher frequency (40%)
  - Less power (up to 50%)
  - Less leakage
  - Higher drive current
  - Noise and latch-up are minimized
  - No reverse-biased diodes to substrate

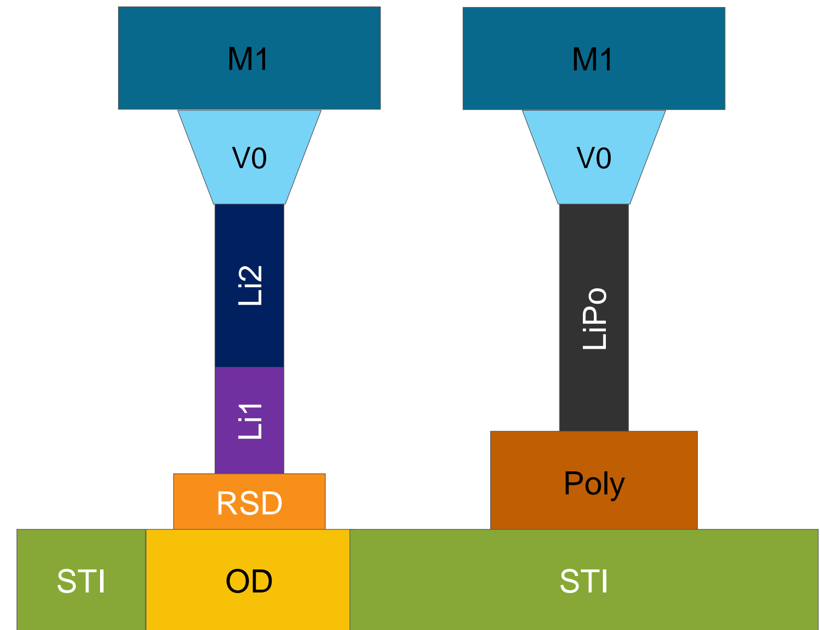
© 2012 Cadence Design Systems, Inc. All rights reserved.

cādence®

Extraction technology

New structures necessitate more complex analysis

- Must address the growing electrical challenges plus unique structures in 20nm
  - New: Fracture_vias
  - Raised source/diffusion
  - New parasitic structures for flash memories
  - Double patterning requires more corner verification files



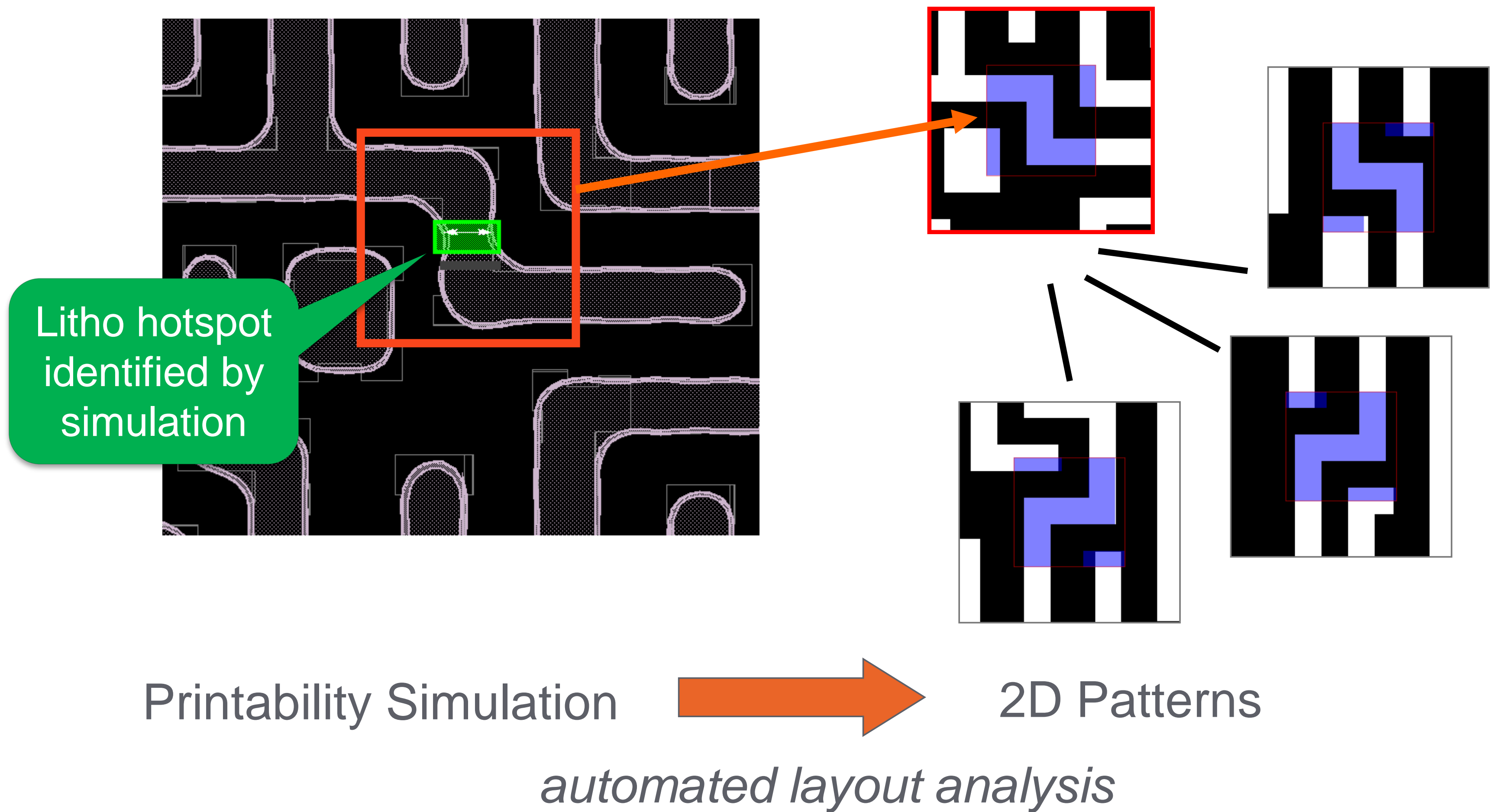
Via fracturing for MOL routing

© 2012 Cadence Design Systems, Inc. All rights reserved.

cādence®

DFM innovation: 100x faster than simulation

Pattern-based litho hotspot identification



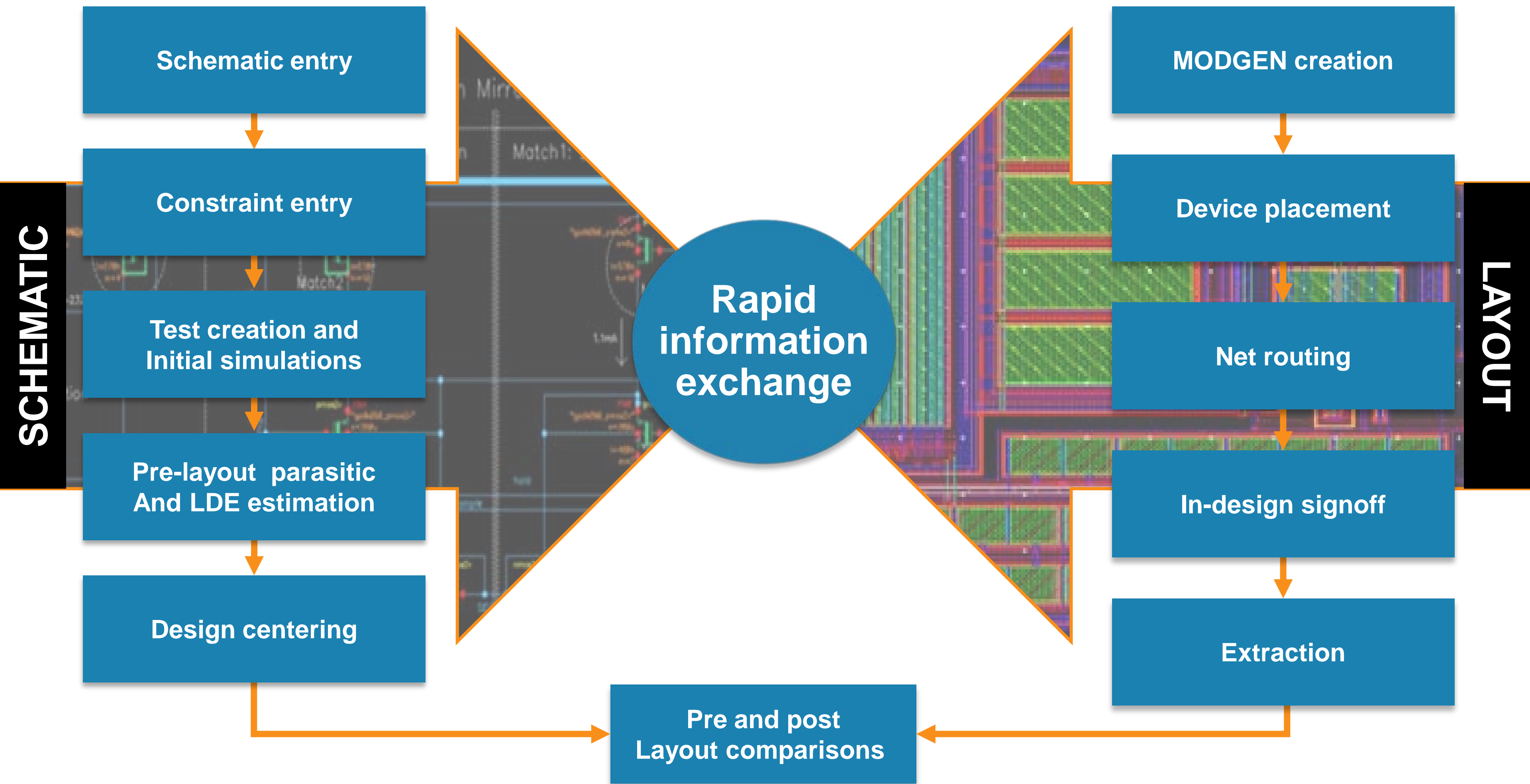
Courtesy: From Cadence Webinar, DRC+ Now: Early DFM Signoff in the Digital Implementation Process' Dr. Vito Dai, GLOBALFOUNDRIES

© 2012 Cadence Design Systems, Inc. All rights reserved.
cadence®

New Custom Methodology

New custom methodology

No more “tossing over the wall”

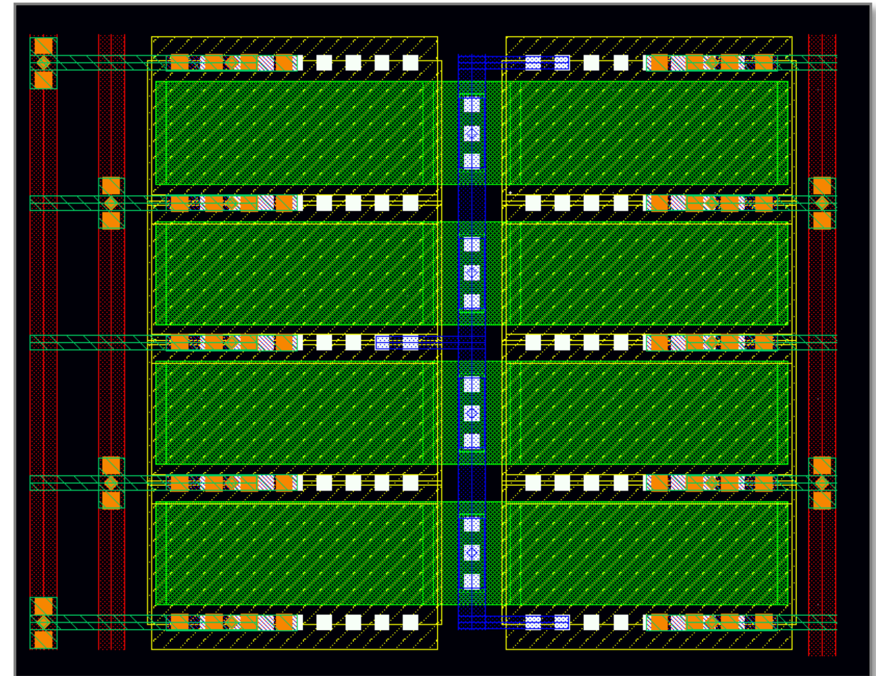


© 2012 Cadence Design Systems, Inc. All rights reserved.

Rapid layout prototyping

Create layout building blocks for better *electrical* understanding

- P&R engine support for 20nm design rules
- Complex abutment rule support
- Local interconnect routing
  - Array-based FinFET configurations
  - Coloring higher-level abstraction
  - Incremental device-level extraction
  - LDE-aware device placement

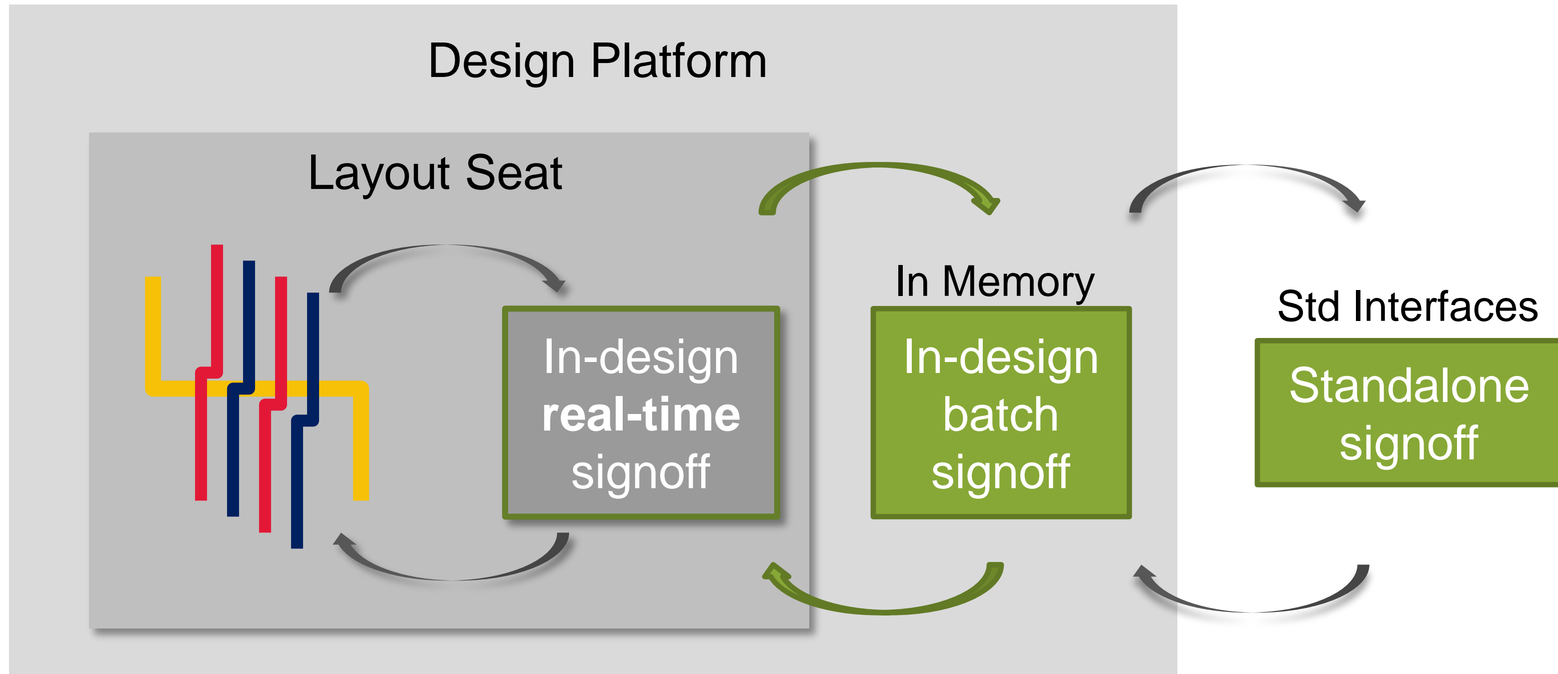


 © 2012 Cadence Design Systems, Inc. All rights reserved.

cādence®

The key to speed: “in-design” signoff

A requirement at 20nm design



GOOD: Traditional standalone signoff using standard interfaces

BETTER: Batch in-design signoff executing off in-memory data

BEST: Dynamic in-design signoff tightly integrated into layout seat

© 2012 Cadence Design Systems, Inc. All rights reserved.

Agenda

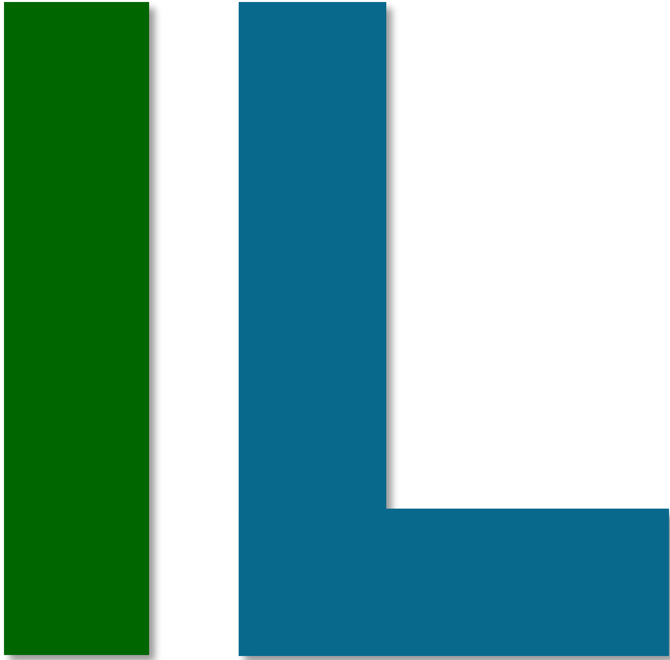
1. Market trend and overview
2. The 20nm custom challenges
3. What do we need to do?
4. Open decisions: color and patterns
5. Summary

© 2012 Cadence Design Systems, Inc. All rights reserved.

cadence®

Good pattern vs bad pattern matching

An ounce of prevention is worth a pound of cure



What color???

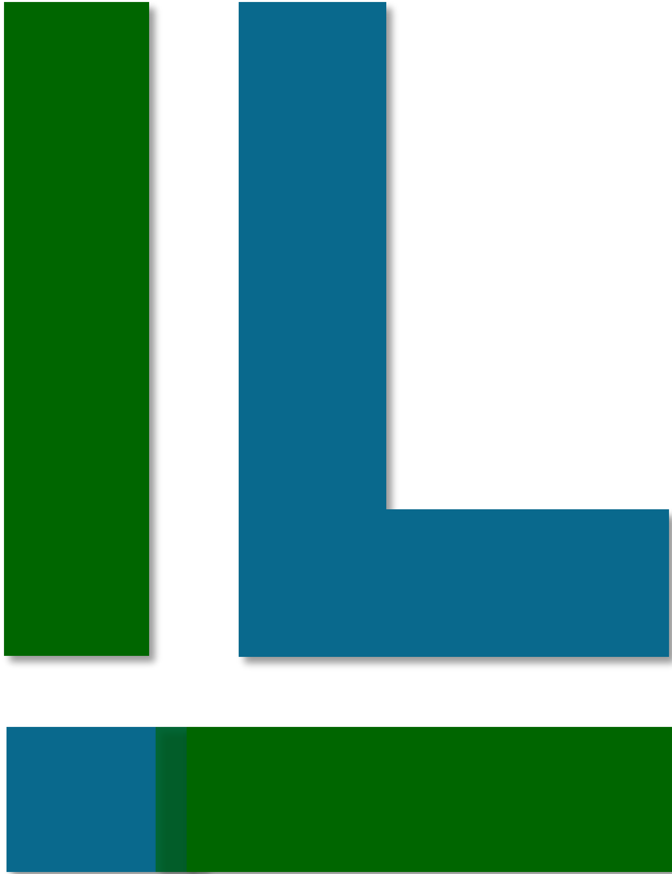
- Today, it’s all about finding and fixing but what if we could prevent in the first place?
- This pattern is DRC correct according to the minSpacing rule, but what color is chosen?

© 2012 Cadence Design Systems, Inc. All rights reserved.

cadence®

Good pattern vs bad pattern matching

An ounce of prevention is worth a pound of cure



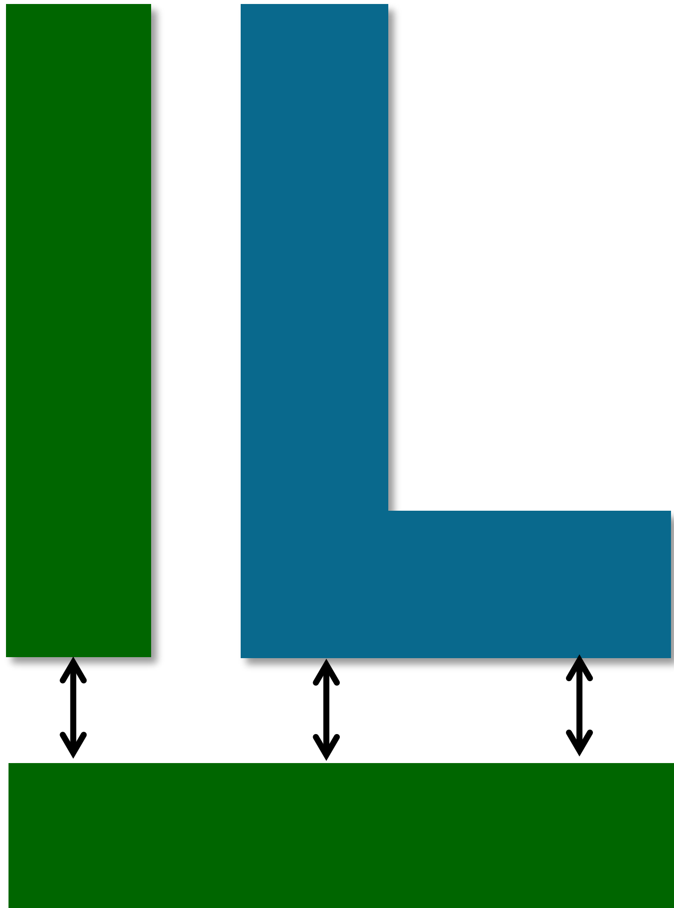
- This pattern is DRC correct according to the minSpacing rule, but what color is chosen?
- Correction method:
  - Split the shape and stitch back together making sure the overlap is sufficient…tricky

© 2012 Cadence Design Systems, Inc. All rights reserved.

cādence®

Good pattern vs bad pattern matching

An ounce of prevention is worth a pound of cure



- This pattern is DRC correct according to the minSpacing rule, but what color is chosen?
- Correction method:
  - Split the shape and stitch back together making sure the overlap is sufficient…tricky
  - Build it right the first time by adding some extra space at the time of creation…develop a "larger" pattern for the auto-router

© 2012 Cadence Design Systems, Inc. All rights reserved.
cadence®

Other lingering manufacturing questions

Each answer seems to raise five new questions

Is DPT sufficient for 14nm?

Will you need to move to MPT at 10nm?

Use simultaneous ebeams for multi/double pattern?

Will EUV ever be ready?

What about Directed Self-Assembly (DSA)?

© 2012 Cadence Design Systems, Inc. All rights reserved.
cādence®

Agenda

1. Market trend and overview
2. The 20nm custom challenges
3. What do we need to do?
4. Open decisions: color and patterns
5. Summary

© 2012 Cadence Design Systems, Inc. All rights reserved.
cādence®

Where will the future take you?

We can have more than ***Moore***

- Industry collaboration
- New methodologies
- New tools

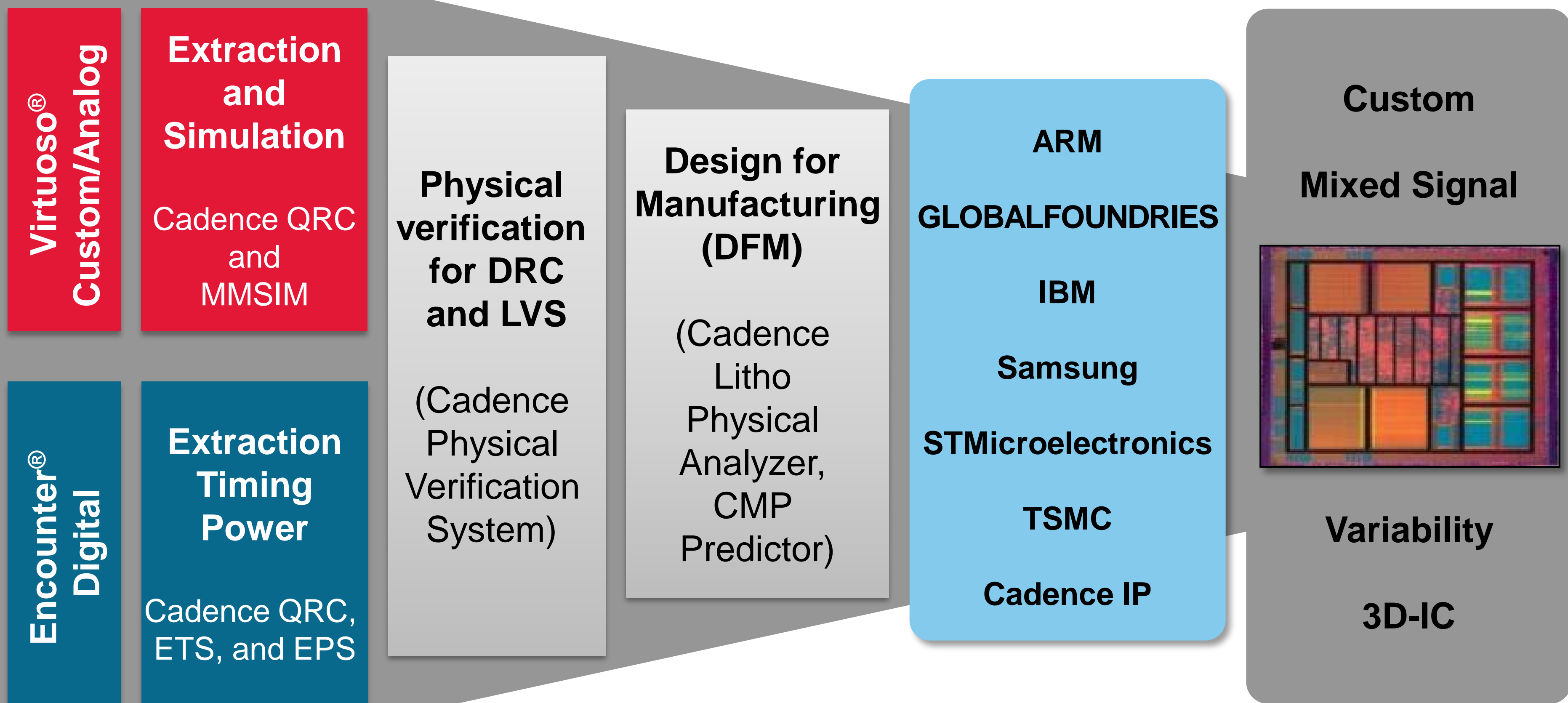
March 17, 2012 Andy Beckley; March Madness Ohio State vs Gonzaga tip-off in Pittsburgh; taken with Apple iPhone 4s with dual core A5 processor; 40nm low-power process.

 © 2012 Cadence Design Systems, Inc. All rights reserved.

cadence®

Cadence 20nm solution

Tools + ecosystem + methodology = design success



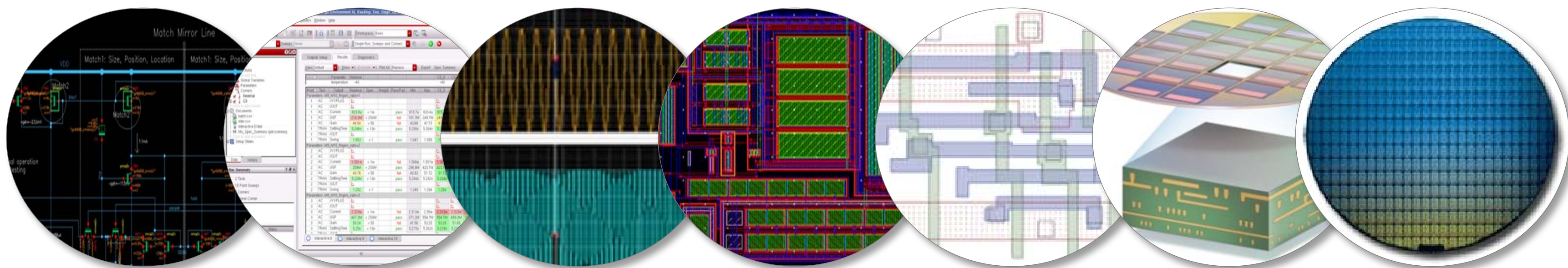
© 2012 Cadence Design Systems, Inc. All rights reserved.

cādence®

Summary

Measure early and often for first-pass success

- Mobility trends will continue to push the technology
- A combination of new tools, devices and methodologies will manage the complex physics
- Industry collaboration will be central to 20nm success
- 20nm is still evolving but don’t let that stop you from the exploration
- Get ready – 14nm will be upon us before you know it



© 2012 Cadence Design Systems, Inc. All rights reserved.

cādence®

cadence®