CALL FOR PAPERS
ASQED 2013
5th Asia Symposium & Exhibits on QUALITY ELECTRONIC DESIGN

Paper Submission Deadline: April 23, 2013
Acceptance Notifications: May 23, 2013
Final Camera-Ready paper: June 16, 2013

A pioneer and leading interdisciplinary electronic design and semiconductor conference in Asia, ASQED accepts and promotes papers in following areas:

- Advanced IC Packaging Technology
- Advanced 3D ICs & 3D Packaging
- FPGA Architecture, Design, and CAD
- Test & Verification
- Design for Test and BIST
- Photovoltaic Technology & Manufacturing
- PCB and PWB Technology & Manufacturing
- Circuit & System Design
- EDA Methodologies, Tools, Flows
- Semiconductor & Nano Technology
- Micro/NANO-Electro-Mechanical System (MEMS/NEMS)
- Bio Electronics Innovations

Papers are published in ASQED proceedings and IEEE Xplore. Please visit www.asqed.com for more information.

Sponsoring Organizations:

IEEE
isQED
InnovoTek
IPC
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ISQED 2014
15th International Symposium & Exhibits on
QUALITY ELECTRONIC DESIGN

March 2014. Santa Clara, CA, USA

Paper Submission Deadline: Sept. 12, 2013
Acceptance Notifications: November 25, 2013
Final Camera-Ready paper: January 10, 2014

A pioneer and leading interdisciplinary electronic design and semiconductor conference, ISQED accepts and promotes papers in following areas:

- System-level Design, Methodologies & Tools
- FPGA Architecture, Design, and CAD
- Design of Embedded Systems
- Advanced 3D ICs & 3D Packaging, and Co-Design
- Robust & Power-conscious Circuits & Systems
- Emerging/Innovative Device Technologies and Design Issues
- Design of Reliable Circuits and Systems
- IP Design, quality, interoperability and reuse
- Design Verification and Design for Testability
- Physical Design, Methodologies & Tools
- EDA Methodologies, Tools, Flows
- Design for Manufacturability/Yield & Quality
- Effects of Technology on IC Design, Performance, Reliability, and Yield

Papers from past ISQED events are published in ISQED proceedings and IEEE Xplore. Please visit www.isqed.org for more information.
On behalf of the ISQED 2013 conference and technical committees, we are pleased to welcome you to the 14th International Symposium on Quality Electronic Design, ISQED 2013. This conference is the premier multidisciplinary design and design automation conference, aimed at bridging the gap between and integration of, electronic design tools and processes, integrated circuit technologies, processes, and manufacturing, to achieve design quality.

ISQED continues to provide and foster a unique opportunity to participants to interact and engage themselves in cutting edge tutorials, presentations, and plenary sessions. The conference topics provide a holistic approach while covering a wide variety of issues impacting the quality of electronic design. We thank you for your support and anticipate your continued participation through the coming years.

All the technical presentations, plenary sessions, tutorials and related events will take place on March 4-6 at the Network Meeting Center in Santa Clara, CA. Please refer to the conference booklet and/or ISQED website for program details.

We would like to thank the ISQED 2013 corporate sponsors: IBM, InnovoTek, Mentor Graphics, Synopsys, and Silicon Valley Technical Institute, and for their valuable support of this conference.

Welcome to another stellar year of ISQED! It couldn’t have happened without your support and participation.

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Rasit Topaloglu  
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Plenary Chair

Rajiv Joshi  
Plenary Co-Chair

Pallab Chatterjee  
Affiliate Relations

Paul Wesling  
Publication Chair

Ali A. Iranmanesh  
ISQED Founder
4A.1
Peak Power Reduction of a Sensor Network Processor
Fabricated With Deeply Depleted Channel Transistors in 65nm Technology

Kentaro Kawakami, Takeshi Shiro, Hironobu Yamasaki, Katsuhiro Yoda, Hiroaki Fujimoto,
Kenichi Kawasaki, Yasuhiro Watanabe
Fujitsu Laboratories Ltd.

4A.3
Cost-effective 45nm 6T-SRAM Reducing 50mV Vmin and 53% Standby
Leakage with multi-Vt Asymmetric Halo MOS and Write Assist Circuitry

Koji Nii¹, Makoto Yabuuchi¹, Hidehiro Fujiwara¹, Yasumasa Tsukamoto¹, Yuichiro Ishii¹,
Tetsuya Matsumura¹, Yoshio Matsuda²
¹Renesas Electronics Corporation, ²Kanazawa University

3A.1
LMgr: A Low-Memory Global Router with Dynamic
Topology Update and Bending-Aware Optimum Path Search

Jingwei Lu¹ and Chiu-Wing Sham²
¹University of California, San Diego,
²The Hong Kong Polytechnic University

* Authors of best papers are honored during the luncheon on Tuesday March 5
### ISQED 2013 Organizing Committee

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<thead>
<tr>
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TECHNICAL PROGRAM COMMITTEES

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Custom Analog & Mixed Signal Design Services

info@SiVDF.com
GENERAL INFORMATION

ISQED 2013
GENERAL INFORMATION

March 4-6, 2013
Techmart
5101 Great America Parkway, Santa Clara, CA

TUTORIALS

Monday Tutorials
Monday, March 4, 9:00am-6:00pm
Room: Fremont

Chair & Moderator:
Rasit Topaloglu - IBM

IC Technology at New Nodes Made Easy
Dr. Alvin Loke, AMD
**********

Physical Design Considerations for Silicon Nanophotonic Circuits
Dr. Ron Ho, Oracle
**********

Design of 3D ICs: From Concept to Practice
Prof. Sung Kyu Lim, Georgia Tech
**********

Computer Architecture Design Utilizing Novel Memories
Prof. Engin Ipek, University of Rochester
**********

Hardware Security and Implications on Design Flows
Prof. Ozgur Sinanoglu, NYU Abu Dhabi

Holistic Power Management: The Future of Handhelds and other Low Power Devices
Dr. Vinod Viswanath, Realintent
Rajeev D. Muralidhar, Intel
Hari Seshadri, Intel

KEYNOTE SPEECHES

Plenary Session 1P
Tuesday, March 5, 8:30am - 10:00am
Room: Silicon Valley

The Changing Device Technology
Prof. Chenming Hu
TSMC Distinguished Professor of Graduate School
University of California, Berkeley
*******

Sustaining Innovation for Smarter Computing in Data Centers
Brad L Brech
Member of the IBM Academy of Technology
IBM
*******

System Level Perspective on Semiconductors for Intelligent Networks
Bill Swift
Vice President of Engineering
Cisco Systems

ISQED LUNCHEON

Tuesday, March 5, 12:00pm-12:45pm
Room: Silicon Valley

ISQED AWARDS CEREMONY

Tuesday, March 5, 12:00pm-12:45pm
Room: Silicon Valley

ISQED Best Paper Awards

Recipients of the ISQED 2013 Best Paper Award will be recognized during the ISQED luncheon on Tuesday. List of best papers is shown in Page 2 of this document.
LUNCHEON KEYNOTE SPEECH
Tuesday, March 5, 12:45pm-1:30pm
Room: Silicon Valley

Trends in Analog/ Mixed-Signal Design Tools
Ed Petrus
Director of Custom Architecture, DSM division
Mentor Graphics

KEYNOTE SPEECHES

Plenary Session 2P
Wednesday, March 6, 9:00am - 10:00am
Room: Silicon Valley

Physical-Aware, High-Capacity RTL Synthesis for Advanced Nanometer Designs
Sanjiv Taneja
Vice President, Product Engineering, Front End Design
Cadence Design Systems

The Lifecycle Of Audio Products, Consumer versus Professional
Perry Goldstein
Director of Sales & Marketing
Marshall Electronics

TECHNICAL SESSIONS
There are a total of 18 technical sessions held on Tuesday and Wednesday. Technical sessions are held in the format of 3 parallel tracks in San Jose, New Almaden, Morgan Hill rooms.

Poster Papers & Mixer
Poster display will take place on Tuesday afternoon 5:00pm-7:00pm in the Atrium area outside of New Almaden/Monte Sereno rooms. Authors will be available to discuss their works and to answer questions. Refreshments will be served.

ON-SITE REGISTRATION
Tentative time schedule of on-site registration is as follows:
Monday, March 4  7:30am-4:00pm
Tuesday, March 5  8:00am-5:00pm
Wednesday, March 6  8:00am-1:00pm

Registration desk is located on the 1st floor Atrium beside the Silicon Valley room.

Co-located Events

3rd Interdisciplinary Engineering Design Education Conference
March 4-5
Rooms: Silicon Valley, San Jose, New Almaden, Fremont
www.IEDEC.org

Sensors - Technology, Design, and Application Conference
March 6
Rooms: Fremont
www.SensorsCon.org
Techmart Meeting Center
5201 Great America Parkway
Santa Clara, California  95054
# ISQED 2013 Program at a Glance

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<tr>
<th>Date</th>
<th>Time</th>
<th>Tutorials</th>
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<tr>
<td><strong>Monday 3/4/2013</strong></td>
<td>9:00AM-5:00PM</td>
<td><strong>Best Design Practices for Modern Integrated Circuits</strong></td>
</tr>
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</table>
| **Tuesday 3/5/2013** | 8:15AM-10:00AM | **Plenary Session 1P** (Room: Silicon Valley)  
**Keynote Speeches by:**  
Chenming Hu - University of California, Berkeley,  
Brad L Brech - IBM,  
Bill Swift - Cisco Systems |
| 10:00AM-10:20AM | **Morning Break**                               |
| 10:20AM-12:00PM | **Session 1A**  
3D Circuits and Packaging  
Room: San Jose |
| 10:20AM-12:00PM | **Session 1B**  
Aging Aware Design  
Room: New Almaden |
| 10:20AM-12:00PM | **Session 1C**  
3D Integrated Circuits  
Room: Morgan Hill |
| 12:00PM-12:45PM | **ISQED Luncheon**  
Best Paper Awards, Committee Recognition Awards  
(Room: Silicon Valley) |
| 12:45PM-1:30PM | **Luncheon Keynote**  
Trends in Analog/Mixed-Signal Design Tools  
Ed Petrus - Mentor Graphics |
| 1:30PM-3:30PM | **Session 2A**  
System Level Design/Optimization for Energy  
Room: San Jose |
| 1:30PM-3:30PM | **Session 2B**  
Low Power System Design  
Room: New Almaden |
| 1:30PM-3:30PM | **Session 2C**  
Emerging Devices and Design Techniques  
Room: Morgan Hill |
| 3:30PM-3:50PM | **Afternoon Break**                               |
| 3:50PM-5:30PM | **Session 3A**  
Advances in Routing and Timing  
Room: San Jose |
| 3:50PM-5:30PM | **Session 3B**  
Robust Design for Fault Tolerance  
Room: New Almaden |
| 3:50PM-5:30PM | **Session 3C**  
CAD for 3D ICs  
Room: Morgan Hill |
| **Wednesday 3/6/2013** | 8:15AM-10:00AM | **Plenary Session 2P** (Room: Silicon Valley)  
**Keynote Speeches by:**  
Sanjiv Taneja - Cadence Design Systems,  
Perry Goldstein - Marshall Electronics |
| 10:00AM-10:20AM | **Morning Break**                               |
| 10:20AM-12:00PM | **Session 4A**  
Low Power Technologies  
Room: San Jose |
| 10:20AM-12:00PM | **Session 4B**  
Silicon Diagnosis and Test  
Room: New Almaden |
| 10:20AM-12:00PM | **Session 4C**  
New Ideas in CAD  
Room: Morgan Hill |
| 12:00PM-1:30PM | **Lunch Break**                               |
| 1:30PM-3:30PM | **Session 5A**  
System Design Methodologies and Automation  
Room: San Jose |
| 1:30PM-3:30PM | **Session 5B**  
Manufacturing and Modeling Issues of Nanoscale CMOS  
Room: New Almaden |
| 1:30PM-3:30PM | **Session 5C**  
Multi-Core and Multi-Processor Systems  
Room: Morgan Hill |
| 3:30PM-3:50PM | **Afternoon Break**                               |
| 3:50PM-5:30PM | **Session 6A**  
Issues and Challenges in Characterization and Power Integrity for Nanometer Technologies  
Room: San Jose |
| 3:50PM-5:30PM | **Session 6B**  
Low Power Circuits  
Room: New Almaden |
| 3:50PM-5:30PM | **Session 6C**  
Reliable System Design  
Room: Morgan Hill |
MONDAY TUTORIALS

Monday, March 4, 2013
9:00AM~6:00PM
Room: Fremont

Best Design Practices for Modern Integrated Circuits

Chair & Moderator:
Rasit Topaloglu, IBM

Presenters:
Dr. Alvin Loke, AMD
Dr. Ron Ho, Oracle
Prof. Sung Kyu Lim, Georgia Tech
Prof. Engin Ipek, University of Rochester
Prof. Ozgur Sinanoglu, NYU Abu Dhabi
Dr. Vinod Viswanath, Real Intent
Rajeev D. Muralidhar, Intel
Hari Seshadri, Intel

While traditional scaling will take us a few more nodes, drastic changes in the way we design integrated circuits may be needed. For example, 3D interconnects may be needed to decrease communication costs, along with a more aggressive on-chip optical integration.

The tutorial will start by illustrating how AMD designers tackle current advanced nodes. It will then follow with a talk where Oracle researchers show how to integrate optics on chip. Next, Georgia Tech researchers present on design tools and models to design and measure 3D chips.

Novel integrated circuit design furthermore may bring changes in computing architecture. Novel memory techniques may be used as illustrated by a talk from University of Rochester. The tutorial will continue by a talk from NYU-Abu Dhabi on the trending topic of hardware security and how to secure designs and design flows. Furthermore, power management will continue to become essential and work by RealIntent and Intel will be presented to conclude the tutorial.

Tutorial 1
9:00AM-10:40AM

IC Technology at New Nodes Made Easy

Presenter:
Dr. Alvin Loke, AMD

Despite increasing economic and technical challenges in scaling CMOS, we continue to witness unprecedented performance with 22-nm fully-depleted tri-gate devices now in production. This tutorial offers a summary of how CMOS device technology has progressed over the past two decades. We will review MOS devices and short-channel fundamentals to motivate how device architectures in production have evolved to incorporate elements such as halos and spaces, mechanical strain engineering, high-K dielectric and metal gate, fully-depleted architectures, and finally trigate fins.
Silicon nanophotonic links have recently captured the attention of designers interested in their potential energy, area, and performance advantages over electrical links. An abstracted view of a silicon nanophotonic link is straightforward, and lends itself nicely to simple and useful system models. Unsurprisingly, however, the realities of building operating photonic links contains several subtleties that are worth understanding. In this talk we will introduce photonic links, discuss their basic operation, and describe the principal physical challenges in their use. These will include resonant ring modulator tradeoffs, ring thermal stability control, efficient receiver designs, and receiver BER vs SNR.

This tutorial covers the design of through-silicon-via (TSV) based three dimensional integrated circuits. It includes details of numerous “manufacturing-ready” GDSII-level layouts of TSV-based 3D ICs, developed with CAD tools covered in this tutorial. Participants will also learn the sign-off level analysis methodologies for timing, power, signal integrity, and thermo-mechanical reliability for 3D IC designs. Coverage also includes various design-for-manufacturability (DFM), design-for-reliability (DFR), and design-for-testability (DFT) techniques that are considered critical to the 3D IC design process.

Continued advances in the performance of computer systems depend critically on the industry’s ability to scale memory density and capacity for decades to come. Unfortunately, scaling of semiconductor memories is increasingly affected by fundamental limits in deep-submicron process technologies. The ITRS projection predicts difficulties in scaling key DRAM process parameters, and the SIA Roadmap projects difficulties scaling Flash past the 20nm node; at 21 nanometers, small numbers of electrons (e.g., 10) tunneling from the floating gate will cause a Flash cell to lose its state. Recent work differentiates charge memories (such as DRAM, SRAM, and Flash memory), which use electric carriers to store the state of a bit, from resistive memories, which use atomic arrangements to set the resistance of a memory cell to store information. Resistive memories, which include phase-change Memory (PCM), Ferroelectric RAM (FeRAM), Spin-Torque Transfer Magnetoresistive RAM (STTMRAM), and Resistive RAM (RRAM), the latter of which includes memristors, are all candidates to succeed charge memories if and when charge memories reach fundamental limits.
To start exploiting the scalability of resistive memories, however, resistive memories must first be architected to address relatively long latencies, high energy writes, and finite endurance. In the first half of this talk, I will examine resistive computation, an architectural technique that aims at developing a new class of power-efficient, scalable systems by migrating much of the functionality of a modern microprocessor from CMOS to STTMRAM. The key idea is to implement most of the on-chip storage and combinational logic using scalable, leakage-resistant RAM arrays and lookup tables (LUTs) constructed from STT-MRAM to lower leakage, thereby allowing many more active cores under a fixed power budget than a pure CMOS implementation could afford. I will then introduce recent work on architecting PCM as a scalable, persistent DRAM replacement. Software cognizant of this newly provided persistence can provide qualitatively new capabilities. For example, system boot/hibernate will be perceived as instantaneous; application check pointing will be inexpensive; file systems will provide stronger safety guarantees. Hence, this work is a first step toward a fundamentally new memory hierarchy with deep implications across the hardware-software interface.

### Tutorial 5
3:40PM-4:50PM

#### Hardware Security and Implications on Design Flows

**Presenter:**
**Prof. Ozgur Sinanoglu, NYU Abu Dhabi**

Today's System on Chip (SoC) is being incorporated with digital, analog, radio frequency, photonic and other devices. More recently, sensors, actuators, and biochips are also being integrated into these already powerful SoCs. On one hand, SoC integration has been enabled by advances in mixed system integration and the increase in the wafer sizes (currently about 300 mm and projected to be 450mm by 2018). Consequently, the cost per chip of such SOCs has reduced. On the other hand, support for multiple capabilities and mixed technologies has increased the cost of ownership of advanced foundries. For instance, the cost of owning a foundry will be $5 billion in 2015. Consequently, only large commercial foundries now manufacture such high performance, mixed system SoCs especially at the advanced technology nodes. Absent the economies of scale, many of the design companies cannot afford owning and acquiring expensive foundries and hence, outsource their design fabrication to these "one-stop-shop" foundries. This globalization of Integrated Circuit (IC) design flow has introduced security vulnerabilities. If a design is fabricated in a foundry that is outside the direct control of the (fabless) design house, reverse engineering, malicious circuit modification, and Intellectual Property (IP) piracy are possible. An attacker, anywhere in this design flow, can reverse engineer the functionality of an IC/IP, and steal and claim ownership of the IP. An untrusted IC foundry may overbuild ICs and sell the excess parts in the gray market. Rogue elements in the foundry may insert malicious circuits (hardware Trojans) into the design without the designer's knowledge. Because of these and similar hardware-based attacks, the semiconductor industry loses $4 billion annually. In this talk, we cover Design-for-Trust techniques to regain trust in manufactured hardware. A popular approach to thwart these attacks is to conceal (encrypt) the functionality of an IC while it passes through the different, potentially untrustworthy phases of the global design flow, giving the control back to the designer. We will survey the different approaches to encrypting the functionality of a design. We will then discuss how IC (testing) fault analysis techniques can be used both as a defense aid and as an attack tool. On one hand, we will show how a designer can use VLSI fault analysis to aid the design encryption process. On the other hand, we will show that the fault analysis can be used as a weapon by an attacker to obtain the design functionality. We will also cover side channel measurement based Trojan detection approaches.
Power efficiency is a growing concern to all aspects of computing systems ranging from the very small, highly integrated System-on-a-Chip (SoC) based handheld devices to larger systems including servers and many-core high performance computing systems. In order to maximize power optimization, the future trend is to perform holistic power management across different levels of design abstractions. This means that embedded/SoC systems that are power optimized will now be application and workload aware. The O/S will be aware of micro-architectural features to program the device in certain power and sleep states.

In this tutorial, we will address the challenges of holistic power management. In particular we'll cover the challenges of a unified specification of power intent across all design abstraction levels; power optimization and holistic power management techniques; and, the challenges of verification of such a system. All three presenters have many years of experience with Intel’s low power design methodologies, challenges and state-of-the-art technology. The tutorial will be amply supplemented with real life examples from Intel’s experience in designing some of its latest handheld devices.
IC device technology has entered a new era of bold changes. FinFET may be the best known new technology. Ultra-thin-body is an attractive new technology. Even bolder changes are envisioned and needed to empower the semiconductor industry.

About Chenming Hu
Chenming Hu is the TSMC Distinguished Professor of UC Berkeley. He was formerly the Chief Technology Officer of TSMC. He is known for developing the 3D transistor, FinFET, that can be scaled beyond 10nm. He also developed the international-standard MOSFET model used by most IC companies since 1997. He has received the IEEE Andrew Grove Award, Solid State Circuits Award, Nishizawa Medal, and UC Berkeley's highest honor for teaching--the Berkeley Distinguished Teaching Award.
Better business economics and accelerated business velocity are the two most important factors to the CxO's of clients moving forward. They see technology as a key to their success in meeting both goals in this fast moving world. Smarter Computing is about successfully overcoming the challenges of new analytics, cloud, big data and security requirements through use of appropriate technologies. In the end, doing things Smarter and Faster are the driving factors for the Next Generation of Data Centers.

About Brad L Brech

Brad Brech is a Distinguished Engineer in the Systems and Technology Division of IBM in the office of the CTO. He is currently leader of the Systems and Technology Architecture board, where his responsibilities include technical strategy, energy efficient computing, intellectual property development and technical vitality for IBM STG. Brad joined IBM in 1982. He has made many contributions to the mid-range systems from the System/36, AS/400, and Power Systems families in roles from logic design, Chief Firmware architect, and Chief Systems SW Architect. As one of the drivers behind IBM's Project Big Green in 2006, he focused on development and delivery of technologies that help customers increase the level of energy efficiency in their data centers. Brad is an IBM Distinguished Engineer, a member of the IBM Academy of Technology, and a board member of The Green Grid. He has many IBM awards, serves on leadership team for the IBM Academy of Technology, and other corporate technical vitality teams. He has published several papers and reports, holds several patents. He is an alumnus Stevens Institute of Technology. Outside of work he spends time with his family and working on the boards of 3 charitable organizations.
The impact of the internet on our lives is accelerating and the innovation required to build the technologies and products for these networks is accelerating with it. Innovations at the semiconductor level, board level, and system level in support of new requirements on signaling, packaging, operation, quality, and reliability are taking analytical, simulation, and compute technologies to new limits. In this keynote, Cisco VP of Engineering Bill Swift highlights technology and business trends, as well as innovation drivers for semiconductor technology in the industry and at Cisco enabling products and solutions for intelligent networks.

About Bill Swift
Bill Swift is the Vice President of Engineering for the Silicon Engineering team in the Cisco Systems Engineering organization. He is currently responsible for silicon development engineering for the service provider, enterprise, and high end switching based products. Bill joined Cisco in 1994 and has held a number of hardware, software and system engineering leadership positions across multiple technologies, developments and platforms including the highly successful 7500, 12K, MGX, CRS, and ASR9K platforms. Prior to that, Bill has led the initial development and integration of many key service provider technologies into Cisco routing products such as packet over sonet, channelized interfaces, IP over optical, and IP over DWDM. Before joining Cisco, Bill worked in product development teams at Tandem Computers on non-stop computing, GTE Telenet on X.25 packet switching and American Satellite Company on satellite communications systems. Bill holds both Bachelor's and Master's degrees in Electrical Engineering from The Johns Hopkins University at Baltimore, Maryland.
SESSION 1A
Tuesday March 5, 2013
Three Dimensional Circuits and Packaging

Chair: Farhang Yazdani, BroadPak
Co-Chair: John Park, Mentor Graphics

10:20AM
1A.1 Hetero2 3D Integration: A Scheme for Optimizing Efficiency/Cost of Chip Multiprocessors
Shivam Priyadarshi¹, Niket Choudhary¹, Brandon Dwiel¹, Ankita Upreti¹, Eric Rotenberg², Rhett Davis³, Paul Franzon²
¹Graduate Student, North Carolina State University, Raleigh, ²Professor, North Carolina State University, Raleigh, ³Associate Professor, North Carolina State University, Raleigh

10:40AM
1A.2 Effective Thermal Control Techniques for Liquid-Cooled 3D Multi-Core Processors
Yue Hu, Shaoming Chen, Lu Peng, Edward Song, Jin-Woo Choi
Louisiana State University

11:00AM
1A.3 Reliability-Constrained Die Stacking Order in 3DICs Under Manufacturing Variability
Tuck-Boon Chan, Andrew B. Kahng, Jiajia Li
University of California, San Diego

11:20AM
1A.4 Analytical Modeling and Numerical Simulations of Temperature Field in TSV-based 3D ICs
Yuriy Shiyanovskii¹, Chris Papachristou¹, Cheng-Wen Wu²
¹Case Western Reserve University, ²National Tsing Hua University / Industrial Technology Research Institute

11:40AM
1A.5 New Electrical Design Verification Approach for 2.5D/3D Package Signal and Power Integrity
Nozad Karim
Amkor Technology

SESSION 1B
Tuesday March 5, 2013
Aging aware design

Chair: Riza Naseer, Intel
Co-Chair: Srinivas Bodapati, Intel

10:20AM
1B.1 An Arbitrary Stressed NBTI Compact Model for Analog/Mixed-Signal Reliability Simulations
Jinbo Wan and Hans Kerkhoff
Testable Design and Testing of Integrated Systems Group, University of Twente, Netherlands
Impacts of NBTI and PBTI Effects on Ternary CAM
Yen-Han Lee, Ing-Chao Lin, Sheng-Wei Wang
National Cheng Kung University, Taiwan

On Predicting NBTI-induced Circuit Aging by Isolating Leakage Change
Yinhe Han\textsuperscript{1}, Song Jin\textsuperscript{1}, Jiebing Qiu\textsuperscript{1}, Qiang Xu\textsuperscript{2}, Xiaowei Li\textsuperscript{1}
\textsuperscript{1}Institute of Computing Technology, Chinese Academy of Sciences, \textsuperscript{2}The Chinese University of Hong Kong

Aging-aware Timing Analysis Considering Combined Effects of NBTI and PBTI
Saman Kiamehr, Farshad Firouzi, Mehdi B. Tahoori
Karlsruhe Institute of Technology (KIT)

Flexible Data Allocation for Scratch-pad Memories to Reduce NBTI Effects
Dimitra Papagiannopoulou, Patipan Prasertsom, Iris Bahar
Brown University

SESSION 1C
Tuesday March 5, 2013
3D Integrated Circuits

Runtime 3-D Stacked Cache Management for Chip-Multiprocessors
Jongpil Jung\textsuperscript{1}, Kyungsu Kang\textsuperscript{2}, Giovanni De Micheli\textsuperscript{2}, Chong-Min Kyung\textsuperscript{1}
\textsuperscript{1}KAIST, \textsuperscript{2}EPFL

A Co-Synthesis Methodology for Power Delivery and Data Interconnection Networks in 3D ICs
Nishit Kapadia and Sudeep Pasricha
Colorado State University

Temperature Aware Thread Migration in 3D Architecture with Stacked DRAM
Dali Zhao\textsuperscript{1}, Houman Homayoun\textsuperscript{2}, Alex V. Veidenbaum\textsuperscript{1}
\textsuperscript{1}University of California, Irvine, \textsuperscript{2}George Mason University
A System-level Solution for Managing Spatial Temperature Gradients in Thinned 3D ICs
Arunachalam Annamalai, Raghavan Kumar, Arunkumar Vijayakumar, Sandip Kundu
University of Massachusetts Amherst

Vertically-Addressed Test Structures (VATS) for 3D IC Variability and Stress Measurements
Conor O'Sullivan, Peter Levine, Siddharth Garg
University of Waterloo

ISQED Luncheon
Tuesday March 5
Room: Silicon Valley
12:00PM-1:30PM

ISQED 2013 Award Ceremony
12:00PM-12:45PM

Best Paper Awards
Recognition Awards
Luncheon Keynote Speech

Tuesday March 5
Room: Silicon Valley
12:45PM-1:30PM

Trends in Analog/ Mixed-Signal Design Tools

Ed Petrus
Director of Custom Architecture, DSM division
Mentor Graphics

Designers who are creating analog/mixed-signal intensive designs are faced with a complex set of challenges. They need to have a high degree of confidence that their designs will be manufacturable and perform to specification in the foundry process before they even consider completing a design in an advanced process node. These ICs are often assembled using multiple resources and various design methodologies including IP reuse, top-down design, and bottom-up design. In the keynote, Ed Petrus discusses the unique challenges of designing custom ICs targeted for smaller manufacturing geometries, and talks about the tools being successfully deployed today while giving insights into what is on the horizon in terms of new functionality.

About Ed Petrus
Ed Petrus is the Director of Custom Architecture for the Deep Submicron division of Mentor Graphics. Before coming to Mentor, Ed was the co-founder of Ciranova where he helped build breakthrough products for automating custom IC physical design. These products are in deployment with design teams at top semiconductor companies using sub-40nm processes. Previous to Ciranova, Ed spent 10 years at Cadence Design Systems where he was an architect and developer of SKILL and other components of Cadence’s DFiI technology. Before Cadence, Ed started his career in EDA as a software engineer at Daisy Systems. Ed has held engineering management positions at Military Advantage and Nanomix. Ed holds B.Sc. and M.Sc. degrees in Computer Science from the University of Essex in the United Kingdom.
SESSION 2A
Tuesday March 5, 2013
System Level Energy

Chair: Lech Jozwiak, Eindhoven University of Technology
Co-Chair: Rajesh Berigei, Texas Instruments

1:30PM
2A.1
Energy-Aware Coarse-Grained Reconfigurable Architectures using Dynamically Reconfigurable Isolation Cells
Syed M. A. H. Jafri¹, Ozan Zeki Bag¹, Ahmed Hemani¹, Nasim Farahini¹, Kolin Paul¹, Juha Plosila², Hannu Tenhunen¹
¹Royal Institute of Technology (KTH) Sweden, ²University of Turku (UTU) Finland

1:50PM
2A.2
Hybrid CMOS-TFET based Register Files for Energy-Efficient GPGPUs
Zhi Li, Jingweijia Tan, Xin Fu
University of Kansas

2:10PM
2A.3
Compiler-assisted Leakage Energy Optimization of Media Applications on Stream Architectures
Shan Cao¹, Zhaolin Li², Zhixiang Chen¹, Guoyue Jiang¹, Shaojun Wei¹
¹Institute of Microelectronics, Tsinghua University, ²Tsinghua National Laboratory for Information Science and Technology, Research Institute of Information Technology, Tsinghua University

2:30PM
2A.4
On a Rewriting Strategy for Dynamically Managing Power Constraints and Power Dissipation in SoCs
Vinod Viswanath¹, Rajeev Muralidhar², Harinarayanan Seshadri², Jacob Abraham³
¹Real Intent Inc., ²Intel Corp., ³University of Texas at Austin

2:50PM
2A.5
Sustainable Dual-Level DVFS-enabled NoC with On-chip Wireless Links
Jacob Murray, Rajath Hegde, Teng Lu, Partha Pande, Behrooz Shirazi
Washington State University
On the Selection of Adder Unit in Energy Efficient Vector Processing
Ivan Ratkovic, Oscar Palomar, Milan Stanic, Osman S. Unsal, Adrian Cristal, Mateo Valero
Barcelona Supercomputing Center

SESSION 2B
Tuesday March 5, 2013
Low Power System Design

Chair: Amin Khajeh Djahromi, Intel
Co-Chair: Krishnan Sundaresan, Oracle America, Inc.

1:30PM
2B.1
Low-Energy Digital Filter Design Based on Controlled Timing Error Acceptance
Ku He, Andreas Gerstlauer, Michael Orshansky
The University of Texas at Austin

1:50PM
2B.2
A Novel and Efficient Method for Power Pad Placement Optimization
Ting Yu and Martin. D. F. Wong
UIUC

2:10PM
2B.3
Min-Cut Based Leakage Power Aware Scheduling in High-Level Synthesis
Nan Wang¹, Song Chen², Takeshi Yoshimura¹
¹Graduate School of IPS, Waseda University, ²University of Science and Technology of China

2:30PM
2B.4
Hierarchical Dynamic Power Management Using Model-Free Reinforcement Learning
Yanzhi Wang¹, Maryam Triki², Xue Lin¹, Ahmed Ammari², Massoud Pedram¹
¹University of Southern California, ²Carthage University
2:50PM
2B.5
Accurate Architecture-level Thermal Analysis Methods for MPSoC with Consideration for Leakage Power Dependence on Temperature
Jiaqi Yan, Zuying Luo, Liang Tang
Beijing Normal University, 19 XinJieKouWai Street, Beijing, P.R.CHINA

3:10PM
2B.6
Application-Driven Power Efficient ALU Design Methodology for Modern Microprocessors
Na Gong¹, Jinhui Wang², Ramalingam Sridhar³
¹University at Buffalo, SUNY, ²VLSI and System Lab, Beijing University of Technology

SESSION 2C
Tuesday March 5, 2013
Emerging Devices and Design Techniques

Chair: Paul Tong, Pericom Semiconductor
Co-Chair: Bao Liu, UT San Antonio

1:30PM
2C.1
Low Power and Compact Mixed-Mode Signal Processing Hardware using Spin-Neurons
Mrigank Sharad¹, Deliang Fan², Kaushik Roy²
¹Purdue University, ²Purdue University

1:50PM
2C.2
System-level Optimization and Benchmarking for InAs Nanowire Based Gate-All-Around Tunneling FETs
Chenyun Pan, Ahmet Ceyhan, Azad Naeemi
Georgia Institute of Technology

2:10PM
2C.3
Impact of Conventional and Emerging Interconnects on the Circuit Performance of Various Post-CMOS Devices
Ahmet Ceyhan and Azad Naeemi
Georgia Institute of Technology
2:30PM
2C.4
Reducing IR Drop in 3D Integration to Less Than 1/4 Using Buck Converter on Top Die (BCT) Scheme
Yasuhiro Shinozuka¹, Hiroshi Fuketa¹, Koichi Ishida¹, Futoshi Furuta², Kenichi Osada², Kenichi Takeda², Makoto Takamiya¹, Takayasu Sakurai¹
¹University of Tokyo, ²Association of Super-Advanced Electronics Technologies (ASET)

2:50PM
2C.5
Energy-Efficient Spin-Transfer Torque RAM Cache Exploiting Additional All-Zero-Data Flags
Jinwook Jung, Yohei Nakata, Masahiko Yoshimoto, Hiroshi Kawaguchi
Kobe University

3:10PM
2C.6
Design Of Ultra High Density And Low Power Computational Blocks using Nano-Magnets
Mrigank Sharad, Karthik Yogendra, Kon-Woo Kwon, Kaushik Roy
Purdue University

SESSION 3A
Tuesday March 5, 2013
Advances in Routing and Timing
Chair: Mark Young, Texas Instruments
Co-Chair: Andre Reis, Universidade Federal do Rio Grande do Sul

3:50PM
3A.1
LMgr: A Low-Memory Global Router with Dynamic Topology Update and Bending-Aware Optimum Path Search
Jingwei Lu¹ and Chiu-Wing Sham²
¹Department of Computer Science and Engineering, University of California, San Diego, ²Department of Electronic and Information Engineering, The Hong Kong Polytechnic University
4:10PM
3A.2
Vision-inspired Global Routing for Enhanced Performance and Reliability
Jun Yong Shin, Nikil Dutt, Fadi Kurdahi
UC Irvine

4:30PM
3A.3
Crosstalk Timing Windows Overlap in Statistical Static Timing Analysis
Hanif Fatemi and Peivand Tehrani
Synopsys, Inc.

4:50PM
3A.4
Multi-objective Optimization Algorithm for Efficient Pin-constrained Droplet Routing Technique in Digital Microfluidic Biochip
Soumyajit Chatterjee, Hafizur Rahaman, Tuhina Samanta
Bengal Engineering & Science University, Shibpur, Howrah, India

5:10PM
3A.5
Advances in Wire Routing
Martin D.F. Wong
University of Illinois at Urbana-Champaign

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SESSION 3B
Tuesday March 5, 2013
Global Circuit Design

Chair: Abhilash Goyal, Oracle
Co-Chair: Riaz Naseer, Intel

3:50PM
3B.1
Effectiveness of Hybrid Recovery Techniques on Parametric Failures
Shrikanth Ganapathy¹, Ramon Canal¹, Antonio Gonzalez², Antonio Rubio³
¹Department of Computer Architecture, Universitat Politecnica de Catalunya, ²Intel Barcelona Research Center, ³Department of Electronic Engineering, Universitat Politecnica de Catalunya
4:10PM
3B.2
Fast Reliability Exploration for Embedded Processors via High-level Fault Injection
Zheng Wang, Chao Chen, Anupam Chattopadhyay
MPSoC Architectures, RWTH-Aachen

4:30PM
3B.3
Analysis and Reliability Test to Improve the Data Retention Performance of EPROM Circuits
Jiyuan Luan and Michael DiVita
Texas Instruments

4:50PM
3B.4
Enabling Sizing for Enhancing the Static Noise Margins
Valeriu Beiu¹, Azam Beg¹, Walid Ibrahim¹, Fekri Kharbash¹, Massimo Alioto²
¹UAEU, ²U Michigan Ann Arbor

5:10PM
3B.5
SRAM Bit-line Electromigration Mechanism and its Prevention Scheme
Zhong Guan¹, Malgorzata Marek-Sadowska¹, Sani Nassif²
¹Dept. of Electrical and Computer Engineering, UC Santa Barbara, ²IBM Austin Research Laboratory

SESSION 3C
Tuesday March 5, 2013
CAD for 3-D ICs

Chair: Masahiro Fujita, University of Tokyo
Co-Chair: Anand Iyer, AMD

3:50PM
3C.1
Cost-driven 3D Design Optimization with Metal Layer Reduction Technique
Qiaosha Zou¹, Jing Xie², Yuan Xie³
¹Pennsylvania State University, ²Penn State University, ³Penn State University and AMD research
3C.2  
**TSV-aware Topology Generation for 3D Clock Tree Synthesis**  
Wulong Liu¹, Haixiao Du¹, Yu Wang¹, Yuchuan Ma², Yuan Xie³, Jinguo Quan⁴, Huazhong Yang¹  
¹Dept. of E.E., TNList, Tsinghua University, Beijing, China, ²Dept. of C.S., TNList, Tsinghua University, Beijing, China, ³Dept. of CSE, Pennsylvania State Univ., USA, ⁴Graduate School at Shenzhen, Tsinghua University, China

3C.3  
**Electrical and Thermal Analysis for Design Exchange Formats in Three Dimensional Integrated Circuits**  
Rishik Bazaz¹, Jianyong Xie¹, Madhavan Swaminathan²  
¹Student, Georgia Institute of Technology, ²Professor, Fellow IEEE, Georgia Institute of Technology

3C.4  
**Reliability Consideration with Rectangle- and Double-Signal Through Silicon Vias Insertion in 3D Thermal–Aware Floorplanning**  
Chih-han Hsu, Shanq-Jang Ruan, Ying-Jung Chen, Tsang-Chi Kan  
Department of Electronic Engineering National Taiwan University of Science and Technology, Taipei, Taiwan

3C.5  
**Configurable Redundant Via-Aware Standard Cell Design Considering Multi-Via Mechanism**  
Tsang-Chi Kan, Hung-Ming Hong, Ying-Jung Chen, Shanq-Jang Ruan  
Department of Electronic and Computer Engineering, National Taiwan University of Science and Technology, Taipei, Taiwan

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**Poster Session & Mixer**  
**Tuesday March 5, 2013**

Chair: **Syed M Alam**, Everspin Technologies  
Co-Chair: **Mark Budnik**, Valparaiso University
P.1
A Novel Flow for Reducing Clock Skew Considering NBTI Effect and Process Variations
Jifeng Chen and Mohammad Tehraniipoor
University of Connecticut

P.2
Suspicious Timing Error Prediction with In-Cycle Clock Gating
Youhua Shi, Hiroaki Igarashi, Nozomu Togawa, Masao Yanagisawa
Waseda Univ.

P.3
Performance Entitlement by Exploiting Transistor’s BTI Recovery
Senthil Arasu¹, Mehrdad Nourani¹, Vijay Reddy², John Carulli³
¹Univ. of Texas at Dallas, ²Texas Instruments Inc, Dallas, ³Texas Instruments Inc. Dallas

P.4
Device Design and Analysis of Logic Circuits and SRAMs for Germanium FinFETs on SOI and Bulk Substrates
Vita Pi-Ho Hu, Ming-Long Fan, Pin Su, Ching-Te Chuang
National Chiao Tung University

P.5
A Novel 6T SRAM Cell with Asymmetrically Gate Underlap Engineered FinFETs for Enhanced Read Data Stability and Write Ability
Shairfe Salahuddin, Hailong Jiao, Volkan Kursun
Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology

P.6
Canonical Ordering of Instances to Immunize the FPGA Place and Route Flow from ECO-Induced Variance
Avijit Dutta, Neil Tuttle, Krishnan Anandh
Cypress Semiconductor Corporation
P.7
Architecture for Monitoring SET Propagation in 16-bit Sklansky Adder
Varadan Savulimedu Veeravalli and Andreas Steininger
Vienna University of Technology

P.8
Application of Six-Sigma DMAIC Methodology in the Evaluation of Test Effectiveness: A Case Study for EDA Tools
Eman El Mandouh
Quality Assurance Manager, Mentor Graphics

P.9
A Low Power Deflection Routing Method for Bufferless NoC
Chung-Kai Hsu¹, Kun-Lin Tsai², Jing-Fu Jheng¹, Shanq-Jang Ruan¹, Chung-An Shen¹
¹National Taiwan University of Science and Technology, ²Tunghai University

P.10
A 64-core Platform for Biomedical Signal Processing
Jordan Bisasky¹, Houman Homayoun², Farhang Yazdani³, Tinoosh Mohsenin¹
¹Univ of Maryland - BC, ²George Mason University, ³BroadPak

P.11
Improving Timing Error Tolerance without Impact on Chip Area and Power Consumption
Ken Yano, Takanori Hayashida, Toshinori Sato
Fukuoka University

P.12
System-Level Modelling of Dynamic Reconfigurable Designs using Functional Programming Abstractions
Bahram Najafi Uchevler¹, Kjetil Svarstad¹, Jan Kuper², Christiaan Baaij²
¹Department of Electronics and Telecommunication, NTNU, Norway, ²Department of Computer Science, University of Twente
P.13
Design of a 6 Gbps Continuous-Time Adaptive Equalizer Using a Voltage Rectifier Instead of a Power Detector
Krishna Srinivasan and Jonathan Rosenfeld
Intel Corporation

P.14
A Predictable Compact Model for Non-monotonous Vth-Pelgrom Plot of Long Channel Halo-implanted Transistors
Shigetaka Kumashiro
Renesas Electronics Corporation

P.15
Manufacturable Nanometer Designs using Standard Cells with Regular Layout
Kasyab Parmesh Subramaniyan and Per Larsson-Edefors
Chalmers University of Technology

P.16
Fast Analog Design Optimization using Regression-based Modeling and Genetic Algorithm: A Nano-CMOS VCO Case Study
Dhruva Ghai¹, Saraju Mohanty², Garima Thakral¹
¹Oriental University, Indore, India, ²University of North Texas, USA

P.17
Low Power Sensor for Temperature Compensation in Molecular Biosensing
Daniela De Venuto
Politecnico di Bari, Italy

P.18
A Power Efficient and Digitally Assisted CMOS Complementary Telescopic Amplifier with Wide Input Common Mode Range
Rishi Todani and Ashis Kumar Mal
National Institute of Technology, Durgapur
The small world of sub-20nm is already upon us and has brought a new set of challenges for RTL designers as the race for best PPA (performance, power, and area) continues unabated. Challenges include giga-scale integration of new functionality, new physics effects, new device structures such as FinFETs, interconnect stacks with vastly varying resistance characteristics from bottom to top layers in a non-linear fashion and process variation. These challenges are raising several questions. Can RTL synthesis handle giga-scale, giga-hertz designs in a timeframe of market relevance? Can logic synthesis perform accurate and predictive modeling of the interconnect stack, vias and other physical effects in RTL? How do new device structures affect dynamic and leakage power tradeoff and library choices? How do logic structuring, cell selection, clock gating, and DFT choices change to anticipate and handle routing congestion? And how do we ensure strong correlation between logic synthesis and P&R/signoff? This talk will explore these challenges and provide an overview of state-of-the-art technology to address them in a predictive and convergent design flow.

About Sanjiv Taneja
Sanjiv Taneja is VP of Product Engineering for the Front End Design Group at Cadence Design Systems. Prior to assuming this role in 2010, he led Cadence's Encounter Test R&D group for over five years. He joined Cadence from Bell Laboratories where he led the development of
transistor-sizing based technology for low power design. Sanjiv holds a BS degree in EE from IIT New Delhi, MS in Computer Science from Ohio State University and MBA from NYU.

Keynote Speech 2P.2

Wednesday, March 6
9:30AM-10:00AM

The Lifecycle of Audio Products, Consumer versus Professional

Perry Goldstein
Director of Sales & Marketing
Marshall Electronics

Most electronics will last many years if they are used in their intended manner. Professional electronics are not necessarily built to last longer, but to perform better. When they are built to meet the needs of the professional user, they will be in use for many more years than if a consumer product is used in a professional environment. This keynote provides a review of electronics lifecycle process, and the elements that make up the process, from a sales and marketing perspective. It will compare the design and lifecycle of consumer and professional electronics. The talk will further explore case studies of actual product applications.

About Perry Goldstein

Perry Goldstein is a veteran of the electronics industry. He spent his career in consumer electronics including 23 years at Panasonic. He is currently Director of Sales & Marketing for Marshall Electronics, manufacturer of broadcast monitors, and MXL recording microphones. He is also a professional speaker and writer for the digital signage industry.
SESSION 4A
Wednesday March 6, 2013
Low Power Technologies

Chair: Syed M. Alam, Everspin Technologies
Co-Chair: Dinesh Somasekhar, Intel

10:20AM
4A.1
Peak Power Reduction of a Sensor Network Processor Fabricated With Deeply Depleted Channel Transistors in 65nm Technology
Kentaro Kawakami, Takeshi Shiro, Hironobu Yamasaki, Katsuhiro Yoda, Hiroaki Fujimoto, Kenichi Kawasaki, Yasuhiro Watanabe
Fujitsu Laboratories Ltd.

10:40AM
4A.2
Evaluation of Tunnel FET-based Flip-Flop Designs for Low Power, High Performance Applications
Matthew Cotter, Huichu Liu, Suman Datta, Vijaykrishnan Narayanan
The Pennsylvania State University

11:00AM
4A.3
A Cost-effective 45nm 6T-SRAM Reducing 50mV Vmin and 53% Standby Leakage with multi-Vt Asymmetric Halo MOS and Write Assist Circuitry
Koji Nii¹, Makoto Yabuuchi¹, Hidehiro Fujiwara¹, Yasumasa Tsukamoto¹, Yuichiro Ishii¹, Tetsuya Matsumura¹, Yoshio Matsuda²
¹Renesas Electronics Corporation, ²Kanazawa University

11:20AM
4A.4
CPDI: Cross-Power-Domain Interface Circuit Design in Monolithic 3D Technology
Jing Xie¹, Yang Du², Yuan Xie³
Impact of Process Parameter and Supply Voltage Fluctuations on Multi-Threshold-Voltage Seven-Transistor Static Memory Cells
Hong Zhu and Volkan Kursun
Hong Kong University of Science and Technology

SESSION 4B
Wednesday March 6, 2013
Silicon Diagnosis and Test

Chair: Sreejit Chakravarty, LSI Logic
Co-Chair: Srivatsa Vasudevan, Synopsys

10:20AM
4B.1
Input-Aware Statistical Timing Analysis-Based Delay Test Pattern Generation
Bao Liu and Lu Wang
University of Texas at San Antonio

10:40AM
4B.2
Effect-Cause Intra-Cell Diagnosis at Transistor Level
Zhenzhou Sun\textsuperscript{1}, Alberto Bosio\textsuperscript{2}, Luigi Dilillo\textsuperscript{3}, Patrick Girard\textsuperscript{3}, Aida Todri\textsuperscript{3}, Arnaud Virazel\textsuperscript{2}, Etienne Auvray\textsuperscript{4}
\textsuperscript{1}LIRMM - ST, \textsuperscript{2}LIRMM - UM2, \textsuperscript{3}LIRMM - CNRS, \textsuperscript{4}ST

11:00AM
4B.3
Framework for Analog Test Coverage
Debesh Bhatta\textsuperscript{1}, Ishita Mukhopadhyay\textsuperscript{2}, Suriyaprakash Natarajan\textsuperscript{3}, Prashant Goteti\textsuperscript{3}, Bin
SESSION 4C
Wednesday March 6, 2013
New Ideas in CAD

Chair: James Lei, Altera
Co-Chair: Debasish Das, Synopsys

10:20AM

4C.1
Tabu Search Based Cells Placement in Nanofabric Architectures with Restricted Connectivity
Sadiq M. Sait and Abdalrahman M. Arafeh
King Fahd University of Petroleum & Minerals

10:40AM

4C.2
Relocatable and Resizable SRAM Synthesis for Via Configurable Structured ASIC
Hsin-Hung Liu, Rung-Bin Lin, I-Lun Tseng
Yuan Ze University
11:00AM

4C.3
Cost-Efficient Scheduling in High-Level Synthesis for Soft-Error Vulnerability Mitigation
Yuko Hara-Azumi\textsuperscript{1} and Hiroyuki Tomiyama\textsuperscript{2}
\textsuperscript{1}Nara Institute of Science and Technology, \textsuperscript{2}Ritsumeikan University

11:20AM

4C.4
Analysis of Very Large Resistive Networks Using Low Distortion Embedding
Sandeep Koranne
Mentor Graphics Corporation

11:40AM

4C.5
Efficient Translation Validation of High-Level Synthesis
Tun Li, Yang Guo, Wanwei Liu, Chiyuan Ma
NUDT

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SESSION 5A
Wednesday March 6, 2013
System Design Methodologies and Automation

Chair: Makram Mansour, Texas Instruments
Co-Chair: Sudeep Pasricha, Colorado State University

1:30PM

5A.1
Performance and Cache Access Time of SRAM-eDRAM Hybrid Caches Considering Wire Delay
Young-Ho Gong, Hyung Beom Jang, Sung Woo Chung
Department of Computer and Radio Communication Engineering, Korea University
1:50PM

5A.2

Increasing the Security Level of Analog IPs by Using a Dedicated Vulnerability Analysis Methodology
Noemie Beringuier-Boher¹, David Hely², Vincent Beroulle², Joel Damiens³, Philippe Candelier³
¹Grenoble-INP LCIS and STMicroelectronics, ²Grenoble-INP LCIS, ³STMicroelectronics

2:10PM

5A.3

High-speed DFG-level SEU Vulnerability Analysis for Applying Selective TMR to Resource-Constrained CGRA
Takashi Imagawa, Hiroshi Tsutsui, Hiroyuki Ochi, Takashi Sato
Kyoto University

2:30PM

5A.4

Geostatistics Inspired Fast Layout Optimization of Nanoscale CMOS Phase Locked Loop
Oghenekarho Okobiah, Saraju Mohanty, Elias Kougianos
University of North Texas, Denton

2:50PM

5A.5

A Method to Determine the Sensitization Probability of a Non-Robustly Testable Path
Dheepakkumaran Jayaraman and Spyros Tragoudas
Southern Illinois University Carbondale

3:10PM

5A.6

Early System Level Modeling of Real-time Applications on Embedded Platforms
Richard Lee¹, Karim Abdel-Khalek¹, Frederic Risacher², Samar Abdi¹
¹Concordia University, ²Research In Motion
SESSION 5B

Wednesday March 6, 2013

Manufacturing and Modeling Issues of Nanoscale CMOS

Chair: Mustafa Yelten, Intel
Co-Chair: Rajan Beera, Texas Instruments

1:30PM

5B.1

SUALD: Spacing Uniformity-Aware Layout Decomposition in Triple Patterning Lithography
Zihao Chen¹, Hailong Yao², Yici Cai²
¹Tsinghua University, China, and Department of Microelectronics, Peking University, Beijing 100871, China, ²Tsinghua University, China

1:50PM

5B.2

Stochastic Behavioral Modeling of Analog/Mixed-Signal Circuits by Maximizing Entropy
Rahul Krishnan¹, Wei Wu¹, Fang Gong¹, Lei He²
¹Student Member, IEEE, ²Senior Member, IEEE

2:10PM

5B.3

Analysis, Modeling and Silicon Correlation of Low-voltage Flop Data Retention in 28nm Process Technology
Animesh Datta, Mohamed Abu-Rahma, Sachin Dasnurkar, Hadi Rasouli, Sean Tamjidi, Ming Cai, Samit Sengupta, PR Chidambaram, Raghavan Thirumala, Nikhil Kulkarni, Prasanna Seeram, Prasad Bhadri, Prayag Patel, Sei Seung Yoon, Esin Terzioglu
Qualcomm

2:30PM

5B.4

A Comparator Energy Model Considering Shallow Trench Isolation Stress by Geometric Programming
Gong Chen¹, Yu Zhang¹, Bo Yang², Qing Dong¹, Shigetoshi Nakatake¹
¹The University of Kitakyushu, ²Design Algorithm Laboratory, Inc.

2:50PM

5B.5

Wire Delay Variability in Nanoscale Technology and Its Impact on Physical Design
Sani Nassif, Gi-Joon Nam, Shayak Banerjee
IBM Research

3:10PM

5B.6

Multi-trap RTN Parameter Extraction based on Bayesian Inference
Hiromitsu Awano, Hiroshi Tsutsui, Hiroyuki Ochi, Takashi Sato
Kyoto University

SESSION 5C
Wednesday March 6, 2013

Multi-core and Multi-processor Systems

Chair: Bin Wu, AMD
Co-Chair: Amir Ajami, Synopsys

1:30PM

5C.1

VERVE: A Framework for Variation-Aware Energy Efficient Synthesis of NoC-based MPSoCs with Voltage islands
Nishit Kapadia and Sudeep Pasricha
Colorado State University

1:50PM

5C.2

A Virtualization Approach for MIPS-based MPSoCs
Alexandra Aguiar, Carlos Moratelli, Marcos Sartori, Fabiano Hessel
PUCRS
2:10PM  
5C.3  
Thermal-Aware Semi-Dynamic Power Management for Multicore Systems with Energy Harvesting  
Yi Xiang and Sudeep Pasricha  
Colorado State University  

2:30PM  
5C.4  
On the Interactions Between Real-Time Scheduling and Inter-thread Cache Interferences for Multicore Processors  
Yiqiang Ding and Wei Zhang  
Virginia Commonwealth University  

2:50PM  
5C.5  
Resource Allocation and Consolidation in a Multi-Core Server Cluster Using a Markov Decision Process Model  
Yanzhi Wang, Shuang Chen, Hadi Goudarzi, Massoud Pedram  
University of Southern California  

3:10PM  
5C.6  
Reliability-Aware and Energy-Efficient Synthesis of NoC based MPSoCs  
Yong Zou and Sudeep Pasricha  
Mr.

SESSION 6A  
Wednesday March 6, 2013  
Issues and Challenges in Characterization and Power Integrity for Nanometer Technologies  
Chair: Srini Krishnamoorthy, AMD  
Co-Chair: Vamsi Srikantam, Applied Micro
3:50PM

6A.1

CMOS Inverter Delay Model Based on DC Transfer Curve for Slow Input

Felipe Marranghello, André Reis, Renato Ribas

UFRGS

4:10PM

6A.2

RF Passive Device Modeling and Characterization in 65nm CMOS Technology

Errikos Lourandakis, Stefanos Stefanou, Konstantinos Nikellis, Sotiris Bantas

Helic Inc.

4:30PM

6A.3

An Efficient Method for ECSM Characterization of CMOS Inverter in Nanometer Range Technologies

Baljit Kaur\textsuperscript{1}, Sandeep Miryala\textsuperscript{2}, Sanjeev Kumar Manhas\textsuperscript{1}, Anand Bulusu\textsuperscript{1}

\textsuperscript{1}Indian Institute of Technology, Roorkee, India, \textsuperscript{2}politecnico di torino, torino

4:50PM

6A.4

Power Integrity Analysis and Discrete Optimization of Decoupling Capacitors on High Speed Power Planes by Particle Swarm Optimization

Jai Narayan Tripathi\textsuperscript{1}, Raj Kumar Nagpal\textsuperscript{2}, Nitin Kumar Chhabra\textsuperscript{2}, Rakesh Malik\textsuperscript{2}, Jayanta Mukherjee\textsuperscript{1}, Prakash R. Apte\textsuperscript{1}

\textsuperscript{1}IIT Bombay, \textsuperscript{2}STMicroelectronics Pvt. Ltd.

5:10PM

6A.5

A Method to Determine the Sensitization Probability of a Non-Robustly Testable Path

Dheepakkumaran Jayaraman\textsuperscript{1} and Spyros Tragoudas\textsuperscript{2}

\textsuperscript{1}Nvidia Corporation, \textsuperscript{2}Southern Illinois University, Carbondale
SESSION 6B
Wednesday March 6, 2013
Low Power Circuits

Chair: Dinesh Somasekhar, Intel
Co-Chair: Amin Khajeh Djahromi, Intel

3:50PM
6B.1
A Power-Efficient On-Chip Linear Regulator Assisted by Switched Capacitors for Fast Transient Regulation
Suming Lai and Peng Li
Texas A&M University

4:10PM
6B.2
A Versatile Rail to Rail Current Mode Instrumentation Amplifier with an Embedded Band-pass Filter for Bio-potential Signal Conditioning
Anvesha Amaravati and Maryam Shojaei Baghini
IIT-Bombay

4:30PM
6B.3
A 0.2nJ/sample 0.01mm2 Ring Oscillator Based Temperature Sensor for On-Chip Thermal Management
Nicolo Testi and Yang Xu
ECE Department, Illinois Institute of Technology

4:50PM
6B.4
Analysis and Comparison of XOR Cell Structures for Low Voltage Circuit Design
Shinichi Nishizawa, Tohru Ishihara, Hidetoshi Onodera
Kyoto University
5:10PM

6B.5

A CMOS High Dimming Ratio Power-LED Driver with a Preloading Inductor Current Method

Kwang Yoon and Keon Lee

Inha University

SESSION 6C

Wednesday March 6, 2013

Reliable System Design

Chair: Mustafa Yelten, Intel

Co-Chair: Srivinas Bodapati, Intel

3:50PM

6C.1

Protection of Muller-Pipelines from Transient Faults

Syed Rameez Naqvi, Jakob Lechner, Andreas Steininger

Embedded Computing Systems, Vienna University of Technology, Vienna, Austria

4:10PM

6C.2

Minimizing Simultaneous Switching Noise at Reduced Power with Constant-Voltage Power Transmission Lines for High-Speed Signaling

Satyanarayana Telikepalli, Madhavan Swaminathan, David Keezer

Dept. of Electrical & Computer Engineering, Georgia Institute of Technology

4:30PM

6C.3

Reliable Express-Virtual-Channel-based Network-on-Chip under the Impact of Technology Scaling

Xin Fu¹, Tao Li², Jose Fortes²

¹University of Kansas, ²University of Florida
6C.4
Clustering Techniques and Statistical Fault Injection for Selective Mitigation of SEUs in Flip-Flops
Adrian Evans¹, Michael Nicolaidis², Shi-Jie Wen³, Thiago Assis⁴
¹iRoC Technologies, ²Institut National Polytechnique de Grenoble, ³Cisco Systems, ⁴Vanderbilt University

5:10PM
6C.5
Easy-to-Build Arbiter Physical Unclonable Function with Enhanced Challenge/Response Set
Dinesh Ganta and Leyla Nazhandali
Virginia Tech