Reliability Challenges in Sub 20nm Technologies

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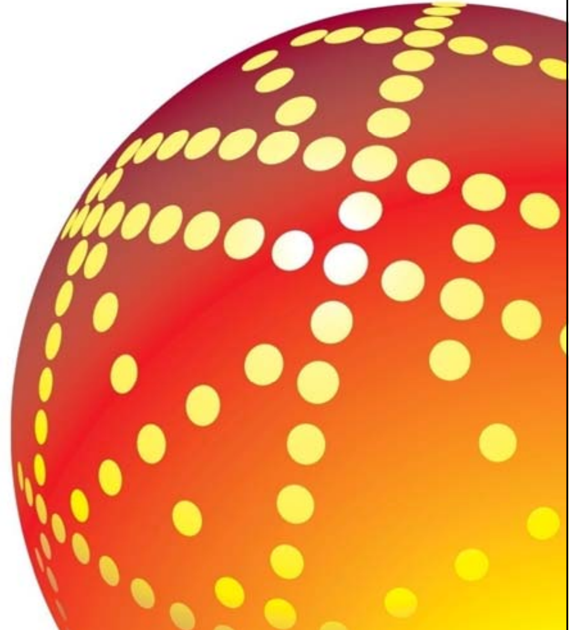
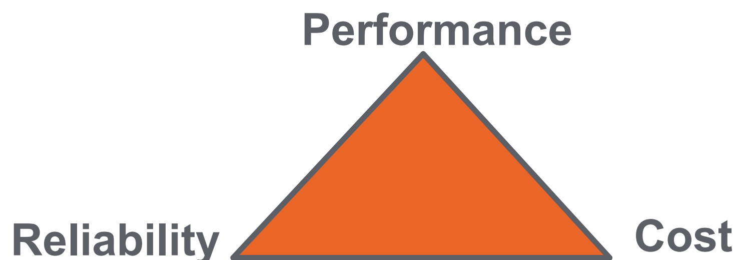
GLOBALFOUNDRIES



Motivation

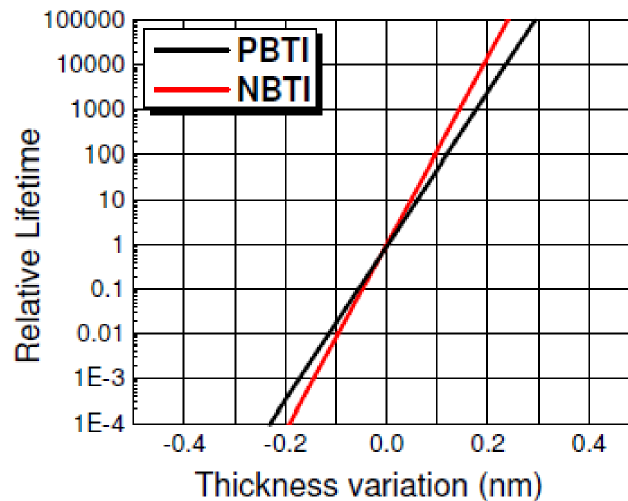
- **Why do we worry about CMOS reliability?**



- CMOS technologies are designed to maximize performance at reduced cost increasing pressure on reliability
- The challenge is finding the optimum trade off to be competitive in the market place
  - If you are too conservative you leave money on the table !!!
  - If you are too aggressive you may risk your business !!!

Tinv Scaling Challenge

E. Cartier et al., p.194, IEDM 2011

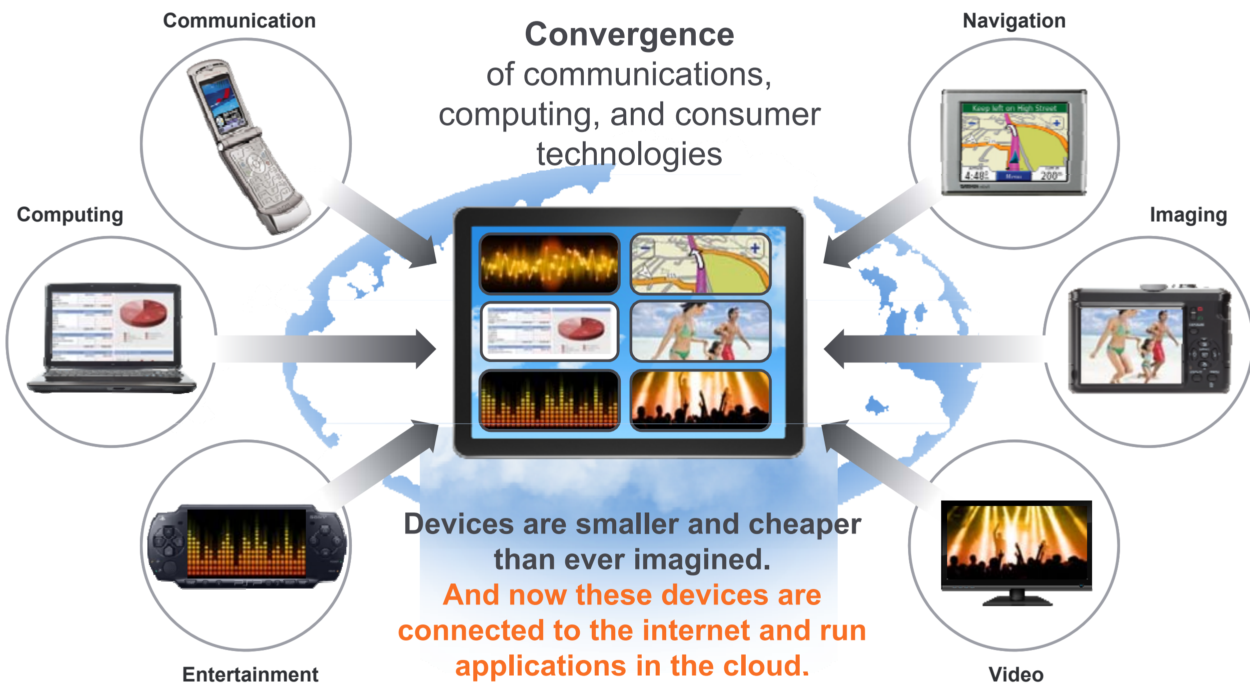


- Tinv Scaling severely limited due to BTI for sub 20 nm nodes.
- **Reliability aware design can alleviate the challenge**

Outline

- Introduction
  - Industry overview
  - Role of Reliability Engineer in Technology Development
  - What is scaling and what is not scaling…
- Basics of FEoL Reliability Mechanisms
  - BTI
  - HCI
  - TDDB
- Moving beyond 20nm
  - Product level degradation
  - New Channel materials

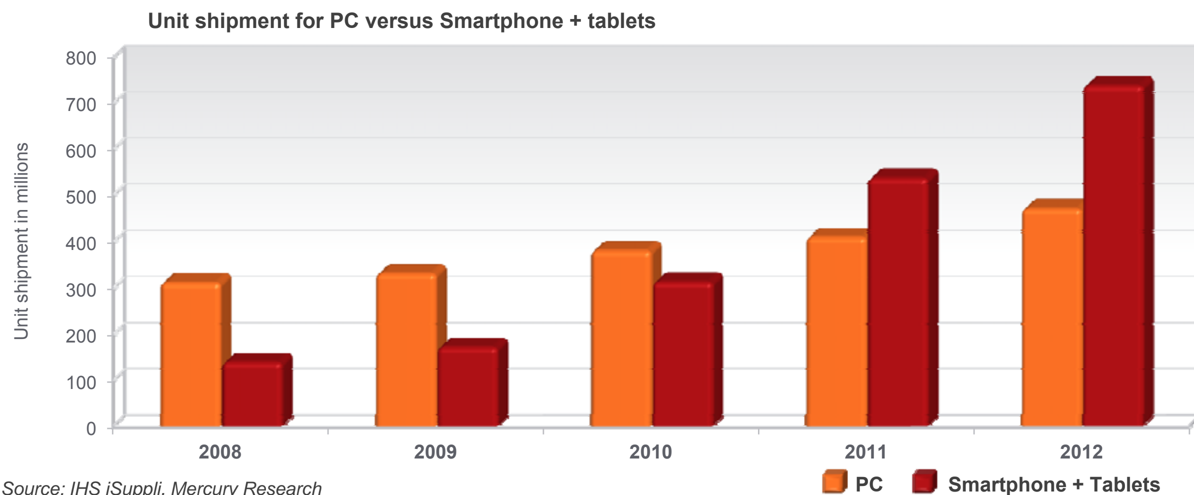
The Convergence is Here



Convergence Powered by Semiconductors

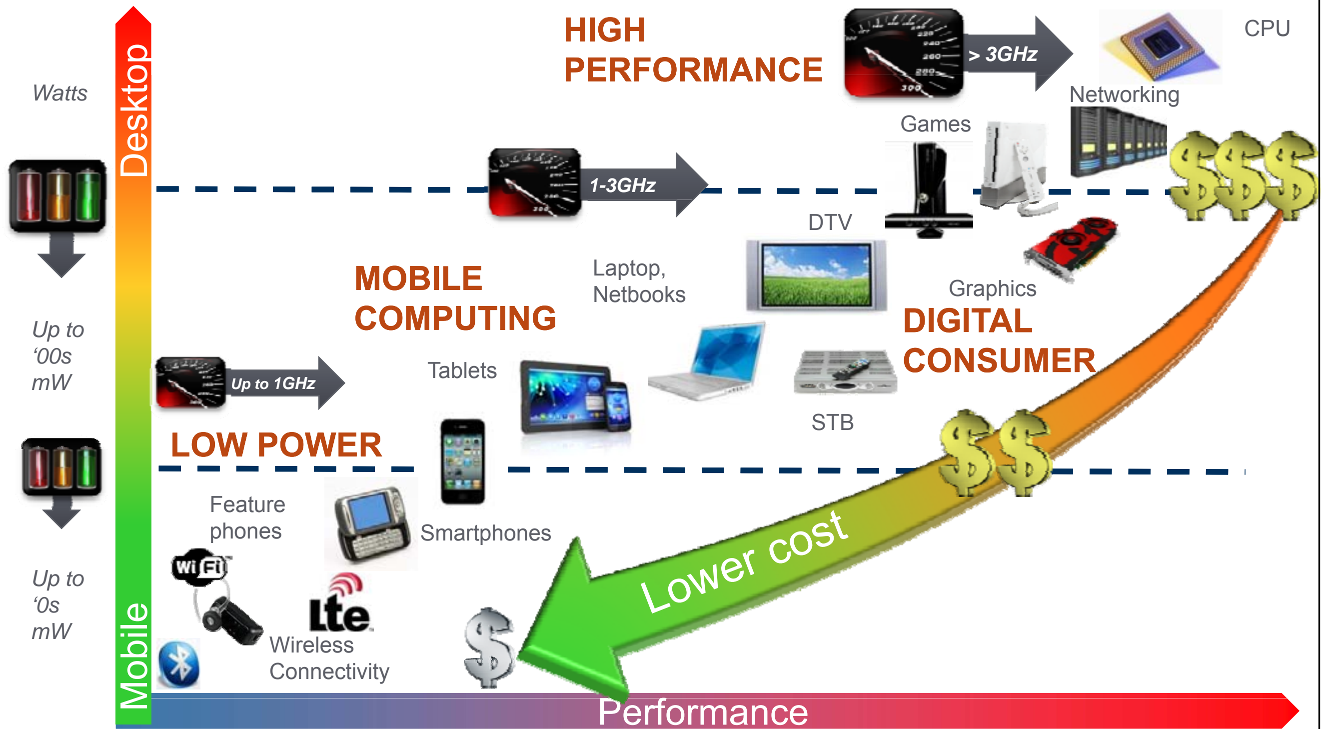
- Wireless segment overtakes PCs in 2011
  - Becoming world's leading market for semiconductor purchasing by OEMs
  - Sign of a fundamental shift from PCs to mobile devices
  - Driven by booming sales of smartphones and tablets

Unit shipment for PC versus Smartphone + tablets



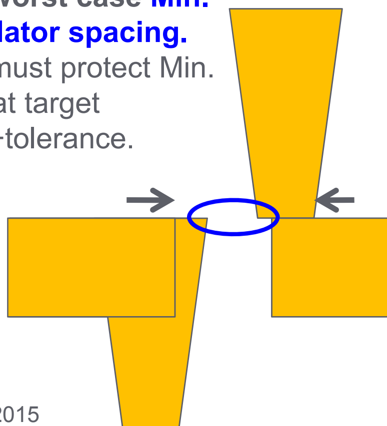
Source: IHS iSuppli, Mercury Research

Application specific 'tuned' Solutions



Role of Reliability Engineers in Technology Development

- **Define Technology Vmax and Tinv**
- **Overlay and Variation of via CDs → worst case Min. Insulator spacing.**
- GR must protect Min. Ins. at target Vdd+tolerance.



- **Provide Feedback to the development line on scaling trends.**
- **Validate the tends as derived from previous technology nodes.**
- **Develop new methodologies which would help technology enablement.**
- **Qualification**

- **Enable reliability support for over biasing the technology**
- **Support custom circuits and design**

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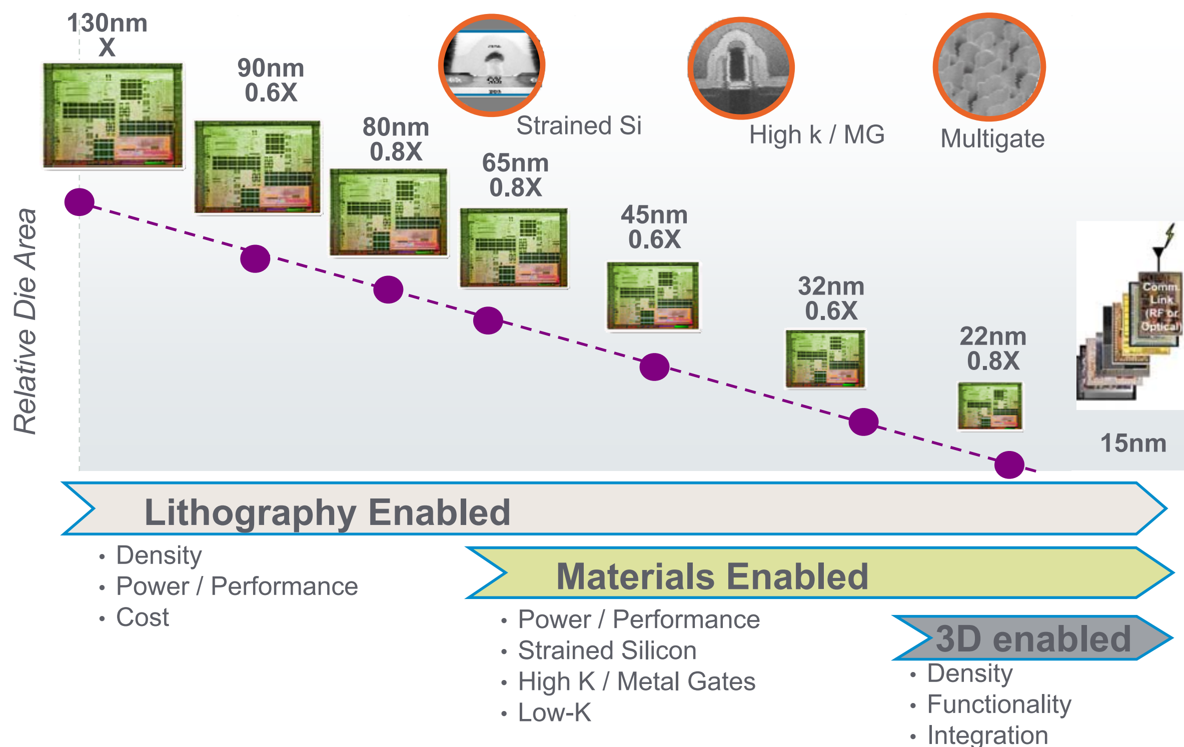
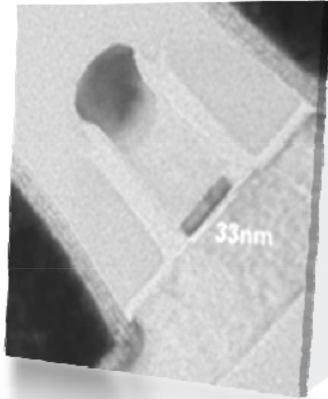
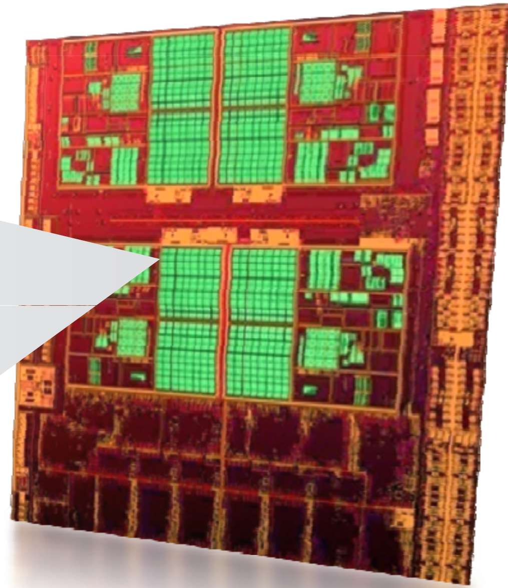
Three Key Technology Enablers



HKMG in Production





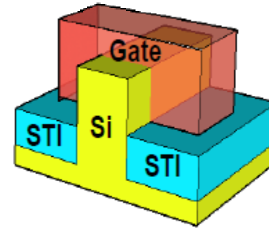
Lessons learned

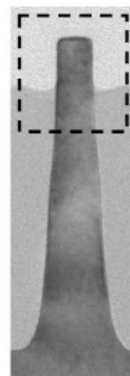
Materials integration as important as materials choice

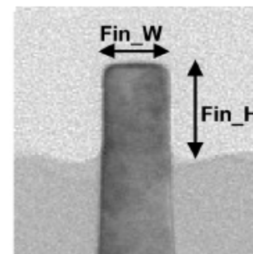
HKMG is hard – but we have tamed the beast!

3D Devices (FINFET/TRIGATE)

- Need for low Vt and better subthreshold slope drives 3D Device approach.
- MOSFET becomes a resistor for short Channel lengths and Drain competes with Gate to control the channel barrier.
- Gate can not control the leakage current paths that are far from gate irrespective of oxide scaling.

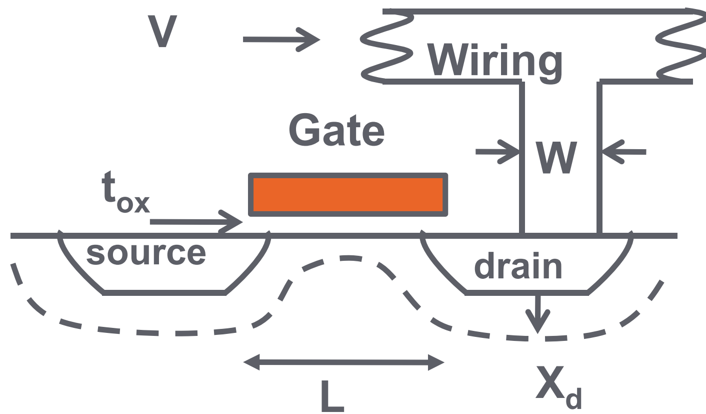






Weff = 2 x Fin_H + Fin_W

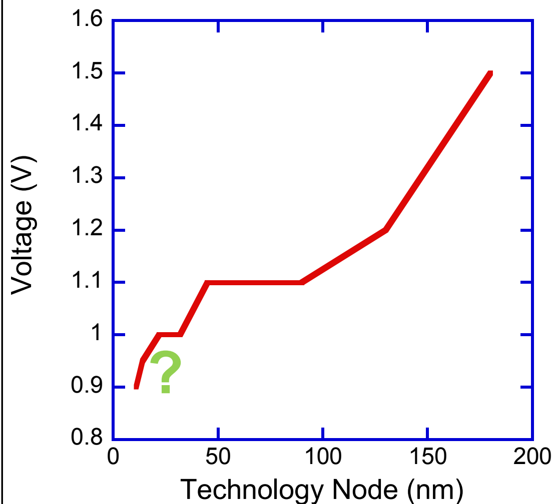
Device Scaling Basics

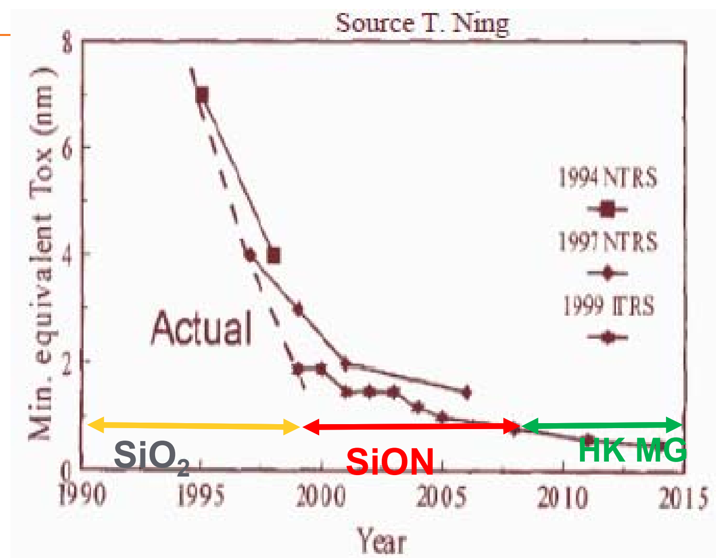


Scaling	
Voltage	V/α
Gate Length	L/α
Wire Width	W/α
t_{ox}	t_{ox}/α
Diffusion	X_d/α
Doping	N_a*α

- **Scaling results in**
  - Higher Density
  - Higher Speed
  - Lower Power
  - ….

Vdd and Thickness Scaling

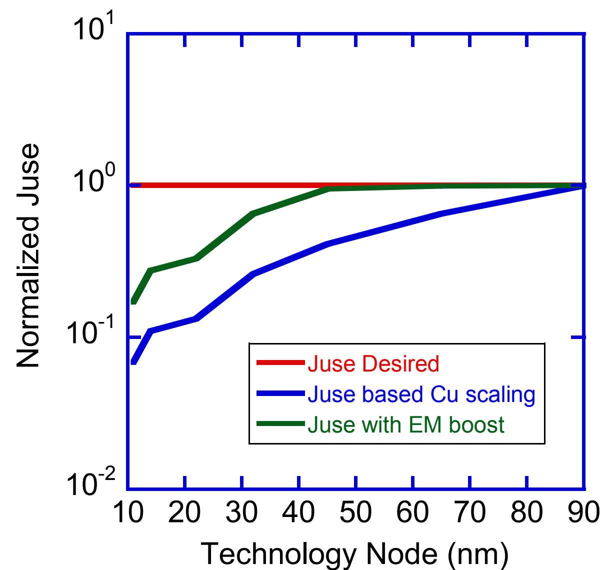




- Vdd and Tox scaling virtually stopped after 90nm technology.
- Below this node the power dissipation and reliability halted further scaling and need for HK- MG became necessary.
- Further material changes seem unlikely and we may again face no further Tox scaling driven by reliability unless Vdd scales with FINFETs.

Juse targets and implications for EM

- Juse targets likely to remain similar to previous node.
- Cu Cross-section could scale as much as 50% for tight pitch lower levels.
- This gap must be bridged by Material engineering and more precise accounting of EM performance;
  - Cu-Alloy seed. (Resistivity hit, industry standard, 20 nm option)
  - Metal Cap. (Manufacturability and TDDB, …)
  - Short line EM boosts.
  - Vertical current flow rules.
  - Redundant via array boosts.



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  - BTI (Bias Temperature Instability)
  - HCI (Hot Carrier Injection)
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  - Product level degradation
  - New Channel materials

What is reliability?

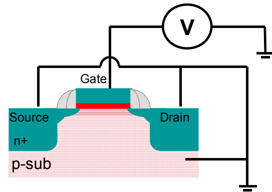
- “Reliability is defined as the probability that a given item will perform its intended function for a given period of time under a given set of conditions”
  - The probability is the likelihood that some given event will occur and as a measure a value between 0 and 1 is assigned
  - The intended function of the item and its use condition are specifications which need to be stated
  - The period of time is often referred as lifetime and depends on the items application

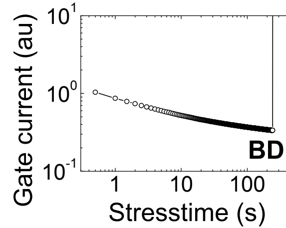
Definition of failure and the various mechanism

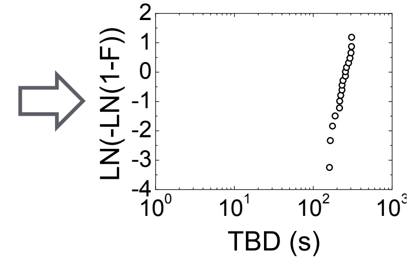
- “Failure is when the given item lost its ability to perform the intended function within previously specified limits”
- FEOL related failure mechanism in CMOS devices:
  - Time Dependent Dielectric Breakdown (TDDB), Bias Temperature Instability (BTI), Hot Carrier Injection (HCI)
  - Mobile Ion Contamination, Plasma-processing Induced Damage (PPID), Random Telegraph Noise (RTN), Electrostatic Discharge (ESD), Latch-up, Soft Error Rate (SER), …
- FEOL related failure modes:
  - Gate current increase, Threshold voltage shift, Drain current degradation, …

Typical failure modes for reliability modeling

- Gate current increase caused by dielectric breakdown
  ➔ sudden failure

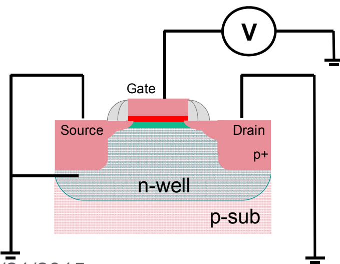


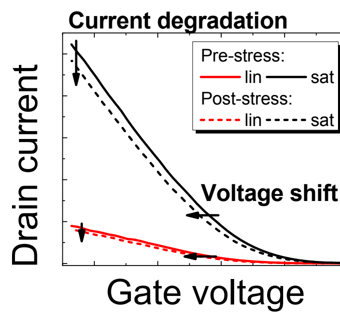


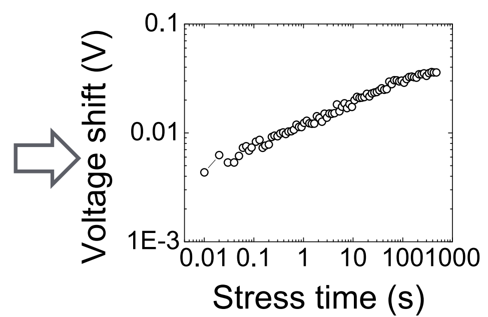


- Threshold voltage shift or drain current degradation caused by e.g. BTI or HCI ➔ gradual failure

e.g. NBTI





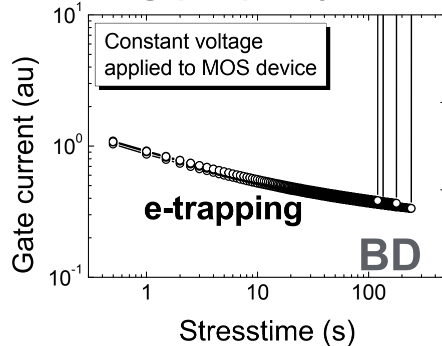


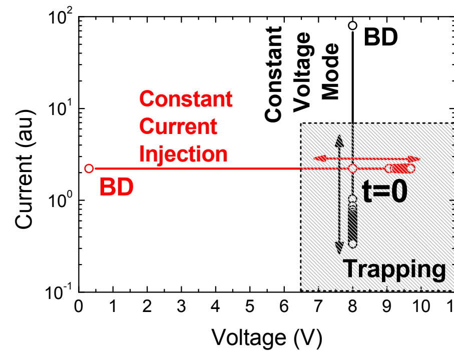
Time Dependent Dielectric Breakdown

- What is TDDB?
- TDDB measurement methods
- Challenges of detecting breakdown
- BD in HK MG

What is dielectric breakdown?

- “Dielectric breakdown occurred when the dielectric has lost its insulating property”



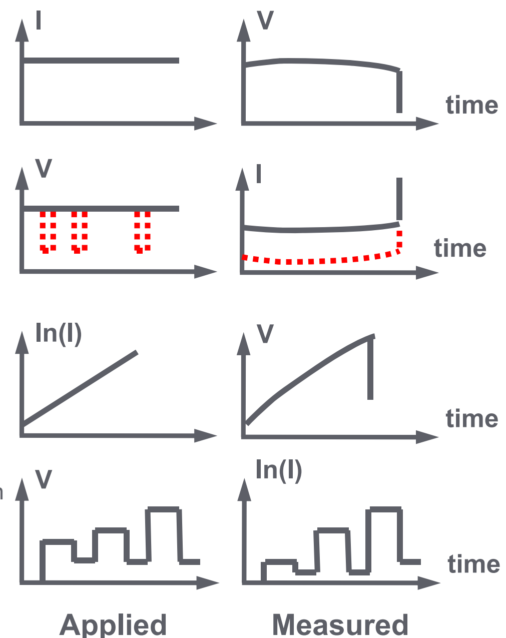


- Loosing insulting property in thick oxide means:
  - High current when a voltage source is connected
  - Small build up of voltage when a current source is connected

Methods to study TDDB

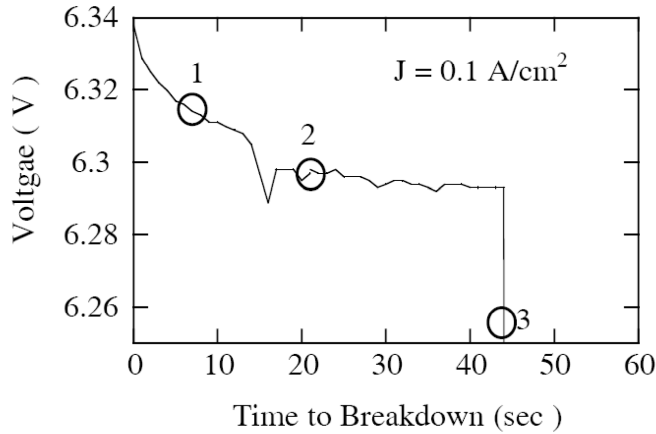
A.Kerber/McMahon, IRPS 2012 tutorial.

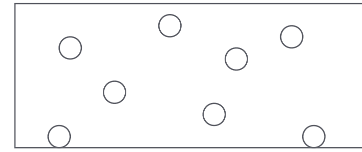
- Constant Current Stress (CCS)
  - Inject current and measure Voltage as function of time.
  - Used for thicker oxides (>~5nm) for F-N stress where Q_{BD}/T_{BD} dependend on J and independent of thickness.
- Constant Voltage Stress (CVS)
  - Apply voltage and measure current as function of time, possibly interrupt stress to measure current at reference condition.
  - Used for thinner dielectrics stressed in DT regime where TBD/QBD depends on gate voltage and thickness.
- Exponential Current Ramp Stress (ECRS)
  - Increase injection current on an exponential scale and measure voltage at each current level.
- Voltage Ramp stress (VRS)
  - Increase stress voltage on a linear scale and measure current at each voltage, include intermittent current measurement at reference condition.
  - Gaining in popularity for quick turn feedback on process learning.

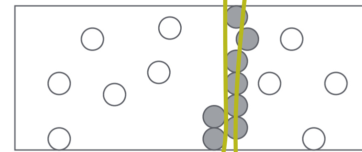


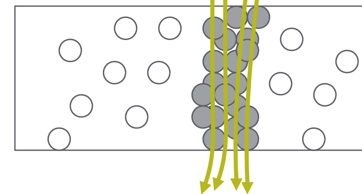
- For leading-edge technologies two methods, CVS and VRS are preferred for TDDB modeling.

Degradation Modes



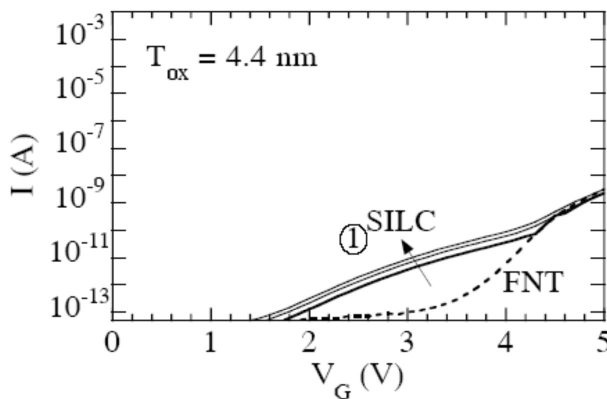


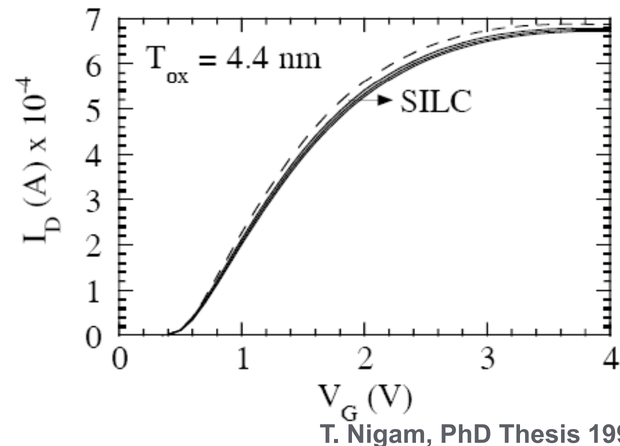




1. Trap generation : Vt shifts and SILC
2. Formation of local conducting path via the neutral electron traps leading to Soft Breakdown (SBD)
3. Thermal run away leading to Hard Breakdown (HBD)

Degradation Mode-SILC

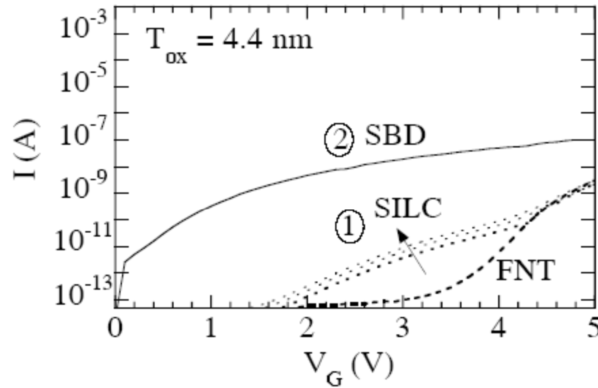


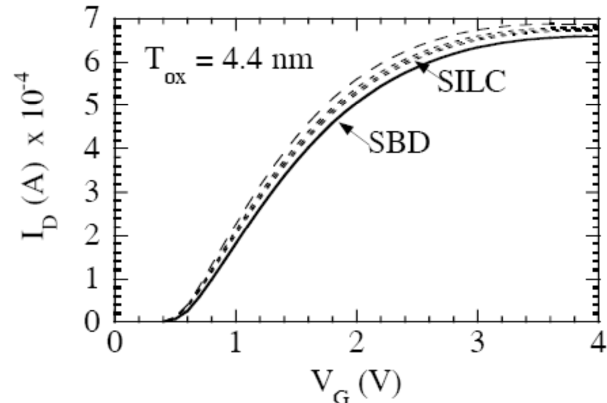


T. Nigam, PhD Thesis 1999

- Signature : Gradual Increase in gate leakage at low voltage/fields
  - Conduction Mechanism: Trap assisted tunneling via neutral electron traps generated in the bulk of the oxide.
  - Current voltage relationship: Exponential with a reduced barrier
  - Impact on Transistor : Gradual shift in Vt, gm etc..
- Is a reliability challenge for Non-Volatile Memory devices

Degradation Mode-SBD

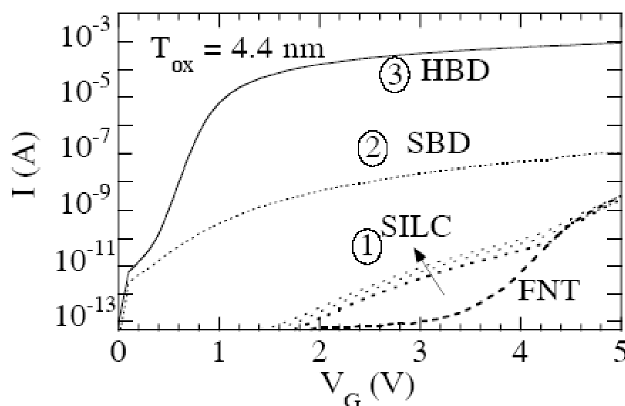


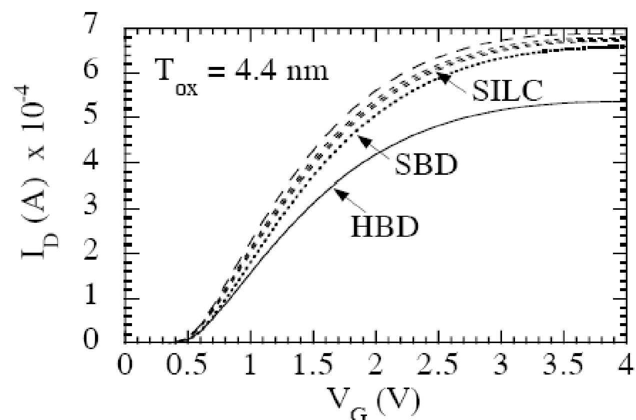


T. Nigam, PhD Thesis 1999

- Signature : Sudden Increase in gate leakage at low voltage/fields
  - Conduction Mechanism: Quantum co-tunneling arising from Coulomb Blockade or Quantum point contact
  - Current voltage relationship: Power law ($I=V^{\delta}$)
  - Impact on Transistor : Further shift in Vt, gm etc., but **transistor still functional**
- May or may not be a reliability challenge for CMOS

Degradation Mode-HBD



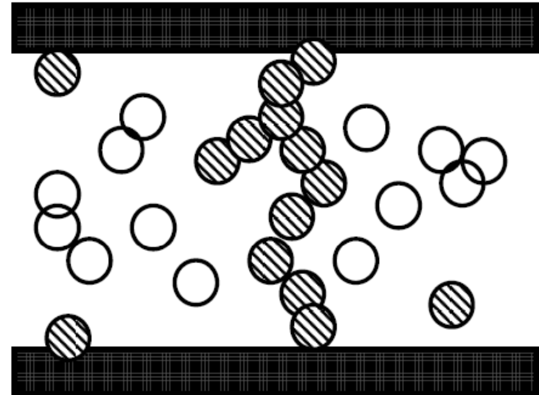


T. Nigam, PhD Thesis 1999

- Signature : Sudden Increase in gate leakage
  - Conduction Mechanism : Simple resistor
  - Current voltage relationship: Linear dependence (I=a.V)
  - Impact on Transistor : **Transistor no longer functional**
- Is a reliability challenge for CMOS

Percolation Theory

- Oxide BD occurs when a conducting path is formed
- Defect density reaches a critical value $\mathbf{N_{BD}}$
- $\mathbf{N_{BD}}$: an intrinsic statistical property of the oxide
- $\mathbf{N_{BD}}$ decreases as T_{OX} decreases
- Predicts reduction in Weibull slope with T_{OX}

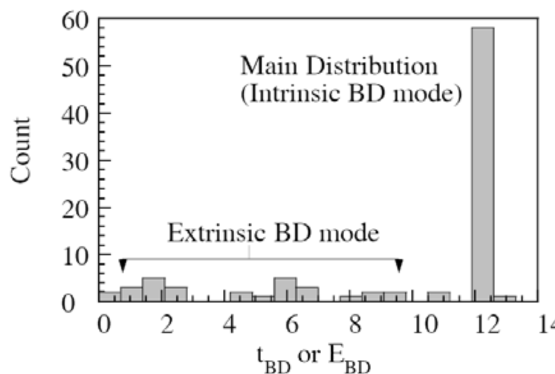


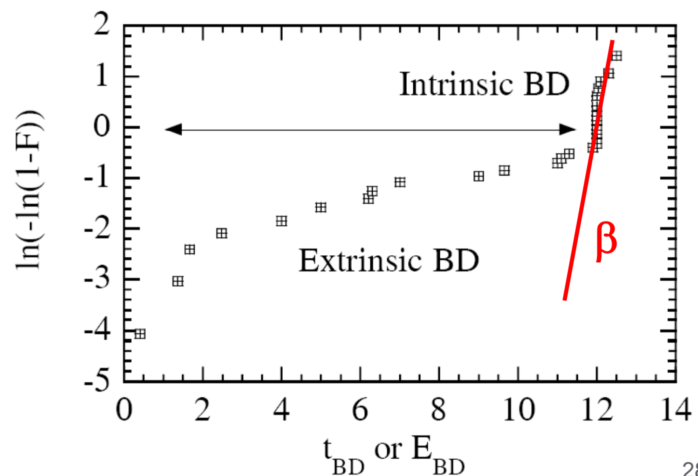
Degraeve et al., IEDM, 863, 1995

Time Dependent Dielectric Breakdown

- 2 modes for breakdown distribution
  - Intrinsic and Extrinsic
- Weibull distribution given by

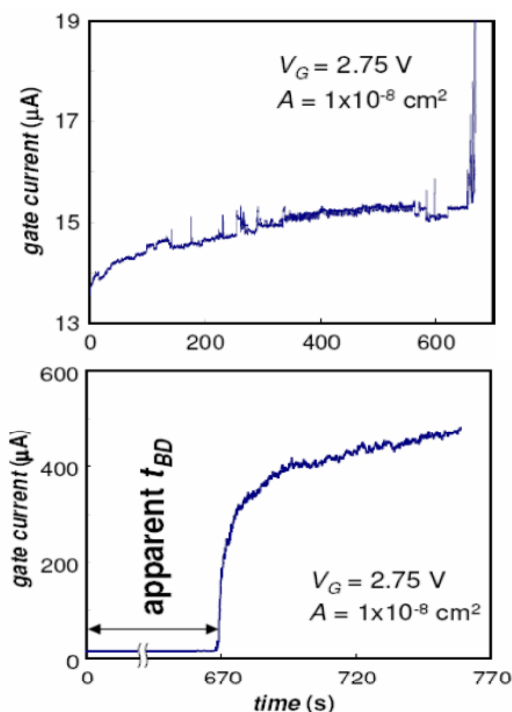
$$\mathbf{F(t)=1\text{-}exp\{-(t/t_{63})^{\beta}\}}$$
$$\mathbf{W(t)=Ln(-Ln(1\text{-}F))=\beta Ln(t/t_{63})}$$

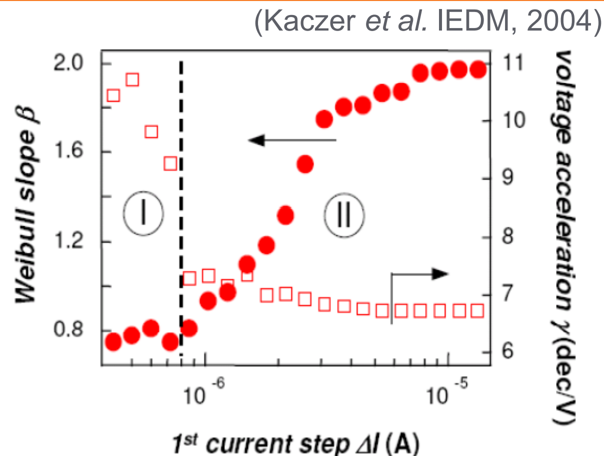




Ultra-thin Oxide Breakdown

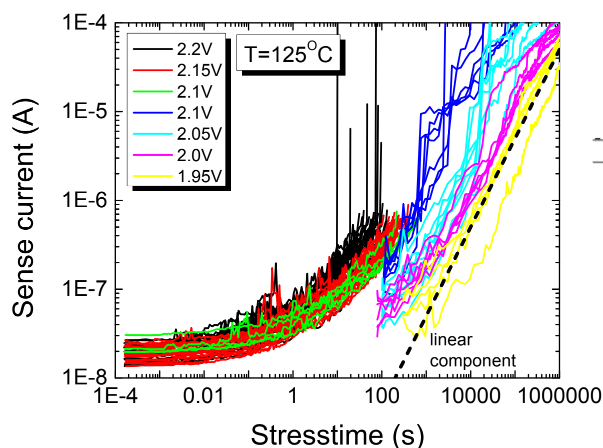
(Kaczer *et al.* IEDM, 2004)

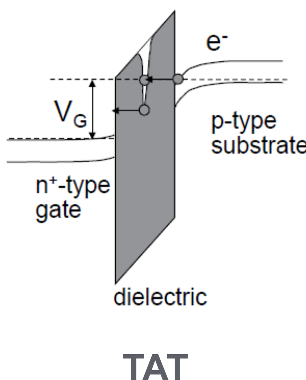


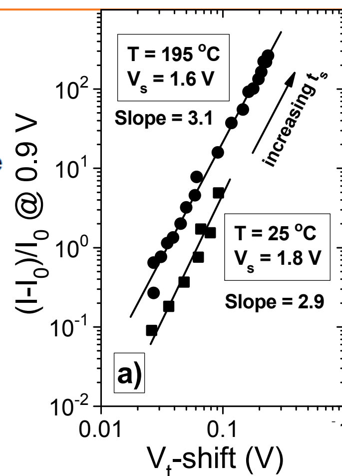


- Larger β and smaller voltage acceleration measured if 1st SBD not detected properly

SILC in HK : Stress Induced Leakage Current







E. Cartier, IRPS 2009

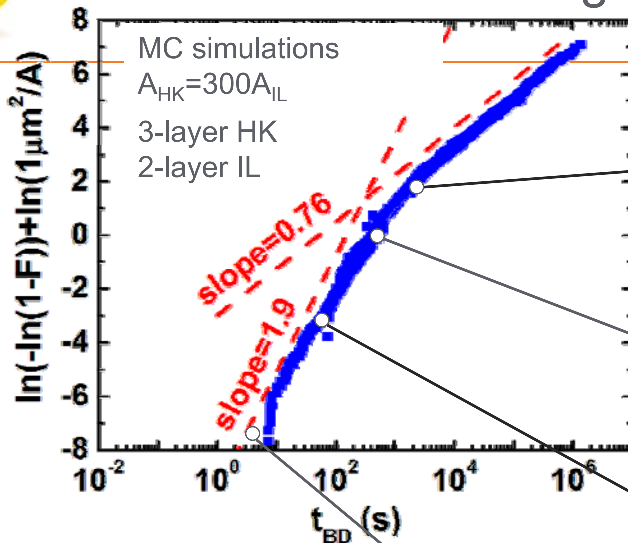
- SILC has emerged as a new concern for HKMG (esp. nFET).
- SILC is commonly attributed to Trap-assisted Tunneling (TAT).
- SILC is sensitive to IL thickness and to gate stack processing
  - Less SILC formation for thicker IL.
  - At long stress times “linear SILC” seen, independent of IL thickness.

Basic TDDB Observations for HK

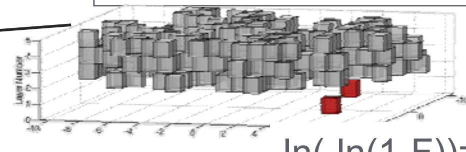
- Significant SILC is measured on NFET during stress
  →Large number of defects are generated in HK.
- In the literature, data is mostly collected on small areas
  →The obtained Weibull slope is limited by the interfacial oxide
- Weibull slope increases with area for NMOS and PMOS
  →See Kerber, IRSP 2009
- PFET Weibull slope is less than that of NFET
  →See Kerber IRPS 2009
- Vertical area scaling works all the way to 1000μm^2

Any theory proposed must explain all the above observations

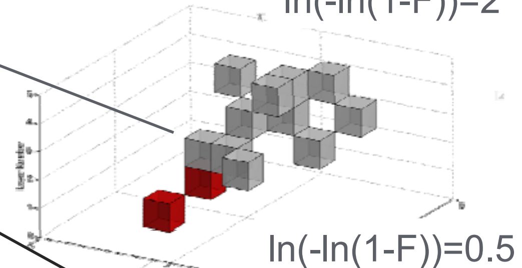
Nature of BD Path Changes



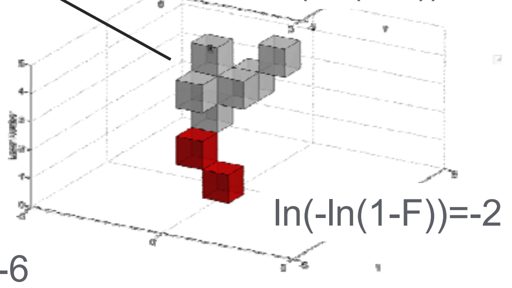
Long BD: probability determined only by IL. β=0.38x2=0.76



ln(-ln(1-F))=2

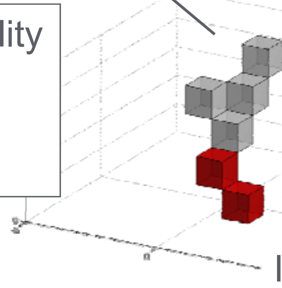


ln(-ln(1-F))=0.5



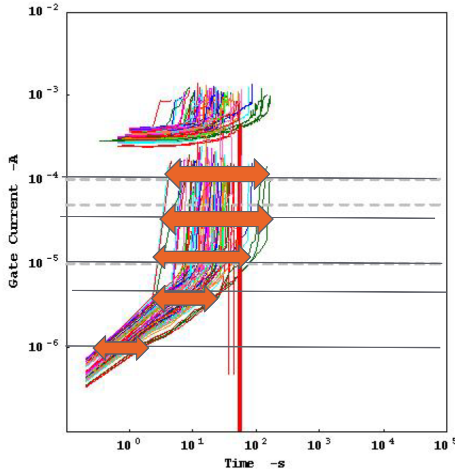
ln(-ln(1-F))=-2

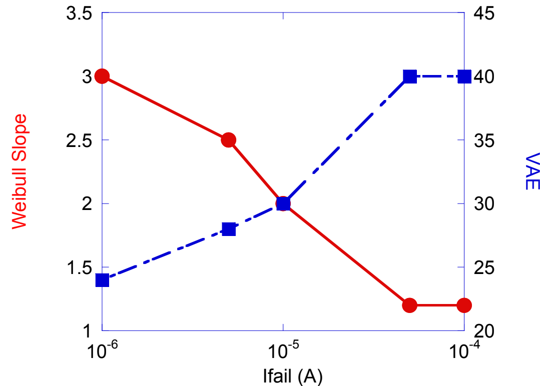
Short BD: probability determined by complete stack. β=0.38x5~1.9



ln(ln(1-F))=-6

HK MG NFET Breakdown Challenge

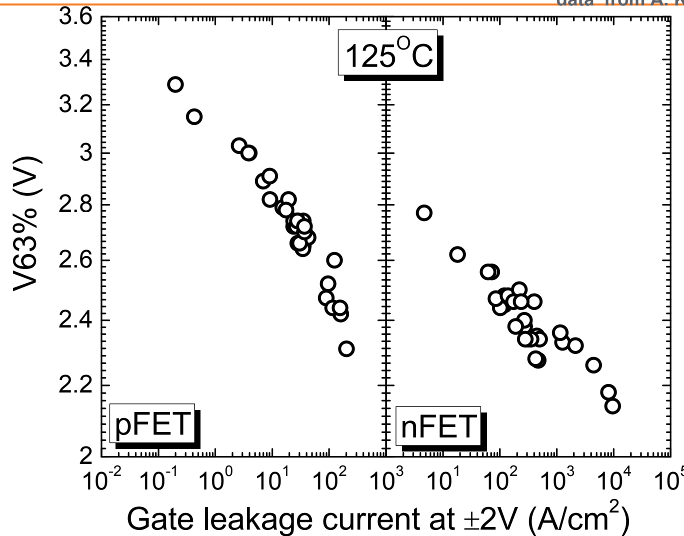




- For small Ifail larger β and smaller voltage acceleration in SILC regime.
- For large Ifail we get lower β if device suffer HBD and may see an uptake in Weibull if progressive breakdown is observed.
- VAE will increase with Ifail.
- For intermediate Ifail Weibull slope will decrease and VAE will increase.

Figure of merit for dielectric breakdown

data from A. Kerber et al., IRPS, pg. 505, 2009.



- Strong correlation between gate leakage and breakdown voltage
- V63 versus Jg a good choice for BD figure of merit

TDDB Take away

- TDDB is studied using CVS.
- Breakdown in oxides can be either soft leading to local percolation or Hard breakdown.
- Detecting dielectric breakdown is becoming challenging as oxide is scaled.
- Presence of SILC in HK MG for NFET devices makes BD detection a challenge.
- Introduction of HK MG induced a new mode in breakdown distribution.
- Continued scaling of dielectric leads to a reduction in lifetime TDDB.

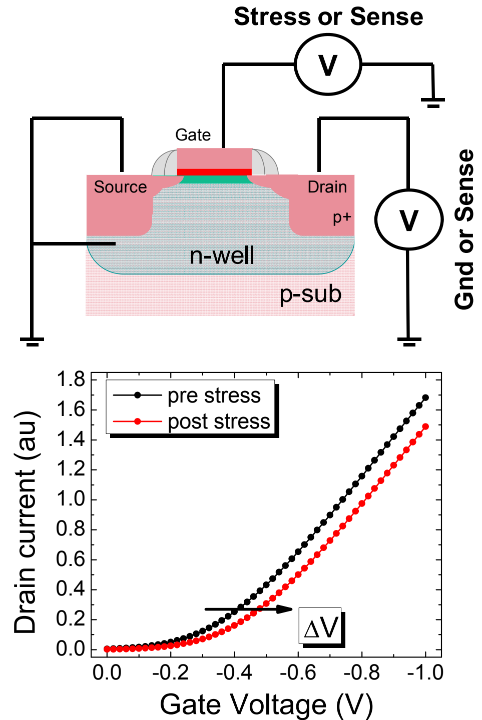
Bias Temperature Instability

- What is BTI?
- BTI measurement methods
- Recovery in BTI
- BTI in HK MG

BTI

A.Kerber/McMahon, IRPS 2012 tutorial.

- When the MOSFET device is biased in inversion mode the device characteristics shift / degrade
  (stress condition: Vg high, Vd low)

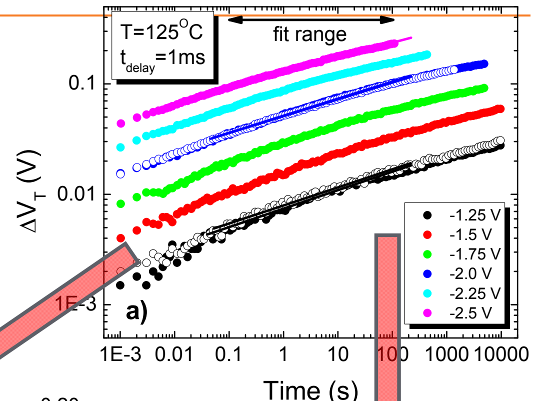


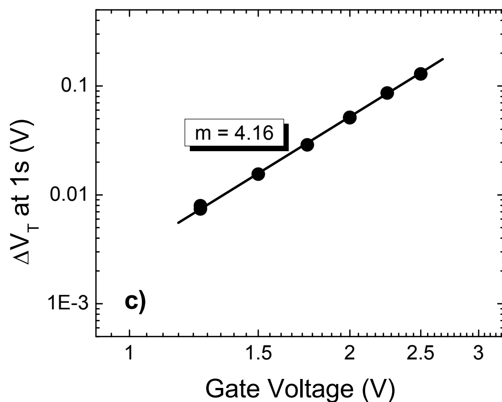
- Magnitude of shift / degradation depends on gate stack (material, thickness), voltage, temperature and time.

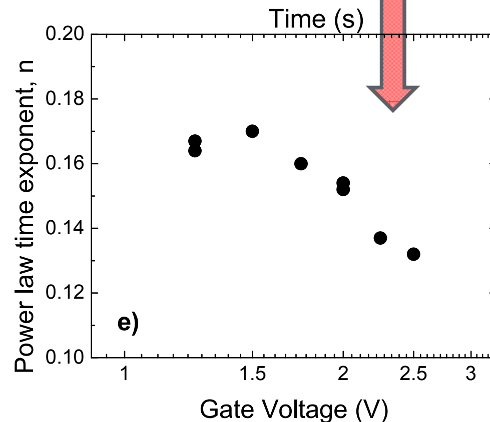
Typical NBTI dataset

A. Kerber, S. Krishnan, E. Cartier, IEEE EDL, VOL. 30, NO. 12, *pp. 1347–1349,* 2009.

- From CVS ΔVt – time traces voltage and time evolution is extracted
  - Note the sub-linear time and super-linear voltage dependence







BTI Degradation Metric

A.Kerber/McMahon, IRPS 2012 tutorial.

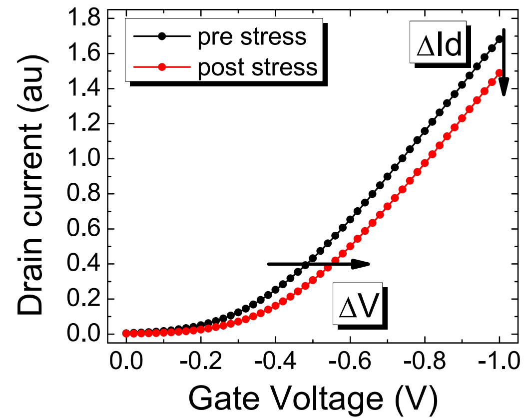
- BTI degradation is reported either as $\%I_{on}$ or more commonly as a V_t shift.
- Id can be approximated as $I_d = g_m(V_g - V_t)$

For negligible gm degradation

$$\frac{I_d - I_{d0}}{I_{d0}} = \frac{g_m(V_g - (V_t + \Delta V_t)) - g_m(V_g - V_t)}{g_m(V_g - V_t)}$$

$$\%I_d = \frac{\Delta V_t}{(V_g - V_t)}$$

- For V_{nom}=1V, V_t=0.3
- 10mV ➔ 0.01/0.7 = 1.4%



BTI measurement methods

- Stress-Measure-Stress (S-M-S)

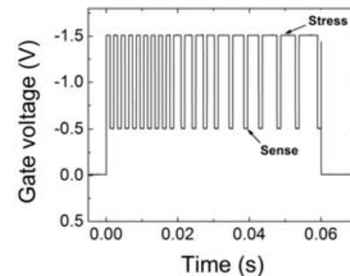
  ➔ challenge is to minimize delay time (intermittent Id-Vg versus spot Id)

- On the fly method

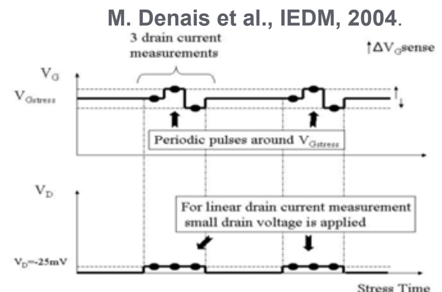
  ➔ challenge is to translate current degradation to voltage shift (issue of the t0 value)

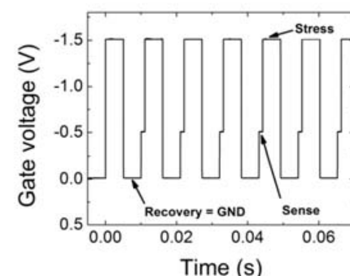
- AC BTI characterization

  ➔ insufficient by itself for comprehending recoverable part of degradation.

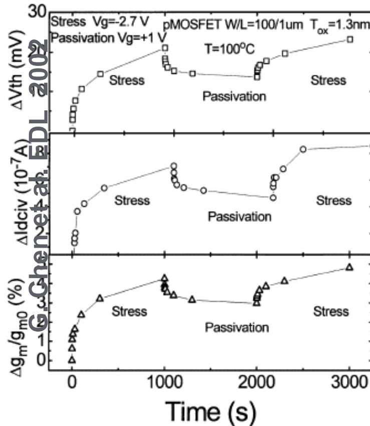


M. Denais et al., IEDM, 2004.

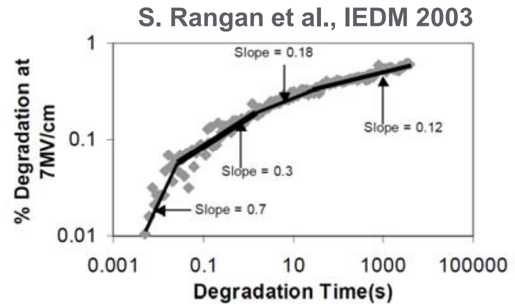


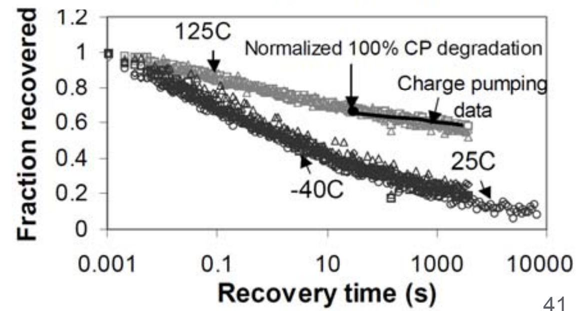


BTI Recovers and has Permanent and Recoverable Parts



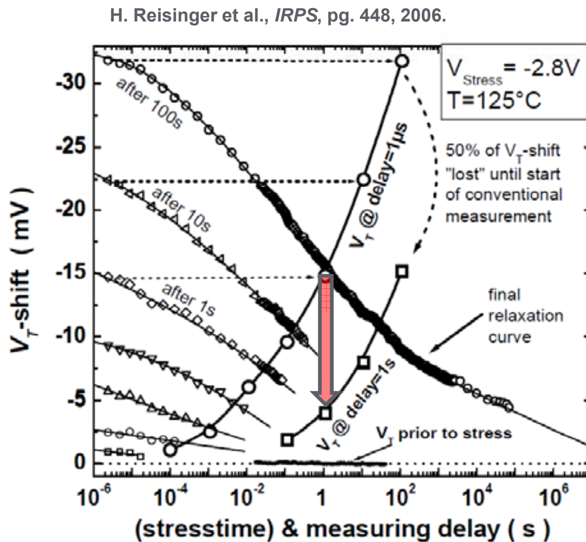
- NBTI recovers





- Unavoidable recovery during S-M-S distorts time dependence. When continuous Idlin is measured, time evolution not a simple power law
- At 125C, there is "lock-in" or permanent damage that is not recovered.

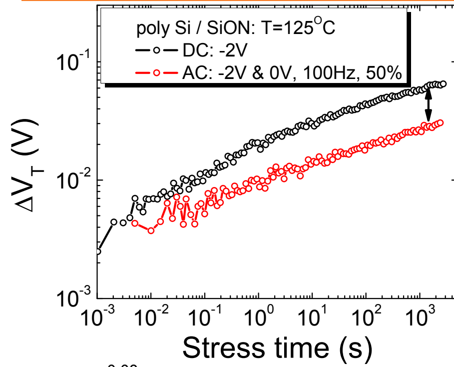
BTI recovery extended to μs delay times

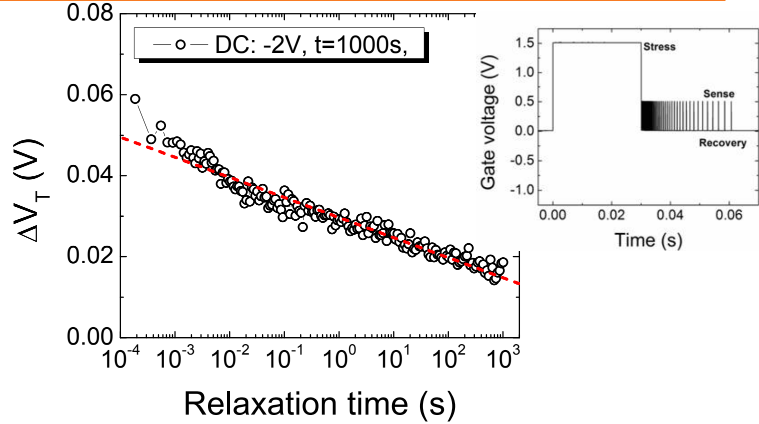


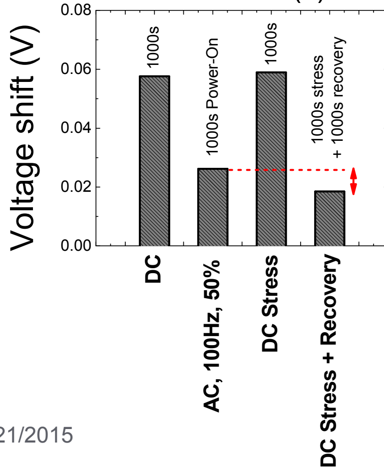
- Log(t) like recovery observed down to μs delay times
  - log(t) recovery implies equal amount of recovery per decade in time
- To accurately determine magnitude of shift, sense delay needs to be minimized

Challenges for dynamic BTI assessment

A.Kerber/McMahon, IRPS 2012 tutorial.



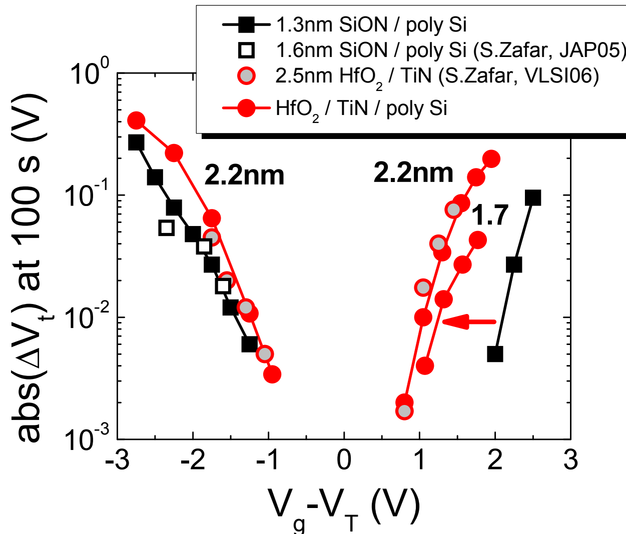




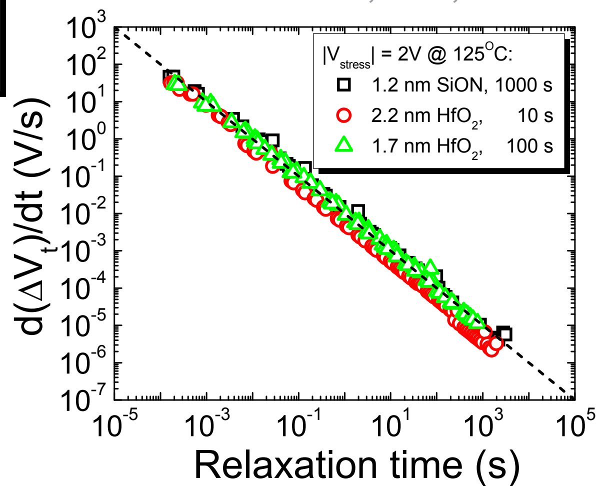
DC=1ms sense
DC Stress=no intermediate sense
AC 100Hz 50%≠DC Stress (1000s)+ Recovery (1000s)

Data from GLOBALFOUNDRIES(unpublished)

Comparison of BTI in MG/HK to conventional Poly Si / SiON gate stacks

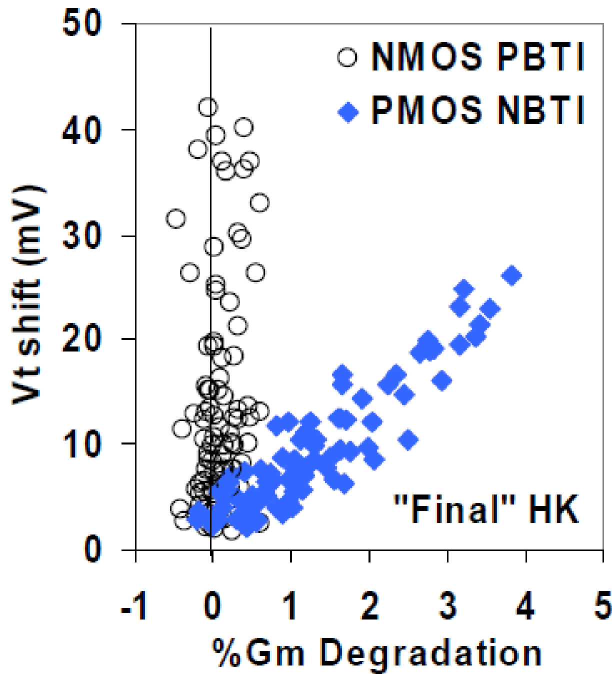


A. Kerber, et al., TED 2008



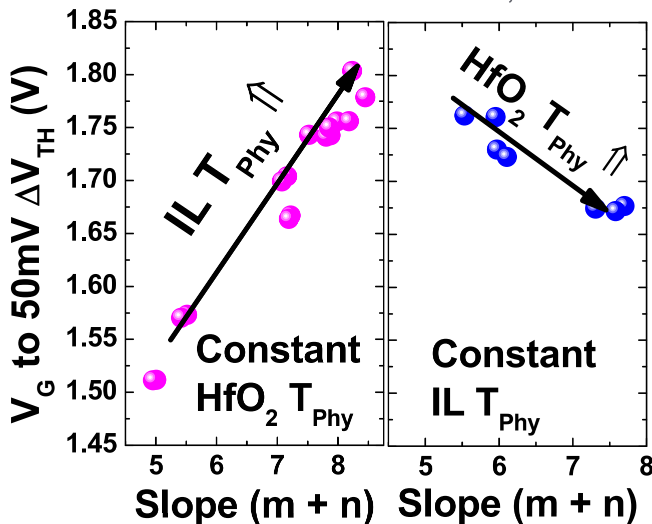
- With introduction of MG/HK into CMOS technologies PBTI has emerged as addition reliability challenge
- Magnitude of PBTI similar to NBTI for technology relevant gate stacks

NBTI versus PBTI in MG/HK



- NBTI:
  - Hole trapping
  - Hole trap generation at and near $Si\text{-}SiO_2$ interface in PFET
  - Interface trap generation and corresponding mobility degradation
- PBTI:
  - Electron trapping and trap generation in HfO_2 for HKMG NFET
  - No interface traps, no mobility degradation

Impact of interlayer and high-k layer thickness on VRS PBTI reliability parameter



- **Increase in interlayer (IL) thickness leads to:**
  - **Increase in V_G to 50mV**
  - **Increase in slope (m+n)**

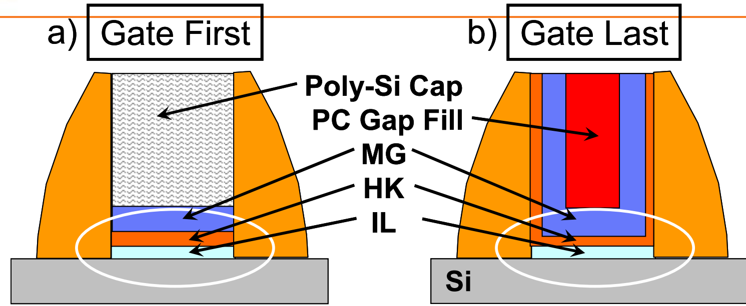
  ➔ substantial improvement in operation lifetime

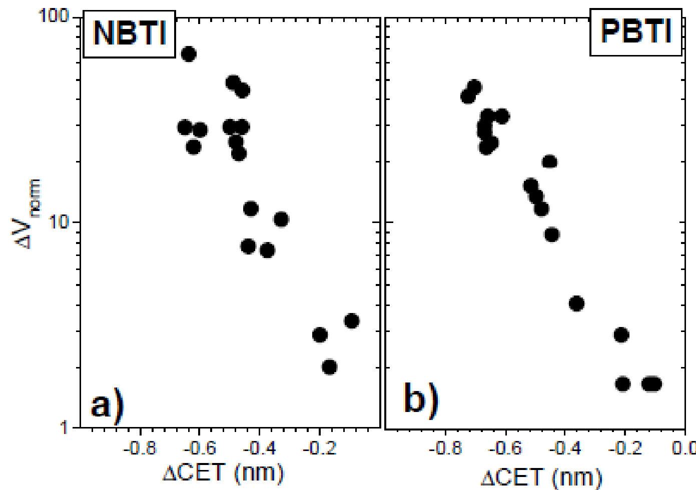
- **Increase in HfO_2 thickness leads to:**
  - **Decrease in Vg to 50mV**
  - **Increase in slope (m+n)**

  ➔ fairly constant lifetime at constant operating bias

Impact of CET scaling on NBTI & PBTI for Gate First and Gate Last processes

E. Cartier et al. (invited), IEDM 2011





- Gate First and Gate Last process follow a universal BTI – CET scaling trend
- Exponential xBTI – ΔCET relation makes gate stack scaling at constant VDD very difficult

Take away for BTI

- NBTI in SiON, PBTI + NBTI in HKMG.
- Both show similar voltage dependence and time evolution including recovery
- NBTI causes gm degradation in addition to Vt shift, PBTI only Vt shift.
- Controlling measurement delays is critical for assessing magnitude of BTI and extracting the time evolution
- Scaling Dieelctric thickness leads to significant increase in BTI.

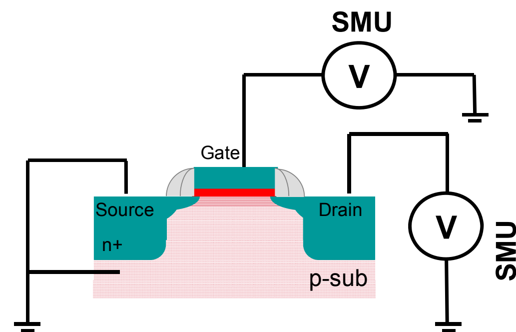
Hot Carrier Injection

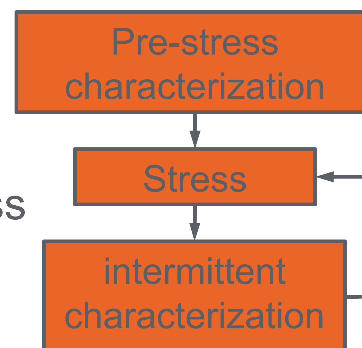
- Methods to study HCI
- Modeling HCI
- Challenges with HCI

Methods to Study HCI

A.Kerber/McMahon, IRPS 2012 tutorial.

- HCI is always studied with Vd high.
- Vg is a variable which needs explicit modeling for circuit level projection.
- Typically during qualification worst case Vg/Vd ratio is tested.
- Two approaches for testing
  - Constant Voltage Stress (Qualification)
  - Ramp Voltage Stress (Screening/Monitoring)
- Recovery is not typically observed in HCI and hence Stress Measure Stress (SMS) is used.





Modeling Idsat degradation

T. Nigam et al., IRPS, *pp. 634,* 2009.

- T0 degradation normalization: leading to Saturation Model for HCI

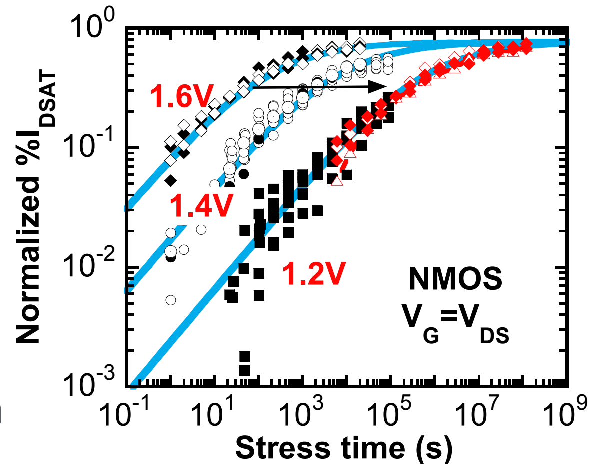
$$\% I_d = \frac{Id_0 - Id(t)}{Id_0} \cdot 100\% \sim \frac{t^n}{1+Bt^n}$$

  - 1/B, B=0.01 for saturation at 100% saturation.

- **Dynamic degradation normalization**

$$\%\left(1/Id\right) = \frac{\left(1/Id(t)\right) - \left(1/Id_0\right)}{\left(1/Id_0\right)} = \frac{Id_0 - Id(t)}{Id(t)}$$

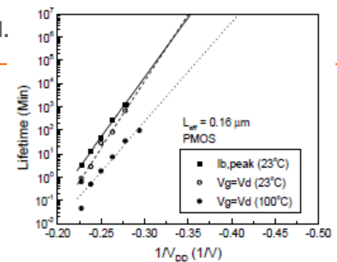
- $N_{it} \sim \frac{1}{\mu}$ **so 1/Id may be a better metric if N_{it} degradation dominates**



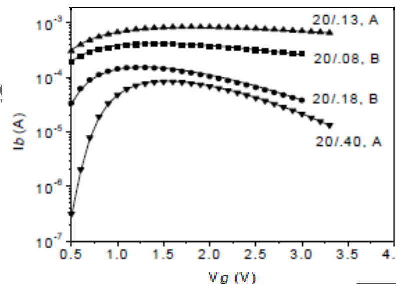
Challenges for HCI modeling as function of Lg

A.Kerber/McMahon, IRPS 2012 tutorial.

- E_a changes from positive to negative

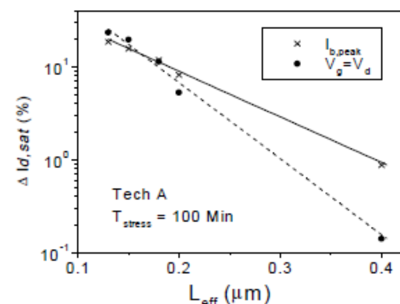


- I_{sub_max} increases from V_g to $V_g \sim V_d$



E. Li et al. IRPS p. 4A.6 1999

- Peak HCI shifts from $V_g < V_d$ to $V_g \sim V_d$ as evident from the channel length dependence of Idsat



Challenges with DC to AC Correlation for short channel HCI

A.Kerber/McMahon, IRPS 2012 tutorial.

Model 1 **(see, e.g. McMahon et al. Trans. Nanotech. p. 33 2002)**

- Multiple carrier bond breaking
- Single Electron Energy < Bond Energy hence multiple electrons required to break bond.

But

- Excitation time >> switching times.

Model 2 **(see, e.g. Rauch IRPS Tutorial 2010)**

- Local self-heating NBTI
- Local self-heating accelerates N/PBTI process, causing high apparent degradation

But

- Self-heating time >> switching times.

Quasi-static approximation breaks down. AC ≠ (integrated) DC.

All models suggest that DC HCI measurements are not meaningful for AC lifetime prediction

Take away for HCI

A.Kerber/McMahon, IRPS 2012 tutorial.

- Worst case DC hot carrier degradation shifts from Isub max to Vg=Vd condition for ~ <200nm devices
- BTI contributions are inherently present in advanced technology nodes (poly Si / SiON pFETs and MG/HK n/pFETs) and the separation is not trivial
- Device degradation >10% only properly capture with saturation models
- All models unable to capture AC to DC translation since quasi static approximation breaks down

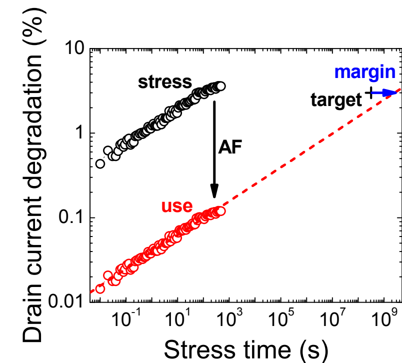
Basic BTI/HCI projection methodology

- Saturation drain current degradation at use condition translated by multiplying the current degradation at stress condition with various acceleration factors

$$\Delta Id_{use} = \Delta Id_{stress} \cdot AF_{Vg} \cdot AF_{Vd} \cdot AF_{time} \cdot AF_{temp} \cdot AF_{width} \cdot AF_{length} \cdot AF_{percentile}$$

- ΔId_{stress} is the current degradation at reference Vg, Vd, T_{OX}, T and frequently call the pre-factor (e.g. A)

$$\Delta Id_{stress} = A\left(Vg_{ref}, Vd_{ref}, T_{ref}\right)$$

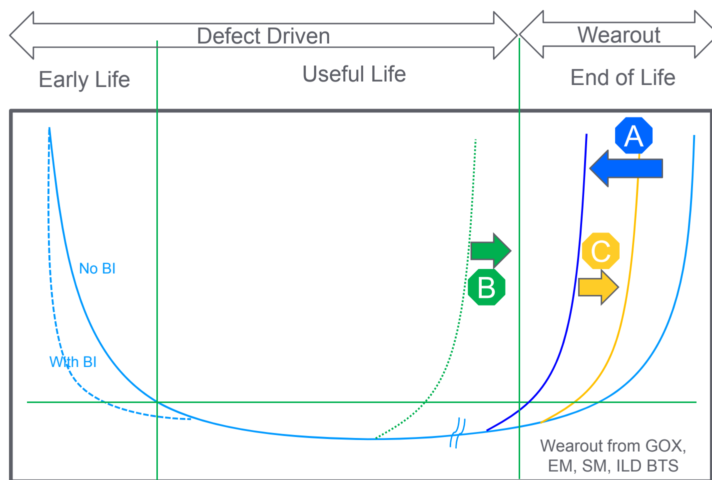


- The various acceleration factors are related to the reference condition

Outline

- Introduction
  - Industry overview
  - Role of Reliability Engineer in Technology Development
- Scaling Roadmap and its enablement
  - What is scaling and what is not scaling…
- Basics of FEoL Reliability Mechanisms
  - BTI
  - HCI
  - TDDB
- Moving beyond 20nm
  - Product level degradation
  - New Channel materials

Product Reliability



- **A** Reduction in Intrinsic Lifetime with Scaling
  - Limited to no Vdd reduction with node scaling
  - Tinv /Design Rule ↓ @ ~ same Vdd
  - Higher power density: Temperature ↑
  - More functionality, SOC complexity: Chip Area ↑
  - Aggressive Burn-In incorporation leads to earlier wear-out
- **B** Enhanced product wear out correlation to Device/Circuit-level REL models
  - Better understanding of physics of wear out
  - Methodology enhancements: TDDB PBD, BTI recovery, EM SEB, BTS SBB
- **C** Design for Reliability
  - Degradation-aware design
  - Increased margin to failure by circuit- and architectural-level compensation

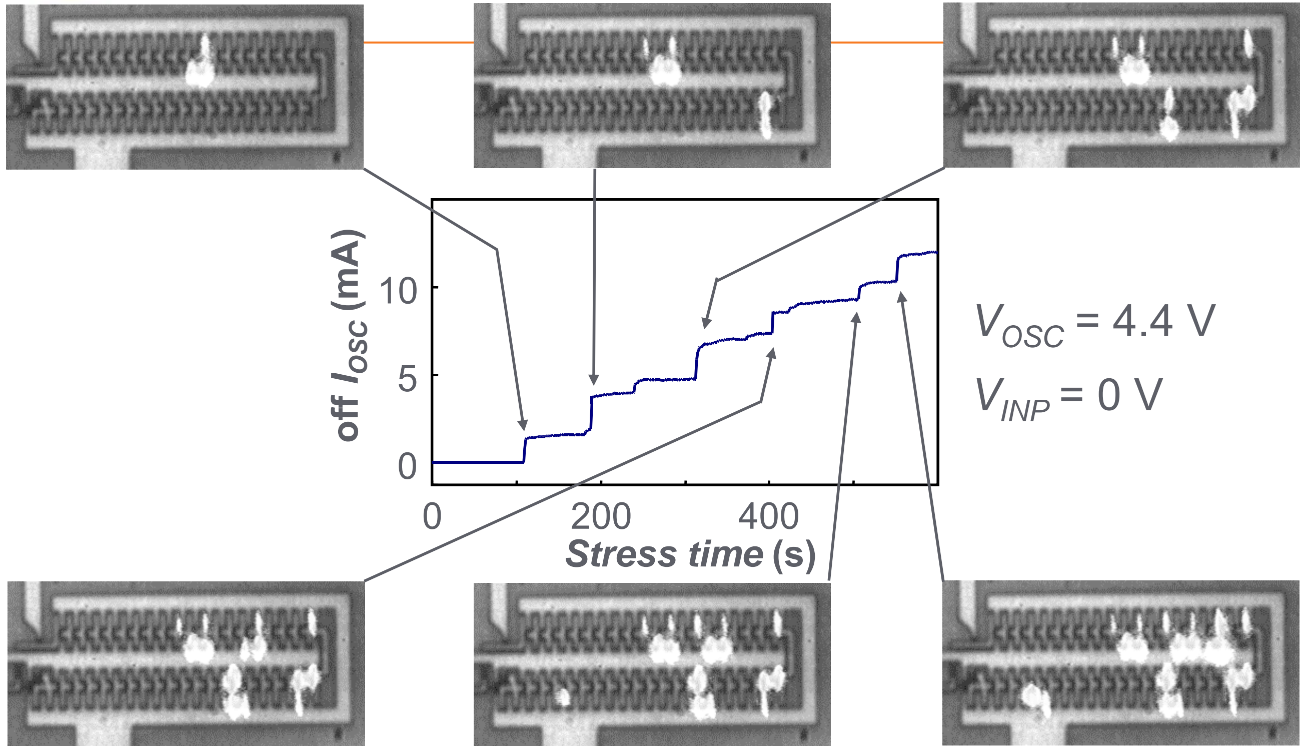
- Predictive capability improvement and increased design for reliability required to offset margin reduction from scaling to produce reliable products.

Enabling technology via device to circuit correlation understanding

1st Breakdown does not destroy Transistor functionality

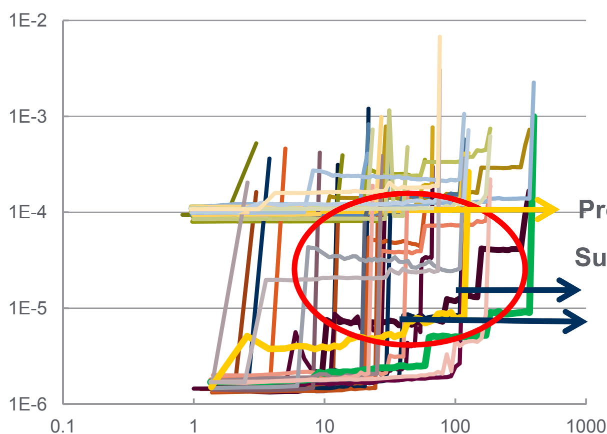
- Impact of oxide breakdown on circuits then depends on post breakdown defect generation and circuit sensitivity to enhanced leakage.
  - Successive breakdown and circuit implications
    - Multiple breakdown spots in a given area
  - Progressive breakdown and circuit implications
    - Growth of the 1st SBD spot into HBD
- Fmax guard banding critical for products
  - Using RO degradation as proxy one can provide a DC to AC level correlation going from device level models to circuit implication
- SRAM sensitivity to BTI
  - Using simple circuits like Cross coupled Inverters device degradation and recovery in SRAM like environment can be studied

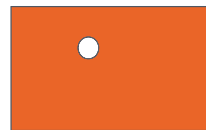
Current jumps correlated to gate oxide BDs

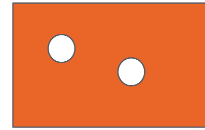


"Satellite" spots identified as hot carrier emission by spectral and SPICE analysis

Progressive breakdown in TDDB (HK MG)



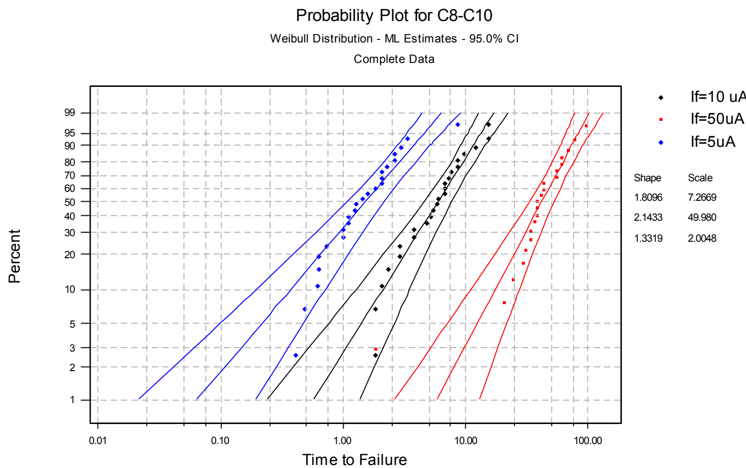




Suñé/Wu/Lai, TED,2004
Alam, IEDM 2002
Monsieur *et al.* IRPS, 45, 2002,
Hosoi *et al.* IEDM, 155, 2002,
Linder/Stathis *et al.* EDL, 661, 2002;
IRPS, 402, 2003

- Progressive and successive breakdown is observed for large area devices.
- Both enhance lifetime and increases Weibull slope.

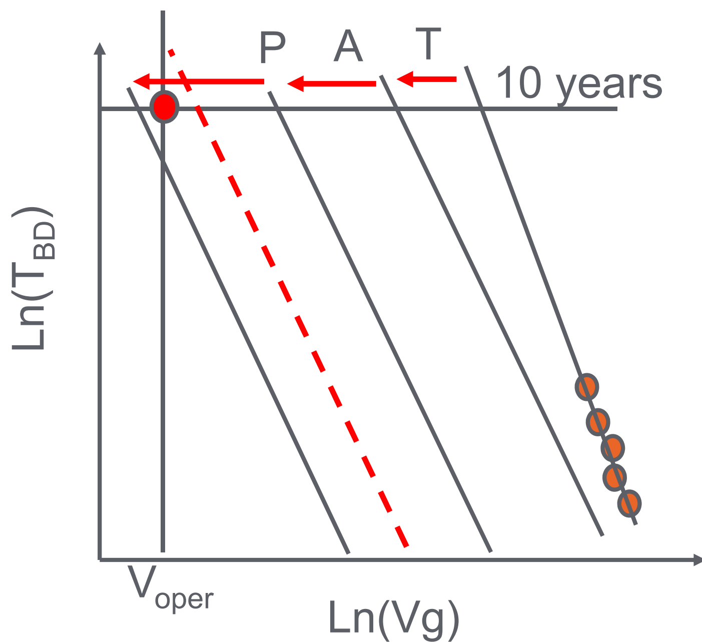
Progressive Breakdown (HK MG)



Ifail	Weibull Slope	Vmax (V)
1uA	1.1	1.0
5uA	1.35	1.1
10uA	1.8	1.25
50uA	2.14	1.35

- Both t63 and Weibull slope increases with increase in acceptable Ifail.
- Vmax boost of 350mV if Ifail increase to 50uA.

Product lifetime extraction

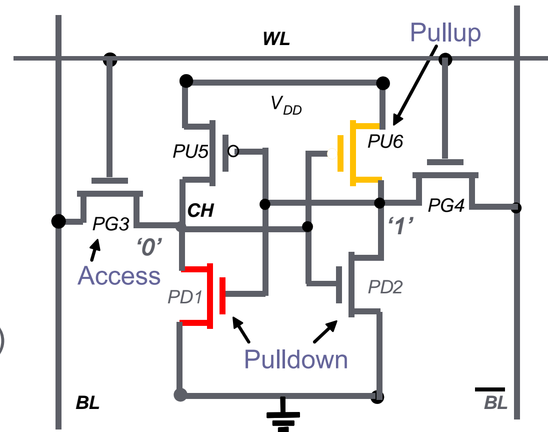


- Voltage Scaling
- Temperature Scaling
- Area Scaling
- Percentile Scaling
- Percentile Scaling with n-SBD or progressive SBD

6T SRAM Cell – role of PBTI and NBTI

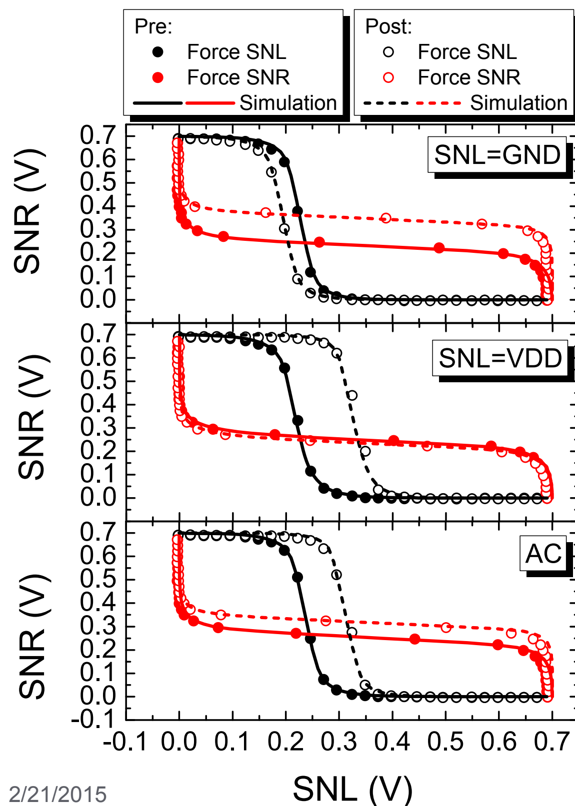
Read disturb example

- When the cell holds a certain state (say ‘0’) PD1 and PU5 are under “DC” PBTI stress
- Weaker PD1 + weaker PU6 increases read disturb
  - Increases read Vmin
- Area of Focus needed
  - BTI(Vdd, time exponent, and recovery)
  - Recovery at time scales that matter (<us)
  - Understanding of these mechanisms better will aid in a better overall attribute for SRAMs



Comparison of measured and modeled CCI transfer characteristics

A. Kerber, et al., IRPS 2011

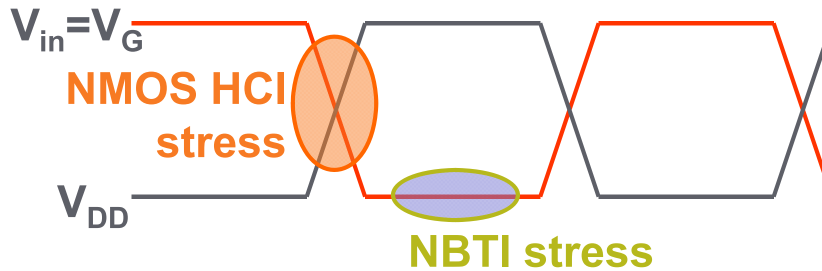


- Simulated CCI transfer characteristics using SPICE model match experimental data well
  - Based on pre- and post- stress device characteristics
- ➔ **SRAM degradation follows device level BTI drift and recovery**

RO Frequency Degradation

T. Nigam, et al., IRPS 2009

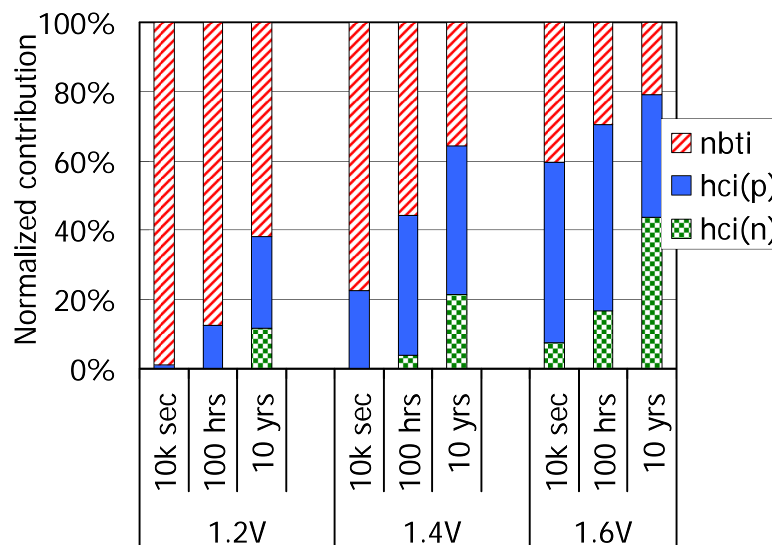
$$\Delta f / f = \frac{1}{2}((\tau_n / \tau).\Delta I_{dsatn} / I_{dsatn} + (\tau_p / \tau).\Delta I_{dsatp} / I_{dsatp})$$



- HCI Occurs only during switching and the equivalent stress time is a function of rise and fall time ($t_{eq}=t_{use}.Z(t_r/t_f)$)
- NBTI occurs only during off state and so $t_{eq}= t_{use}/2$

Individual Components - II

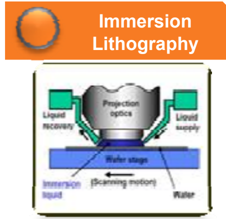
T. Nigam, et al., IRPS 2009



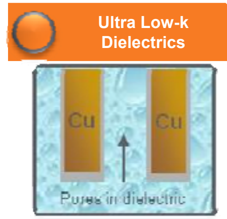
- Process optimization needs to comprehend the individual components at the typical operating voltage

Beyond 20nm: What's Next?

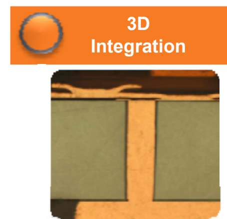
Immersion Lithography



Ultra Low-k Dielectrics

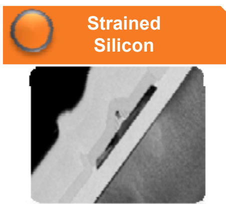


3D Integration

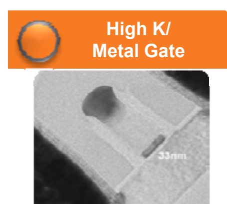


Extreme Ultraviolet (EUV)

Strained Silicon

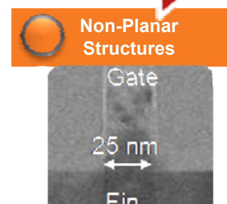


High K/ Metal Gate



Source Mask Optimization

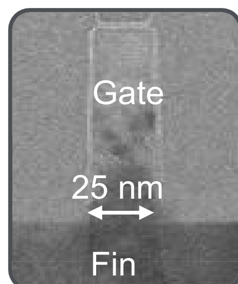
Non-Planar Structures

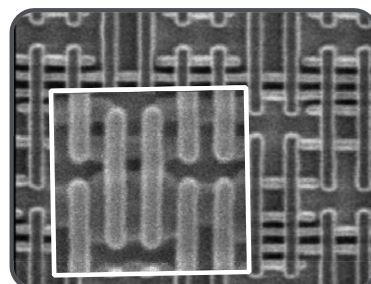


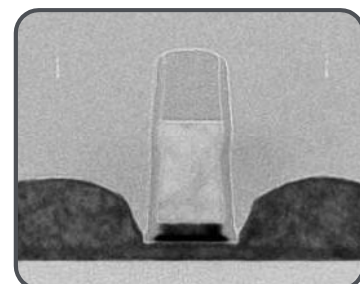
14nm and Beyond

- Multi-gate FinFET
  - New transistor structure
  - Smaller geometries
  - Low operating voltage for power/performance improvement
  - Successfully demonstrated in SRAM
- Source Mask Optimization
  - Improves pattern fidelity on wafers by computational optimization of lithography light source and reticle

- ETSOI
  - Geometrical confinement reduces leakage
- Further innovations
  - Packaging
  - Novel device architectures (III-V, Ge channels)
  - Ultimate replacement for the CMOS switch







Summary

- Semiconductor industry on path towards sub 20 nm technology
  - Key Challenges continue to be
    - Lithography
    - Material innovation and integration with an eye towards manufacturability
    - Building in Reliability Margins
- Reliability Challenges
  - Comprehend and model the impact of material change
  - Develop fundamental physical understanding
  - Leverage learning from other areas
  - Comprehend and link device level degradation to circuit level degradation
  - Provide designer with tools to build reliability aware designs

Acknowledgements

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