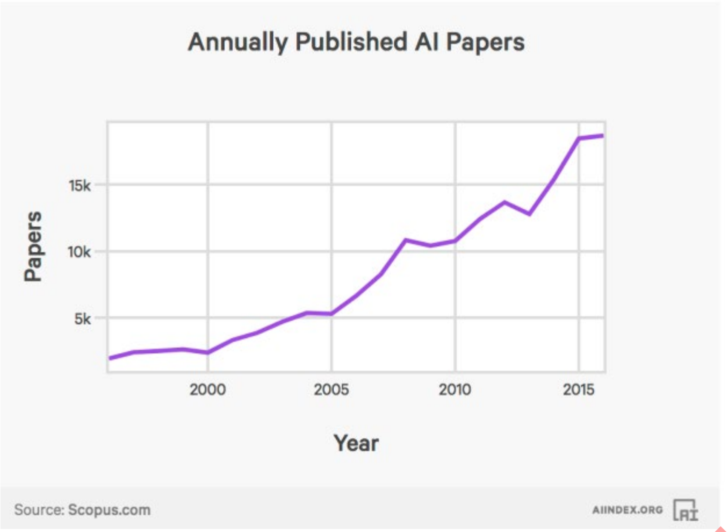
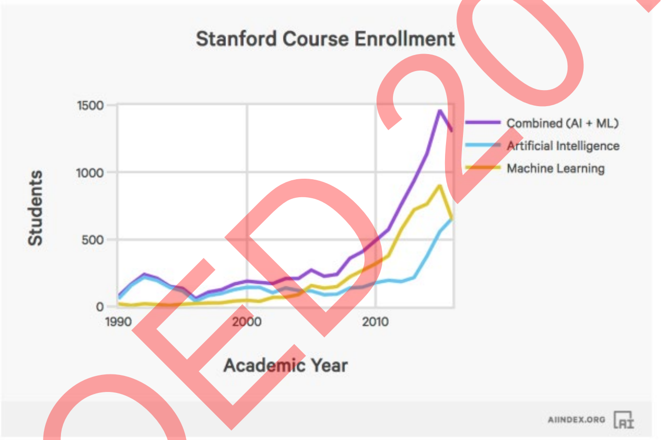
GOLDEN AGE OF MACHINE LEARNING *FOR EDA*

Amit Gupta
General Manager, IC Verification Solutions Solido
Mentor, a Siemens Business

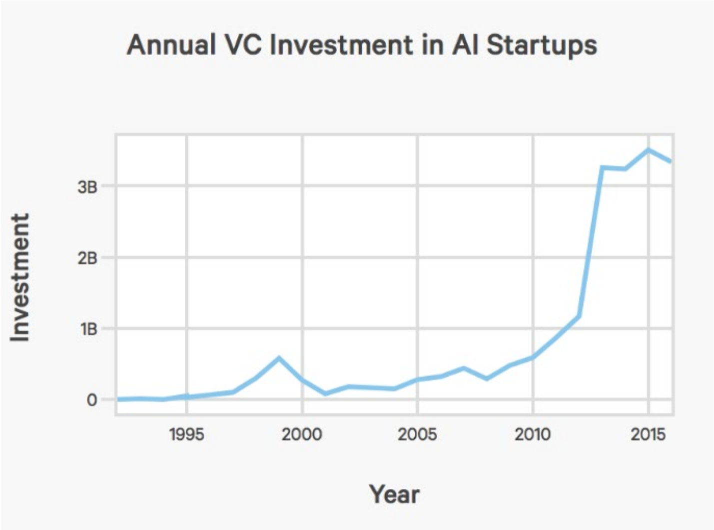
Artificial Intelligence having a profound impact on society

Artificial Intelligence activity dramatically increasing

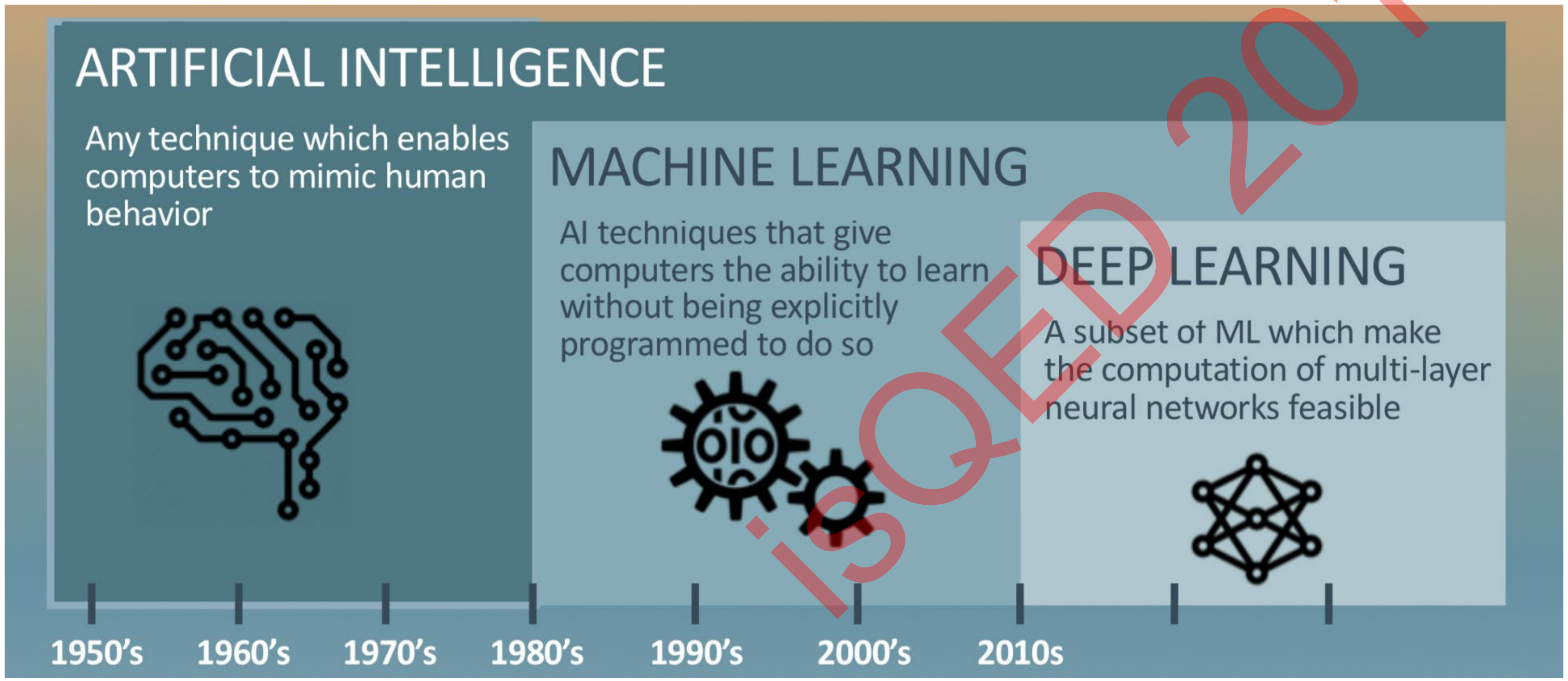


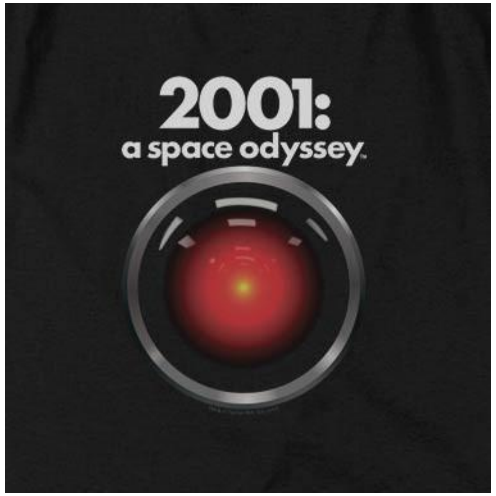


11x *Introductory AI class enrollment at Stanford has increased 11x since 1996.*



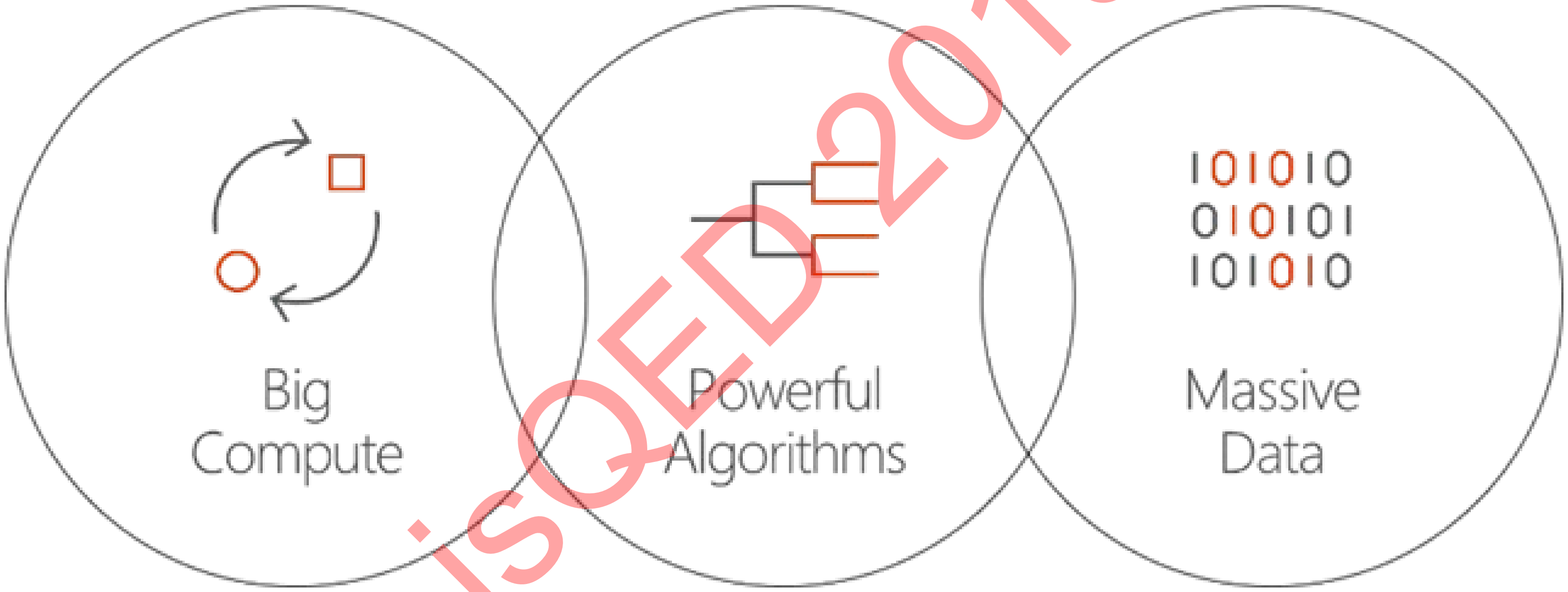
Evolution of AI





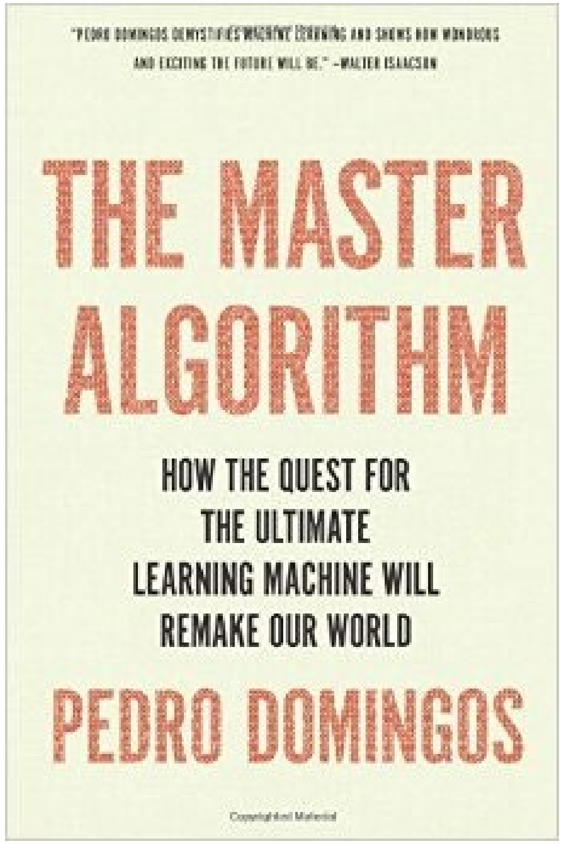
Source: Oracle

What enables AI?



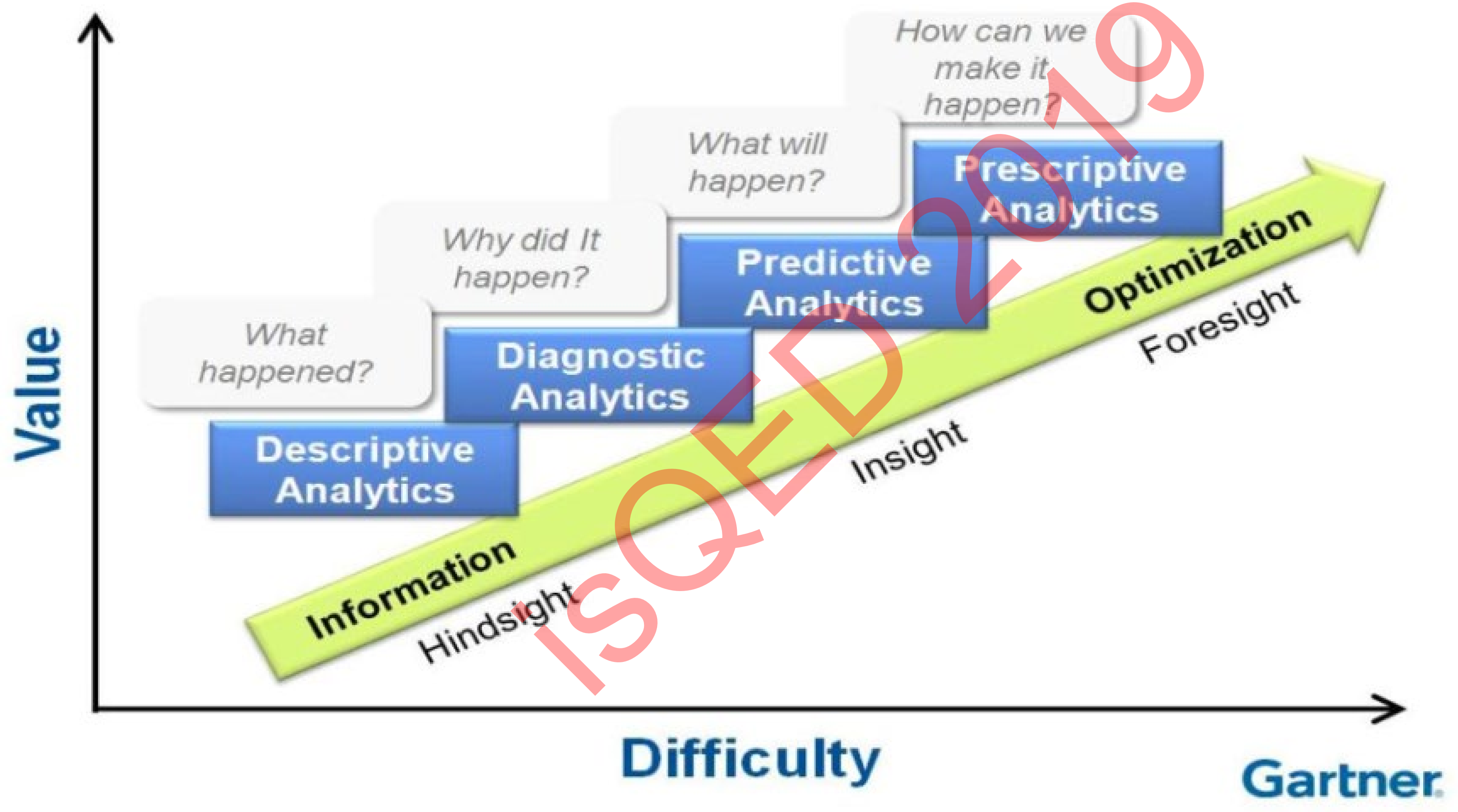
Machine Learning Approaches

- Symbolists
  - Inverse deduction approach
- Connectionists
  - Modeling the brain
- Evolutionaries
  - Simulate evolutionary biology
- Bayesians
  - Probabilistic inference
- Analogizers
  - Extrapolating with support vector machines

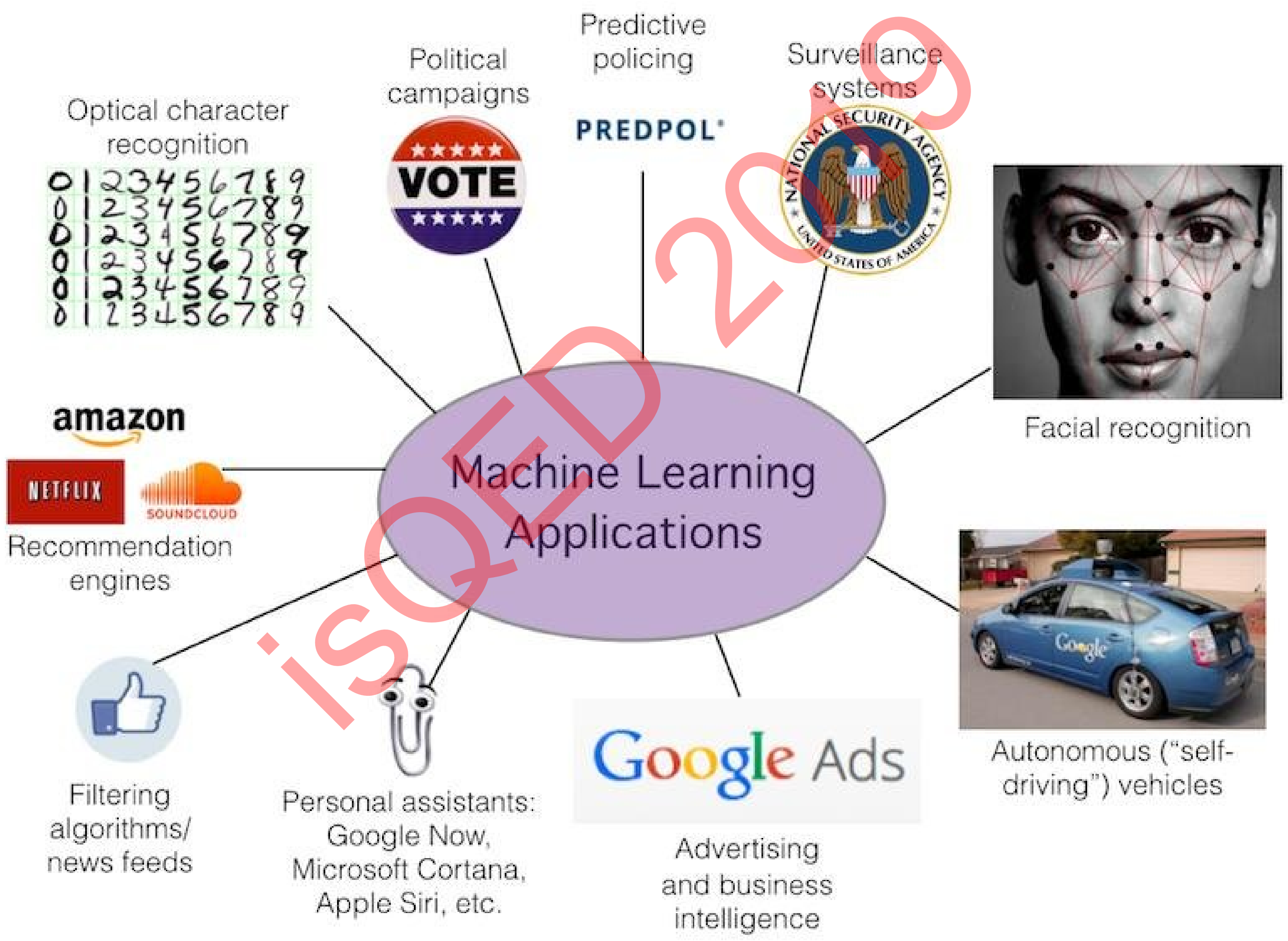


Data is the fuel

AI Driving Customer Value



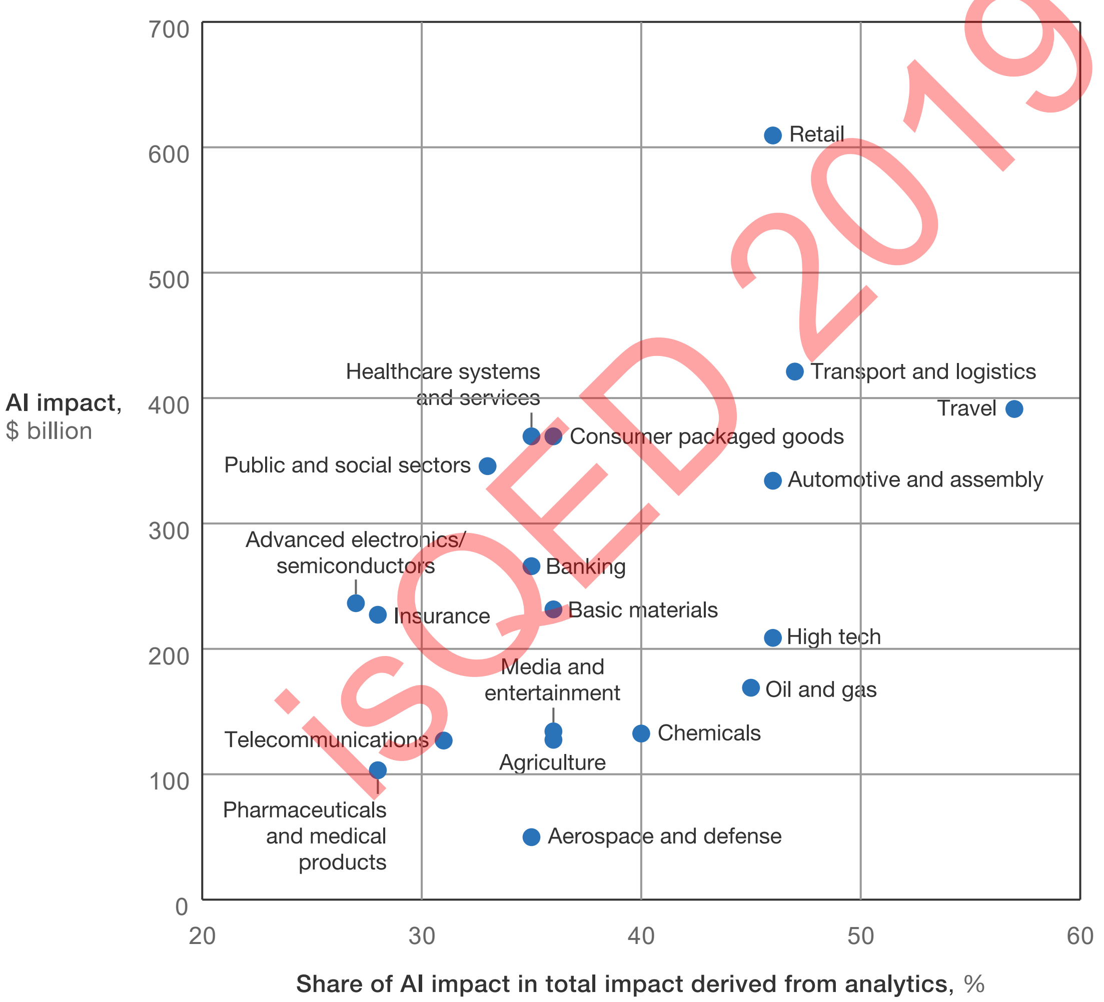
Machine Learning applied



Source: Research Gate

$ impact of AI

Artificial intelligence (AI) has the potential to create value across sectors.

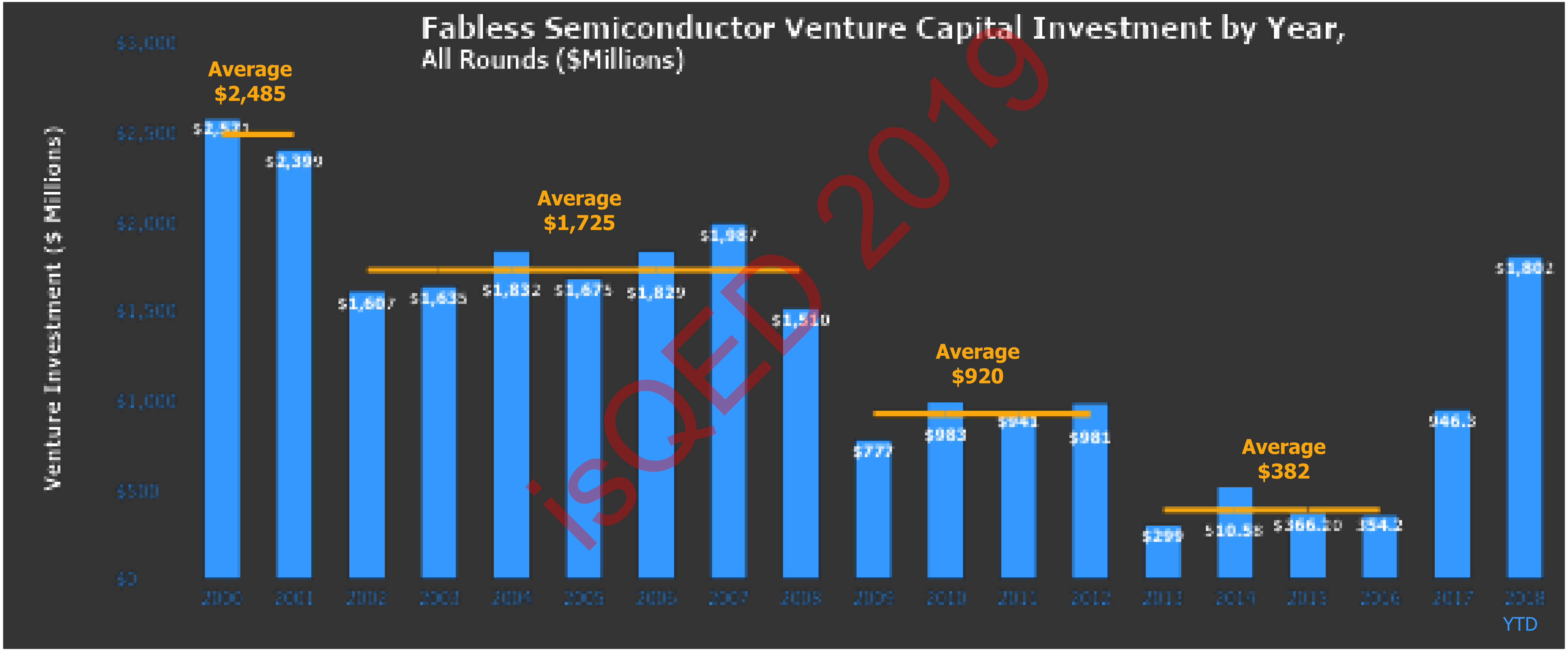


McKinsey&Company | **Source:** McKinsey Global Institute analysis

Democratizing Machine Learning

Source: Google

Venture Capital Investment in Fabless Semiconductor Startups



Source: Global Semiconductor Alliance (GSA) , IMF, VentureSource, Pitchbook, Crunchbase, & Mentor Graphics Analysis Rev 8/16/18

AI in Semiconductor: Neuromorphic vs. Von Neumann Architecture

	What They Do Well	What They're Good For
Neuromorphic Chips	Detect and predict patterns in complex data using relatively little electricity	Applications that are rich in visual or auditory data and require a machine to adjust its behavior as it interacts with the world
Traditional Chips (Von Neumann)	Readily make precise calculations	Anything that can be reduced to a numerical problem although more complex problems require substantial amounts of power

Source: MIT Technology Review, Neuromorphic Chips – Microprocessors configured more like Brains Than Traditional Chips Could Soon Make Computers far More Astute About What is going on Around Them, Robert D. Hof

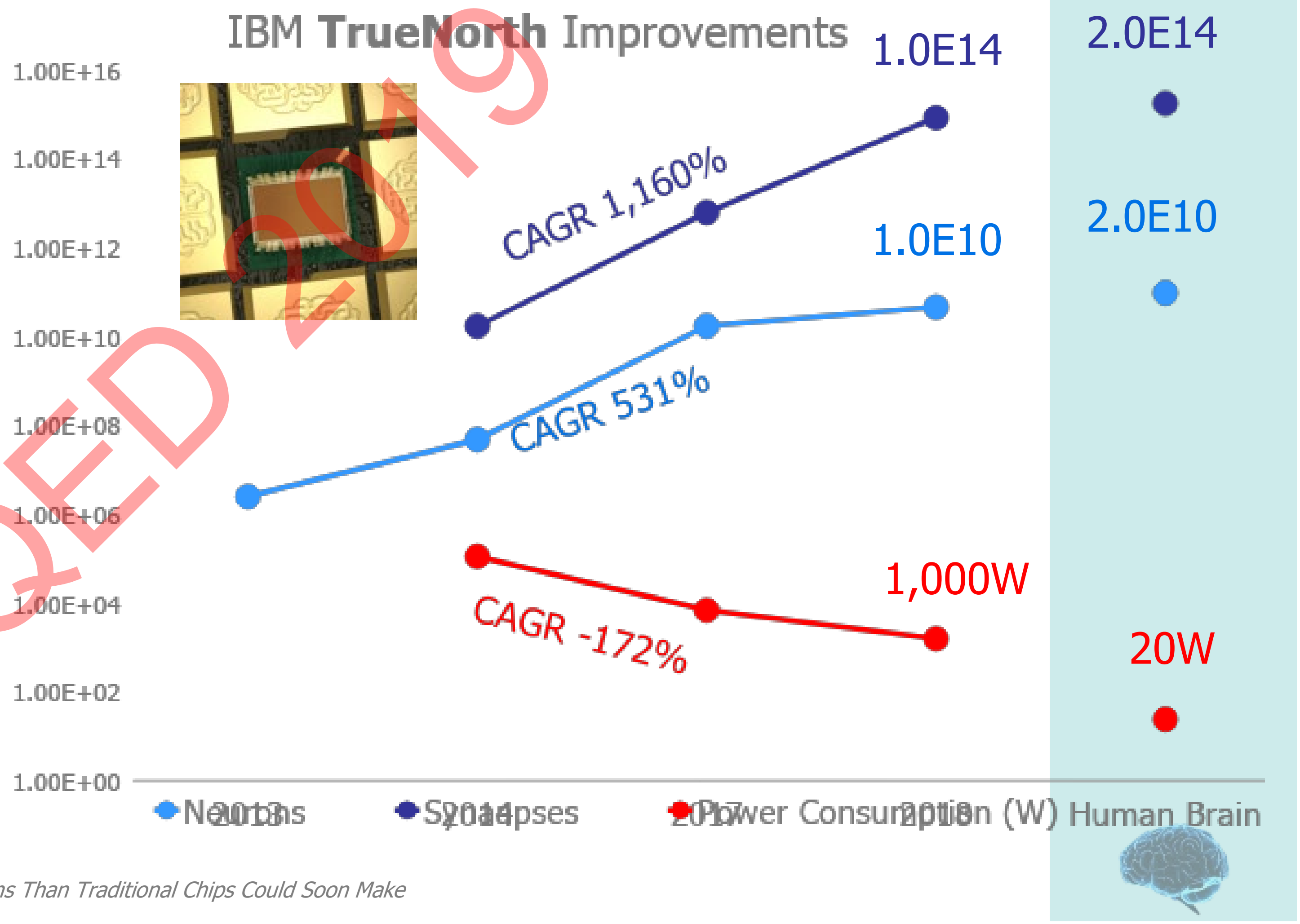
Requirements for Brain-Like Pattern Recognition

Memory improvements

- Increased capacity
- Hierarchical memory
- Memory cell connectivity
- "Invariant" memory

Processor architecture improvements

- Parallelism
- Error tolerance
- Continuous feedback
- Integration with memory

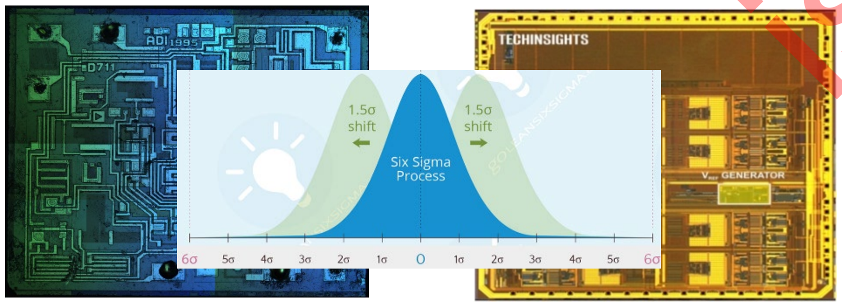


Source: MIT Technology Review, Neuromorphic Chips – Microprocessors configured more like Brains Than Traditional Chips Could Soon Make Computers far More Astute About What is going on Around Them, Robert D. Hof

Machine Learning for EDA

Domain expertise in Machine Learning and Variability; Software solutions for IC Analysis and Characterization

Advanced Analysis & Characterization of Integrated Circuits Spanning Analog, RF, Digital, and Memory.



Press Release

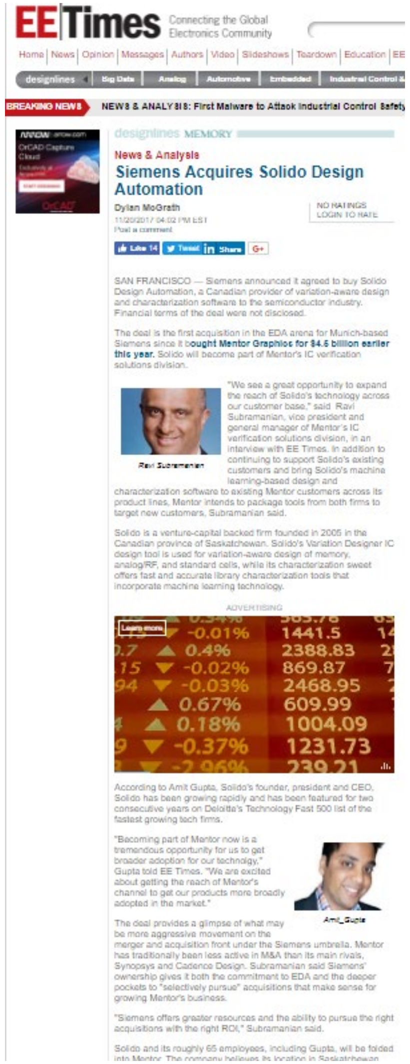
Plano, Texas, November 20, 2017

Siemens strengthens IC market commitment with acquisition of Solido Design Automation

- Siemens to acquire the leading provider of machine learning-based variation-aware design and characterization software, growing its commitment to Mentor's integrated circuit (IC) design and verification technology
- Siemens continues to build upon its digitalization strategy and to expand its software business in North America and Canada

Siemens has entered into an agreement to acquire Saskatoon, Canada-based Solido Design Automation Inc., a leading provider of variation-aware design and characterization software to semiconductor companies worldwide. Solido's machine learning-based products are currently used in production at over 40 major companies, enabling them to design, verify, and manufacture more competitive products than ever before. The acquisition of Solido further expands Mentor's Analog/mixed-signal (AMS) verification portfolio to help customers address the growing challenges of IC design and verification for automotive, communications, data-center computing, networking, mobile, and IoT applications. The terms of the transaction are not disclosed. Siemens expects to close the transaction in early December 2017.

"With the acquisition of Mentor we made a large commitment to EDA," said Tony Hemmelgarn, president and CEO of Siemens PLM Software. "This new acquisition of Solido strengthens that presence and demonstrates our commitment to serving our customers in the IC industry."



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News & Analysis

Siemens Acquires Solido Design Automation

Dylan McGrath
11/20/2017 04:02 PM EST
Post a comment

NO RATINGS
LOGIN TO RATE

SAN FRANCISCO — Siemens announced it agreed to buy Solido Design Automation, a Canadian provider of variation-aware design and characterization software to the semiconductor industry. Financial terms of the deal were not disclosed.

The deal is the first acquisition in the EDA arena for Munich-based Siemens since it **bought Mentor Graphics for $4.5 billion earlier this year.** Solido will become part of Mentor's IC verification solutions division.

Ravi Subramanian

"We see a great opportunity to expand the reach of Solido's technology across our customer base," said Ravi Subramanian, vice president and general manager of Mentor's IC verification solutions division, in an interview with EE Times. In addition to continuing to support Solido's existing customers and bring Solido's machine learning-based design and characterization software to existing Mentor customers across its product lines, Mentor intends to package tools from both firms to target new customers, Subramanian said.

Solido is a venture-capital backed firm founded in 2005 in the Canadian province of Saskatchewan. Solido's Variation Designer IC design tool is used for variation-aware design of memory, analog/RF, and standard cells, while its characterization sweet offers fast and accurate library characterization tools that incorporate machine learning technology.

According to Amit Gupta, Solido's founder, president and CEO, Solido has been growing rapidly and has been featured for two consecutive years on Deloitte's Technology Fast 500 list of the fastest growing tech firms.

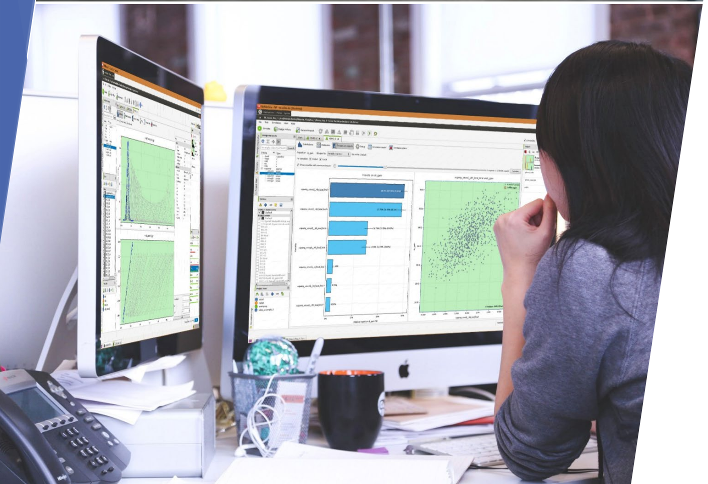
"Becoming part of Mentor now is a tremendous opportunity for us to get broader adoption for our technolgy," Gupta told EE Times. "We are excited about getting the reach of Mentor's channel to get our products more broadly adopted in the market."

Amit_Gupta

The deal provides a glimpse of what may be more aggressive movement on the merger and acquisition front under the Siemens umbrella. Mentor has traditionally been less active in M&A than its main rivals, Synopsys and Cadence Design. Subramanian said Siemens' ownership gives it both the commitment to EDA and the deeper pockets to "selectively pursue" acquisitions that make sense for growing Mentor's business.

"Siemens offers greater resources and the ability to pursue the right acquisitions with the right ROI," Subramanian said.

Solido and its roughly 65 employees, including Gupta, will be folded into Mentor. The company believes its location in Saskatchewan

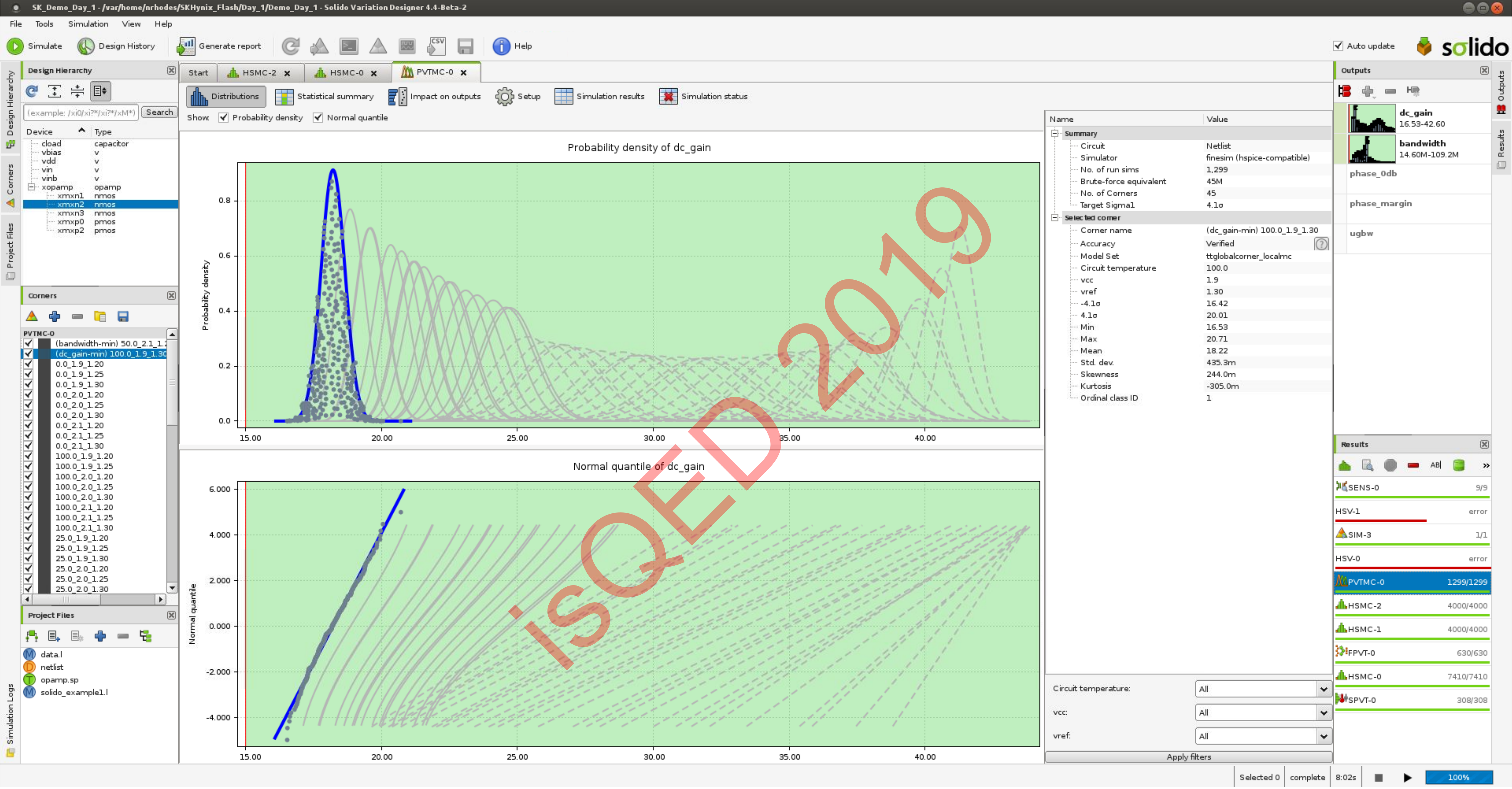


The solido Story

- **Founded: 2005**
- Mission: Variation-aware design and characterization technologies
- Differentiation: Machine learning and usability
- Team: Includes Machine learning and HCI experts
- Locations: Saskatoon, Canada (+ a few ww staff)
- Research: 14 patents total, 9 ML patents, 100s of trade secrets
- Products: Variation Designer and ML Char Suite
- Users: 1000s of production chip designers
- Customers: Most of the top-40 semiconductor companies
- **Dec. 1, 2017: Acquired by Mentor, a Siemens Business**

Solido Products

Variation Designer	ML Characterization Suite
Machine Learning for 1,000x+ faster and more thorough verification	*Machine Learning for reducing library characterization time by up to 70%*


SK_Demo_Day_1 - /var/home/nrhodes/SKHynix_Flash/Day_1/Demo_Day_1 - Solido Variation Designer 4.4-Beta-2
File Tools Simulation View Help
Simulate
Design History
Generate report
Help
Auto update
solido
Design Hierarchy
Search
Device Type
cload capacitor
vbias v
vdd v
vin v
vinb v
xopamp opamp
xmxn1 nmos
xmxn2 nmos
xmxn3 nmos
xmxp0 pmos
xmxp2 pmos
Corners
PVTMC-0
(bandwidth-min) 50.0_2.1_1.2
(dc_gain-min) 100.0_1.9_1.30
0.0_1.9_1.20
0.0_1.9_1.25
0.0_1.9_1.30
0.0_2.0_1.20
0.0_2.0_1.25
0.0_2.0_1.30
0.0_2.1_1.20
0.0_2.1_1.25
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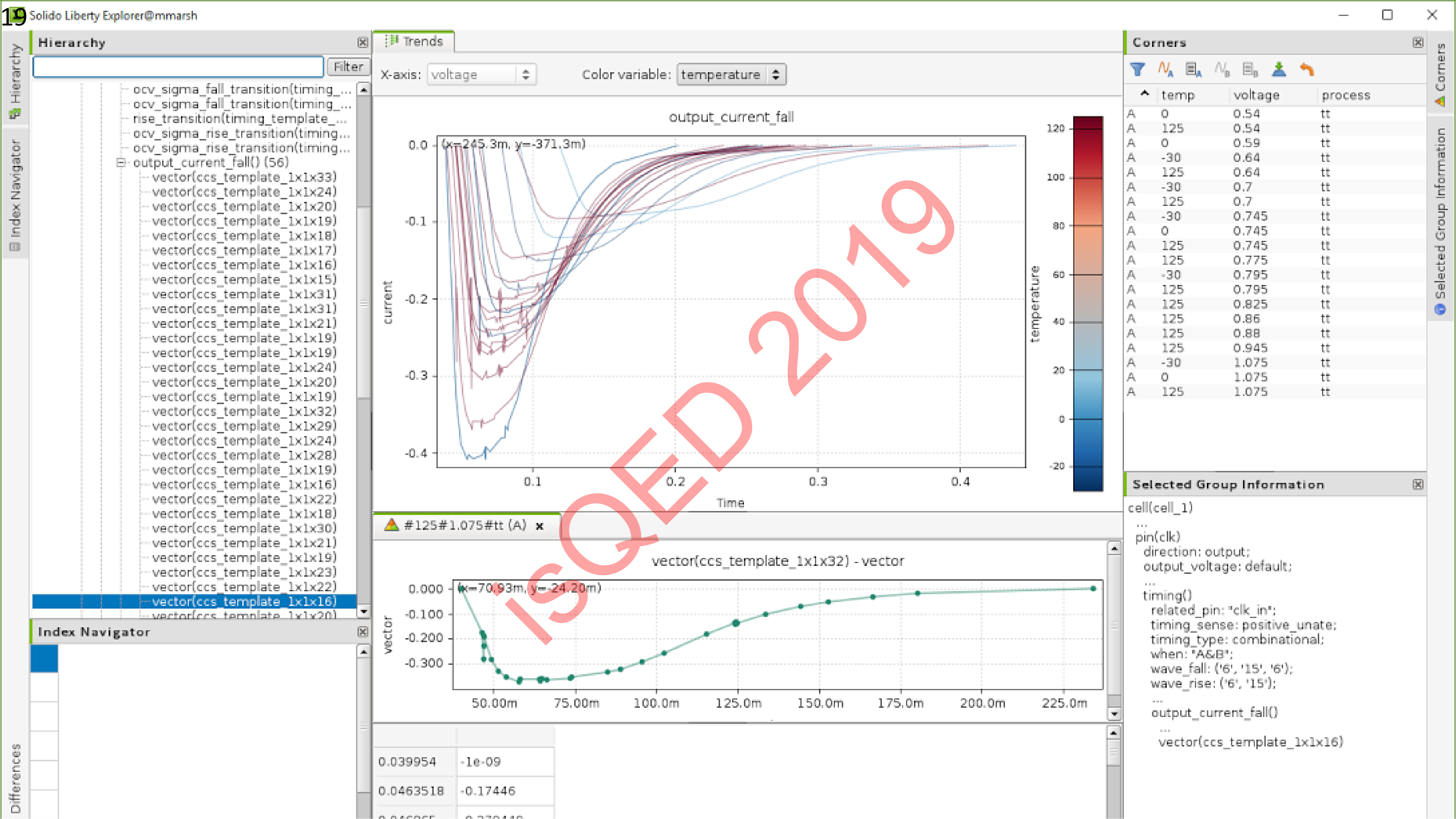
25.0_2.0_1.30
Project Files
data.l
netlist
opamp.sp
solido_example1.l
Simulation Logs
Start
HSMC-2
HSMC-0
PVTMC-0
Distributions
Statistical summary
Impact on outputs
Setup
Simulation results
Simulation status
Show: Probability density Normal quantile
Probability density of dc_gain
Probability density
0.8
0.6
0.4
0.2
0.0
15.00 20.00 25.00 30.00 35.00 40.00
Normal quantile of dc_gain
Normal quantile
6.000
4.000
2.000
0.000
-2.000
-4.000
15.00 20.00 25.00 30.00 35.00 40.00
iSQED 2019
Name Value
Summary
Circuit Netlist
Simulator finesim (hspice-compatible)
No. of run sims 1,299
Brute-force equivalent 45M
No. of Corners 45
Target Sigma1 4.1σ
Selected corner
Corner name (dc_gain-min) 100.0_1.9_1.30
Accuracy Verified
Model Set ttglobalcorner_localmc
Circuit temperature 100.0
vcc 1.9
vref 1.30
-4.1σ 16.42
4.1σ 20.01
Min 16.53
Max 20.71
Mean 18.22
Std. dev. 435.3m
Skewness 244.0m
Kurtosis -305.0m
Ordinal class ID 1
Circuit temperature: All
vcc: All
vref: All
Apply filters
Outputs
dc_gain 16.53-42.60
bandwidth 14.60M-109.2M
phase_0db
phase_margin
ugbw
Results
SENS-0 9/9
HSV-1 error
SIM-3 1/1
HSV-0 error
PVTMC-0 1299/1299
HSMC-2 4000/4000
HSMC-1 4000/4000
FPVT-0 630/630
HSMC-0 7410/7410
SPVT-0 308/308
Selected 0
complete
8:02s
100%


Solido Liberty Explorer@mmarsh
Hierarchy
Filter
ocv_sigma_fall_transition(timing_...
ocv_sigma_fall_transition(timing_...
rise_transition(timing_template_...
ocv_sigma_rise_transition(timing...
ocv_sigma_rise_transition(timing...
output_current_fall() (56)
vector(ccs_template_1x1x33)
vector(ccs_template_1x1x24)
vector(ccs_template_1x1x20)
vector(ccs_template_1x1x19)
vector(ccs_template_1x1x18)
vector(ccs_template_1x1x17)
vector(ccs_template_1x1x16)
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vector(ccs_template_1x1x22)
vector(ccs_template_1x1x18)
vector(ccs_template_1x1x30)
vector(ccs_template_1x1x21)
vector(ccs_template_1x1x19)
vector(ccs_template_1x1x23)
vector(ccs_template_1x1x22)
vector(ccs_template_1x1x16)
Index Navigator
Differences
Trends
X-axis: voltage
Color variable: temperature
output_current_fall
(x=245.3m, y=-371.3m)
current
Time
temperature
#125#1.075#tt (A)
vector(ccs_template_1x1x32) - vector
(x=70.93m, y=-24.20m)
vector
0.039954
-1e-09
0.0463518
-0.17446
Corners
temp
voltage
process
A 0 0.54 tt
A 125 0.54 tt
A 0 0.59 tt
A -30 0.64 tt
A 125 0.64 tt
A -30 0.7 tt
A 125 0.7 tt
A -30 0.745 tt
A 0 0.745 tt
A 125 0.745 tt
A 125 0.775 tt
A -30 0.795 tt
A 125 0.795 tt
A 125 0.825 tt
A 125 0.86 tt
A 125 0.88 tt
A 125 0.945 tt
A -30 1.075 tt
A 0 1.075 tt
A 125 1.075 tt
Selected Group Information
cell(cell_1)
pin(clk)
direction: output;
output_voltage: default;
timing()
related_pin: "clk_in";
timing_sense: positive_unate;
timing_type: combinational;
when: "A&B";
wave_fall: ('6', '15', '6');
wave_rise: ('6', '15');
output_current_fall()
vector(ccs_template_1x1x16)

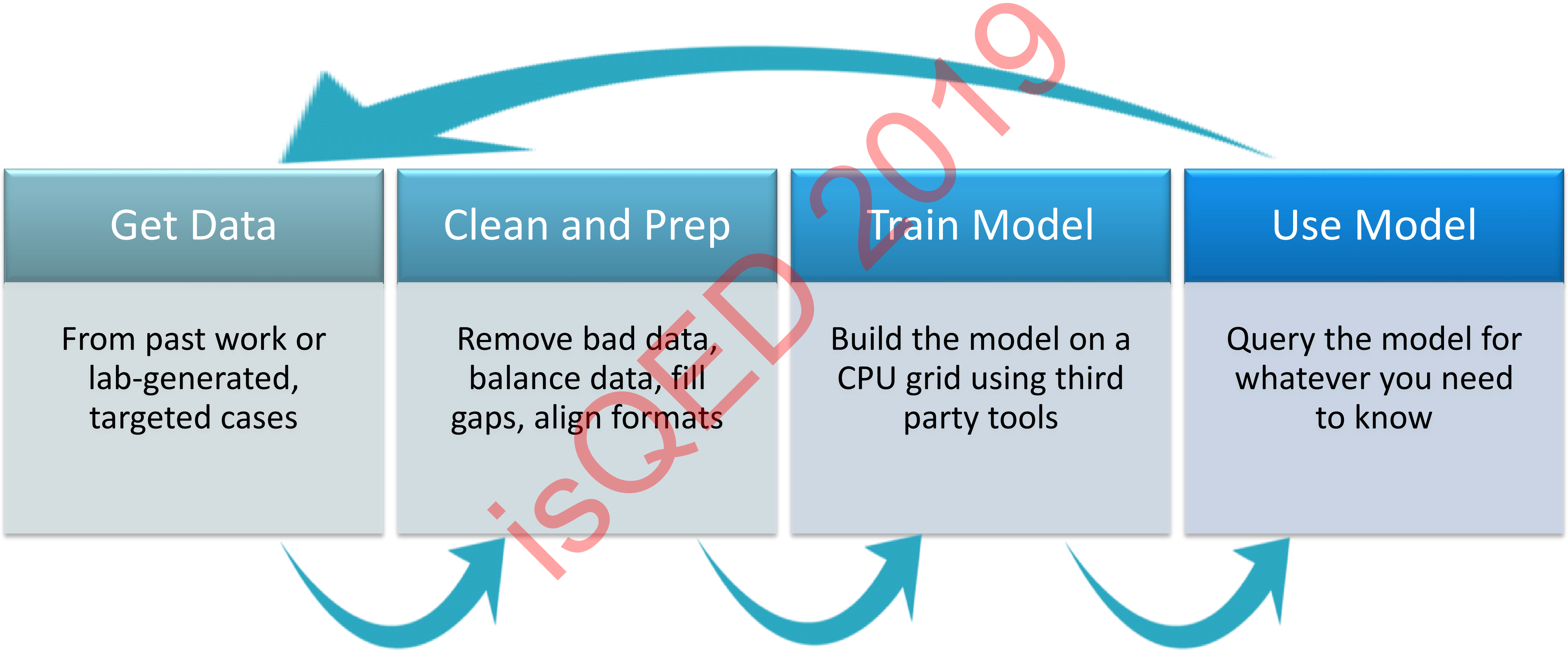
Use ML For High Value Problems

- Accelerate time-to-market by months
- Eliminate person years of engineering time
- Improve performance, area, and power by 20%

- Be general; apply to many circuit types, process techs, CAD flows, and companies

Machine Learning

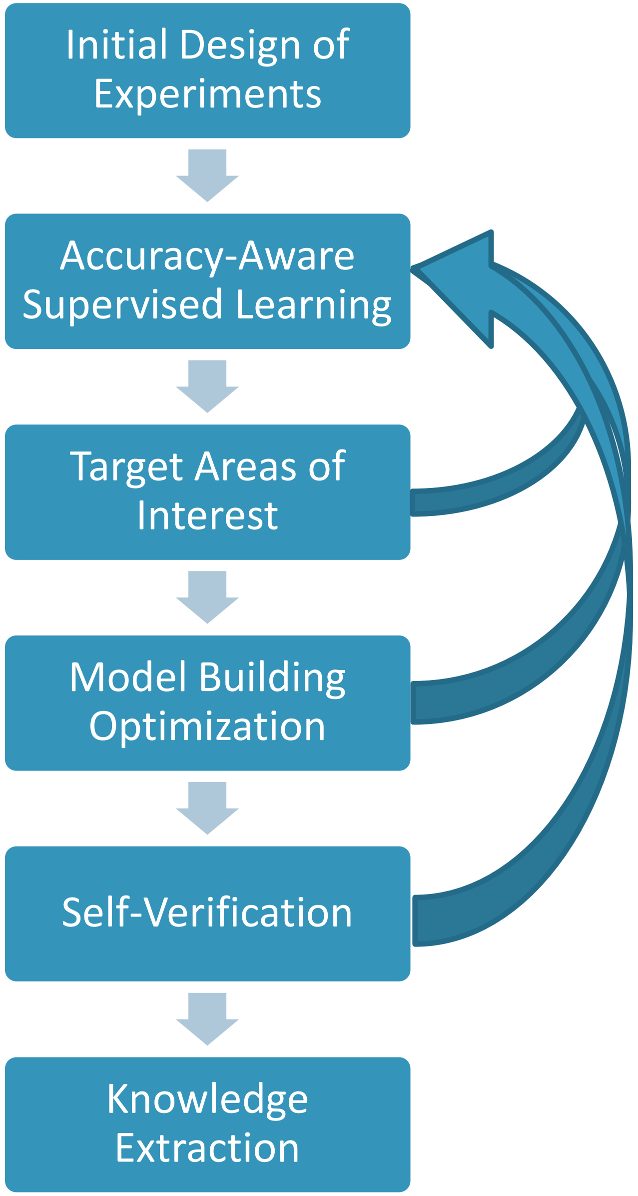
(Traditional train the model / use the model interpretation)



Limitations

(Traditional train the model / use the model interpretation)

- Deals poorly with things that are different than training data
  - Like a new chip on a new process!
- No way to improve accuracy on the fly
  - Chip design has accuracy tolerances!
- Does not dynamically target regions of interest
  - Chip design requires high accuracy in certain areas!
- Iterations are time consuming
  - Chip schedules don't wait!
- **Often fails to solve chip problems due to accuracy and schedule**



Adaptive ML With Data Acquisition In The Loop

- Learns about the subject on the fly
  - E.g. a new chip on a new process
- Targets areas of interest
  - Worst case PVTs, tails of MC distributions
  - Temperature inversions, low-voltage drop-offs
- Improves accuracy dynamically
  - E.g. can achieve < 2% or 2 ps on a standard cell rise delay
- **Solves way more chip design challenges than "train the model/use the model" ML**

Main Requirement for Adaptive ML

Real-time data acquisition capability

E.g. SPICE simulator that can be driven

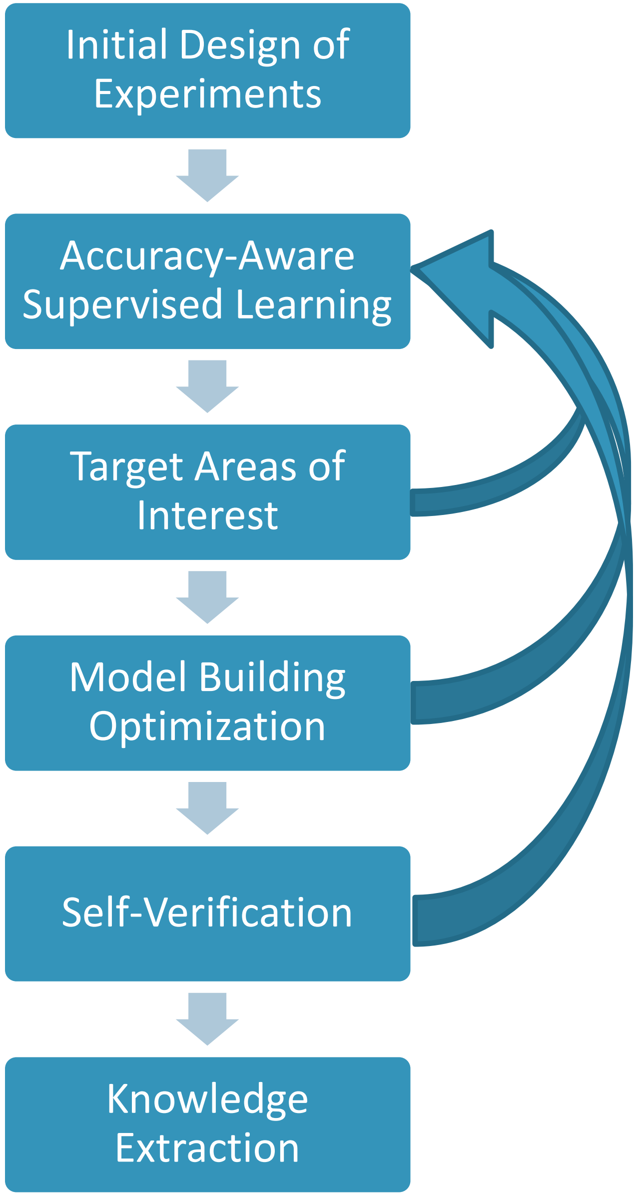
Some creativity

Case Study 1: Fast PVT

- Challenge: Reduce SPICE corner simulations
  ...and still get the right answer ;)
- E.g.:
  Process (5): TT, FF, SS, SF, FS
  Temp (4): -40, 25, 100, 150
  Vdd (8): 0.45, 0.52, 0.58, 0.65, 0.78, 0.9, 1.1, 1.4
  Extraction condition (3): best, worst, typical
  5 * 4 * 8 * 3 = 480 combinations
- **Goal: Full coverage with far fewer than 480 simulations**

PVT Brute-Force Solution

For every PVT combination, simulate in SPICE



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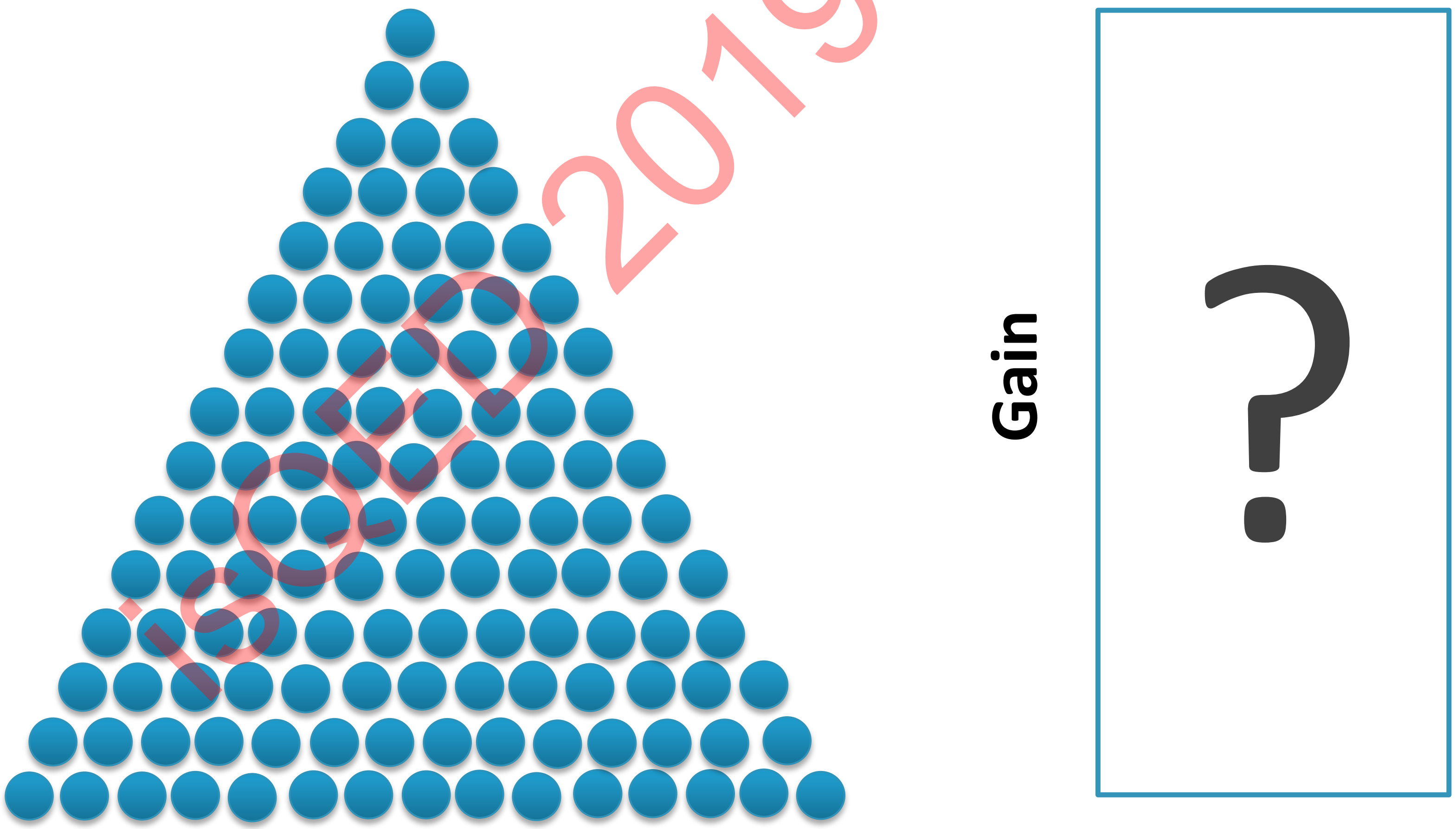
Basic Fast PVT Example: Initial Design of Experiments

- **Initial Design of Experiments**
- Accuracy-Aware Supervised Learning
- Target Areas of Interest
- Model Building Optimization
- Self-Verification
- Knowledge Extraction



Initial Design of Experiments

Accuracy-Aware Supervised Learning

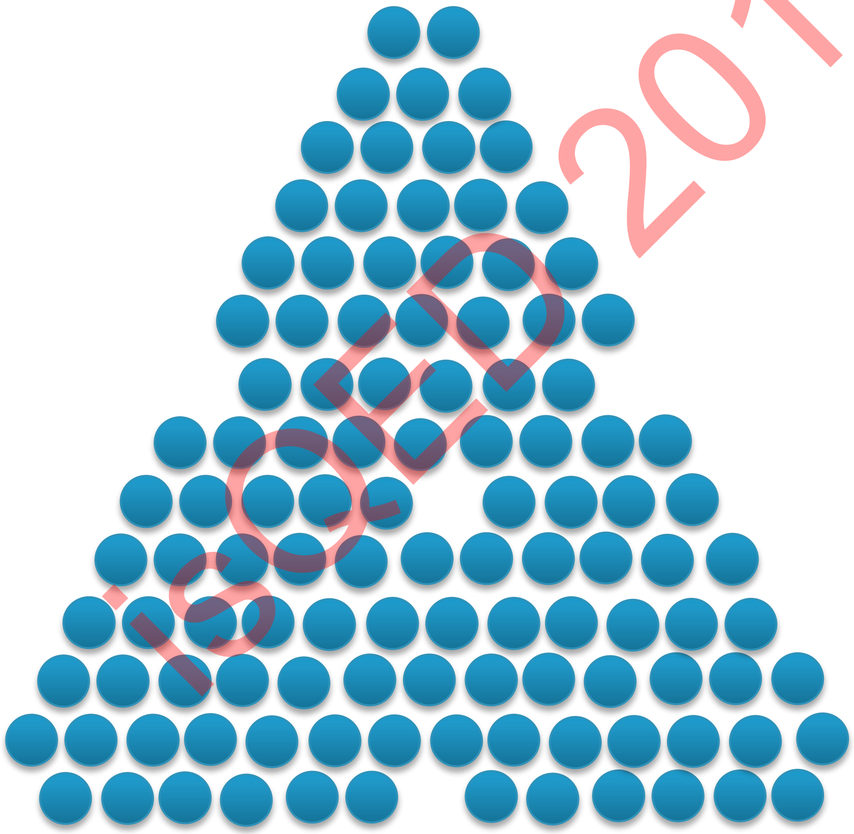
Target Areas of Interest

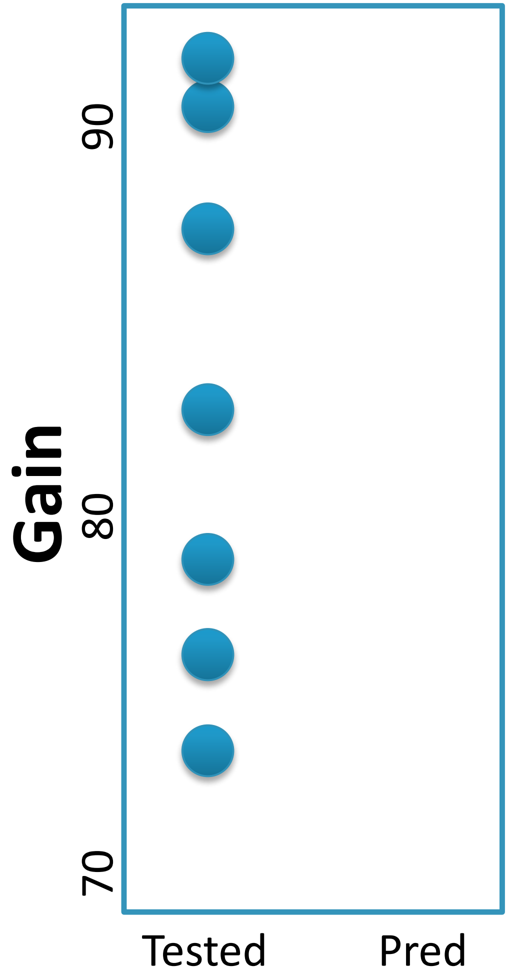
Model Building Optimization

Self-Verification

Knowledge Extraction

Basic Fast PVT Example: Initial Design of Experiments





Initial Design of Experiments

Accuracy-Aware Supervised Learning

Target Areas of Interest

Model Building Optimization

Self-Verification

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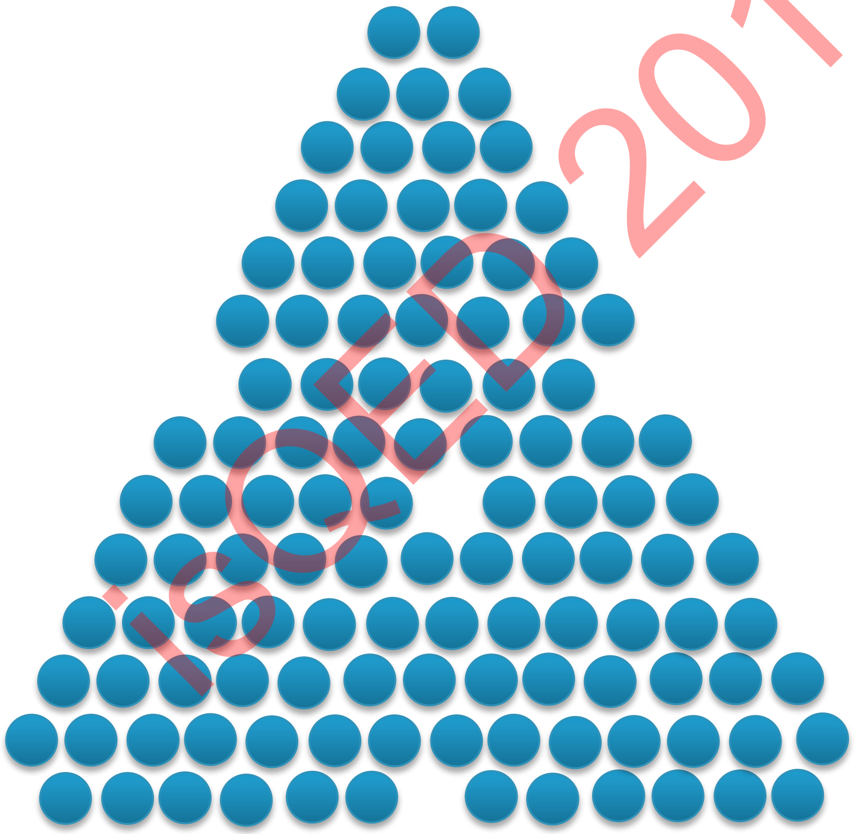
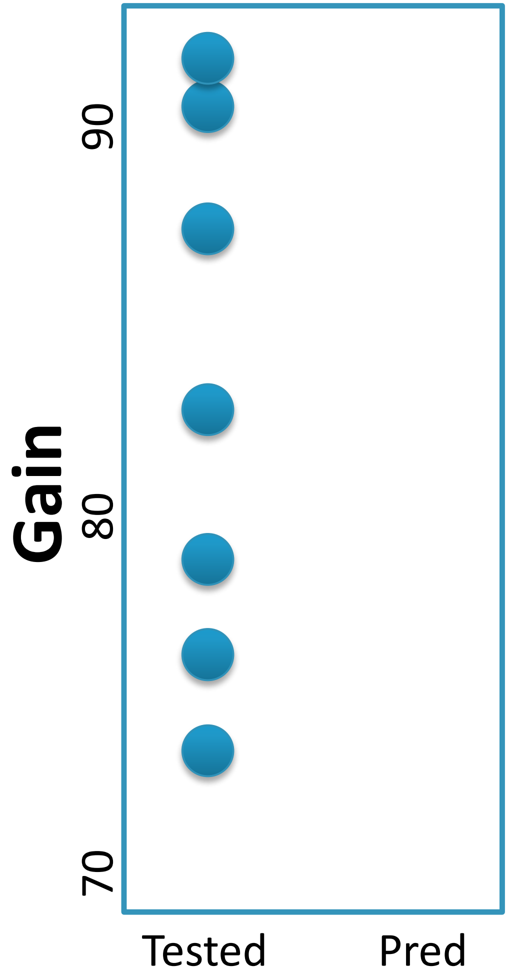
Basic Fast PVT Example: Accuracy-Aware Supervised Learning





Initial Design of Experiments

Accuracy-Aware Supervised Learning

Target Areas of Interest

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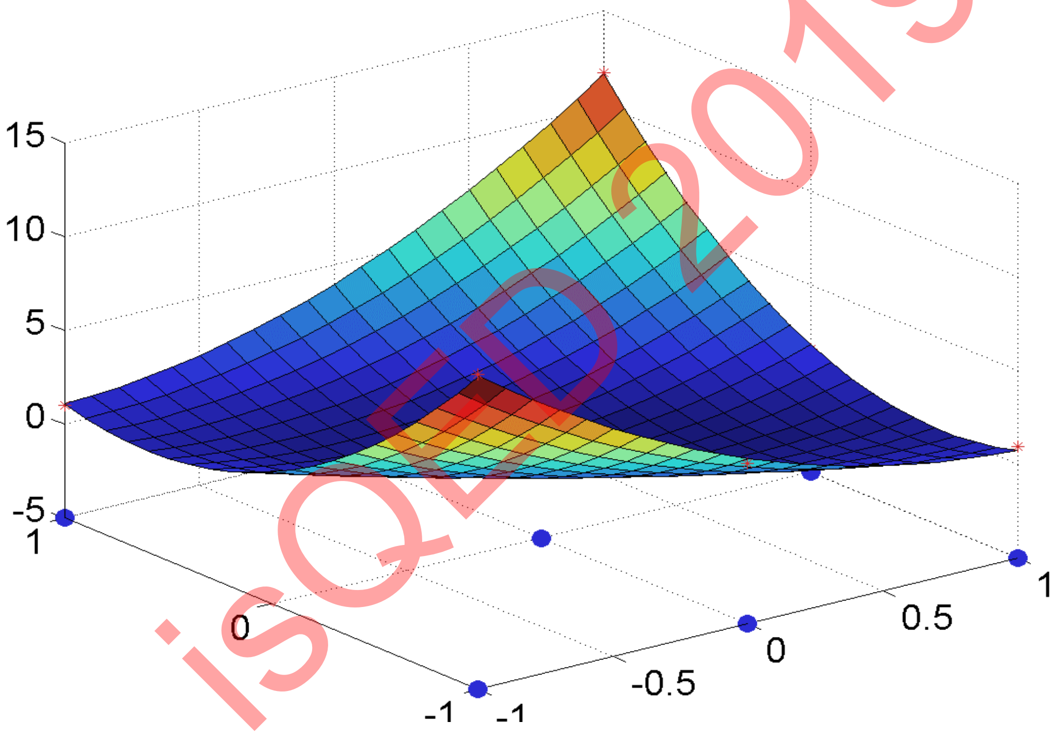
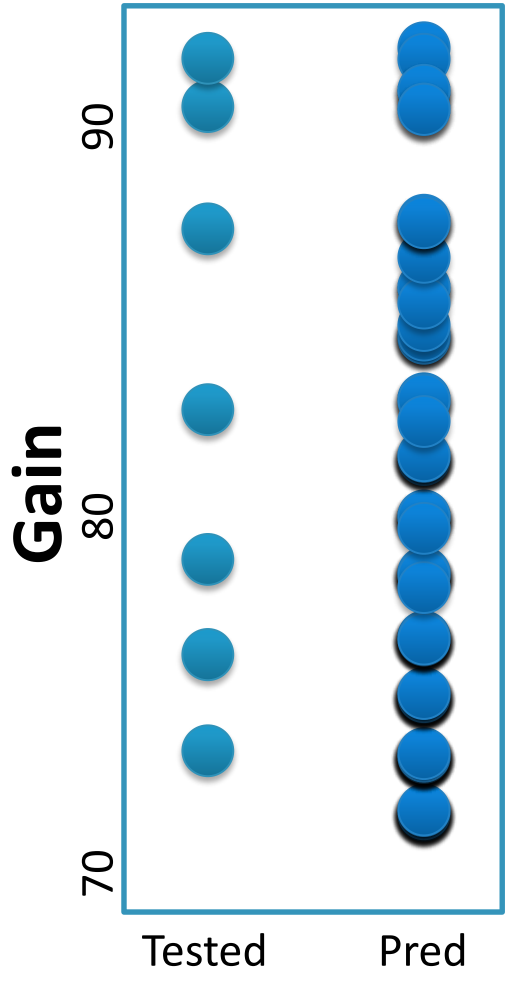
Basic Fast PVT Example: Accuracy-Aware Supervised Learning



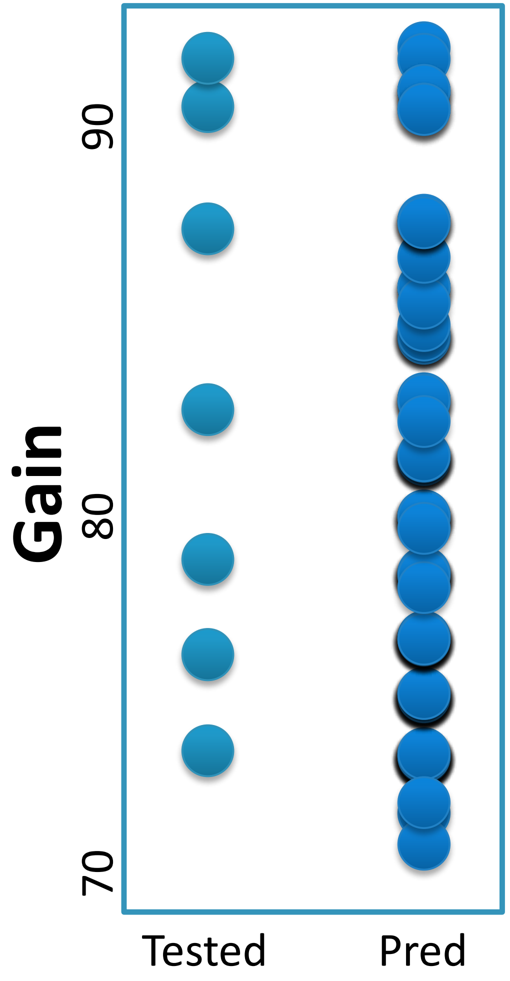


Basic Fast PVT Example: Target Areas of Interest

- Initial Design of Experiments
- Accuracy-Aware Supervised Learning
- **Target Areas of Interest**
- Model Building Optimization
- Self-Verification
- Knowledge Extraction

Goal: Perfect accuracy for worst cases

Simulate those!



Initial Design of Experiments

Accuracy-Aware Supervised Learning

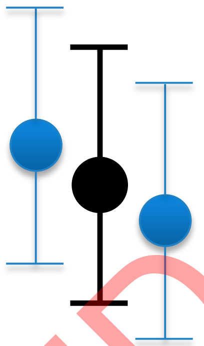
Target Areas of Interest

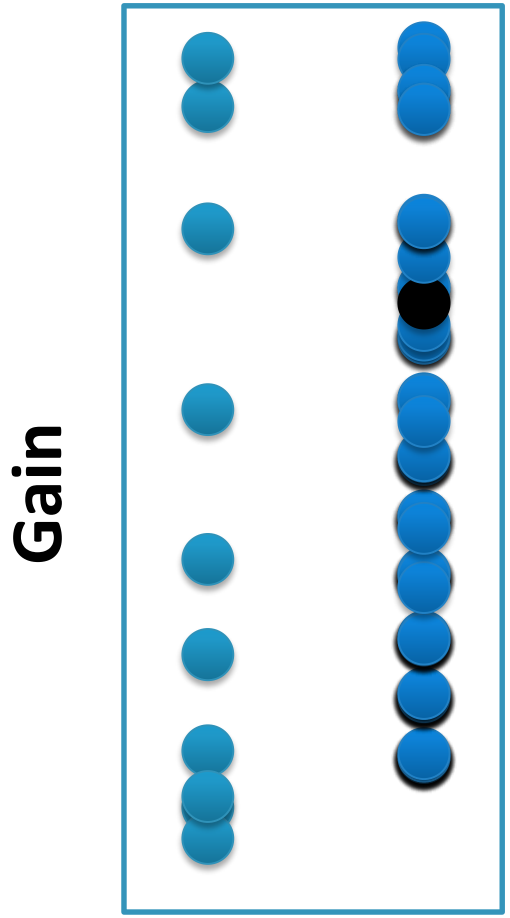
Model Building Optimization

Self-Verification

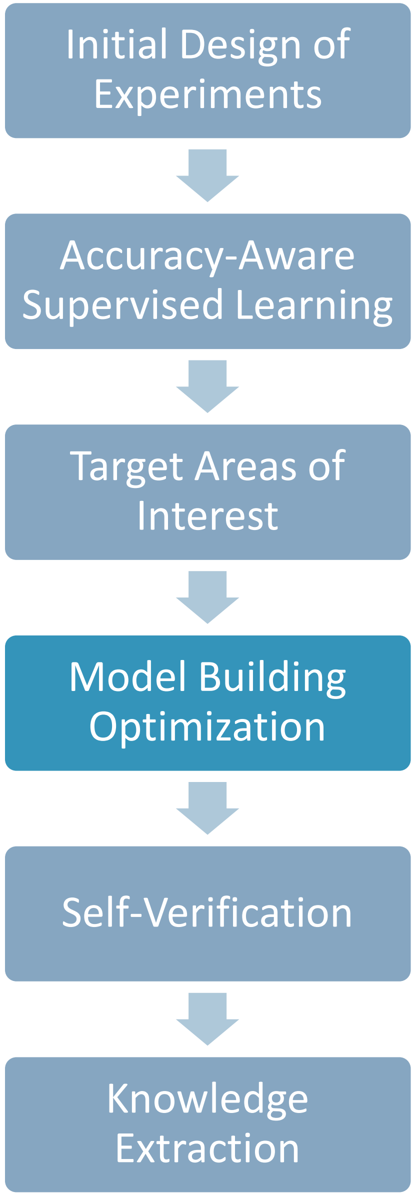
Knowledge Extraction

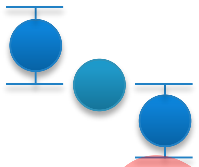
Basic Fast PVT Example: Model Building Optimization

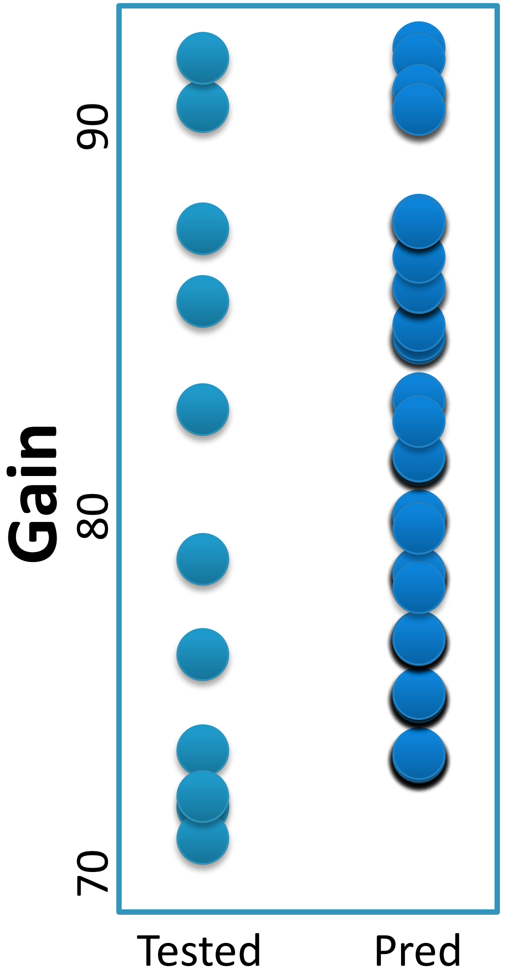




Basic Fast PVT Example: Model Building Optimization

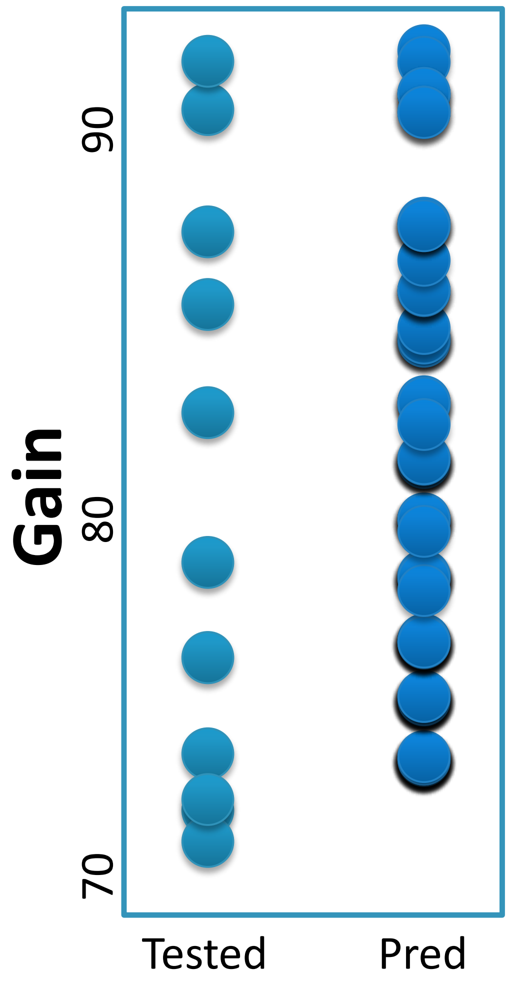






Basic Fast PVT Example: Self-Verification

- Initial Design of Experiments
- Accuracy-Aware Supervised Learning
- Target Areas of Interest
- Model Building Optimization
- **Self-Verification**
- Knowledge Extraction



Initial Design of Experiments

Accuracy-Aware Supervised Learning

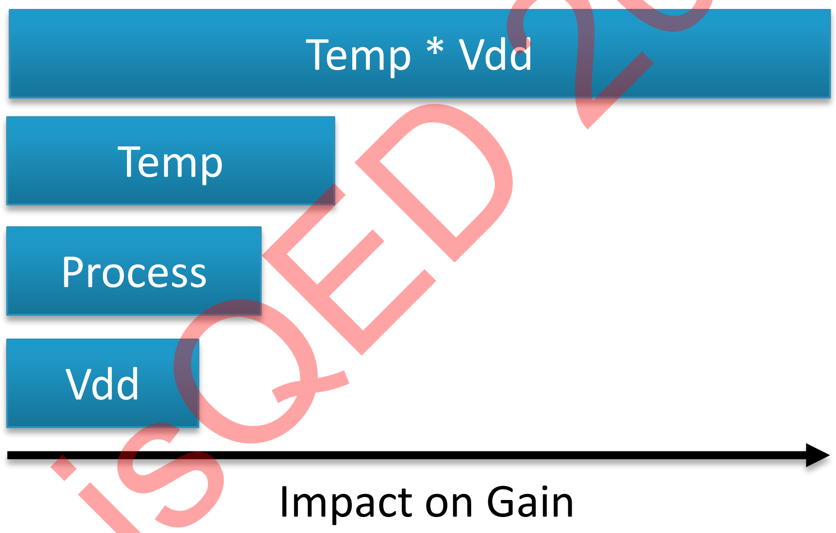
Target Areas of Interest

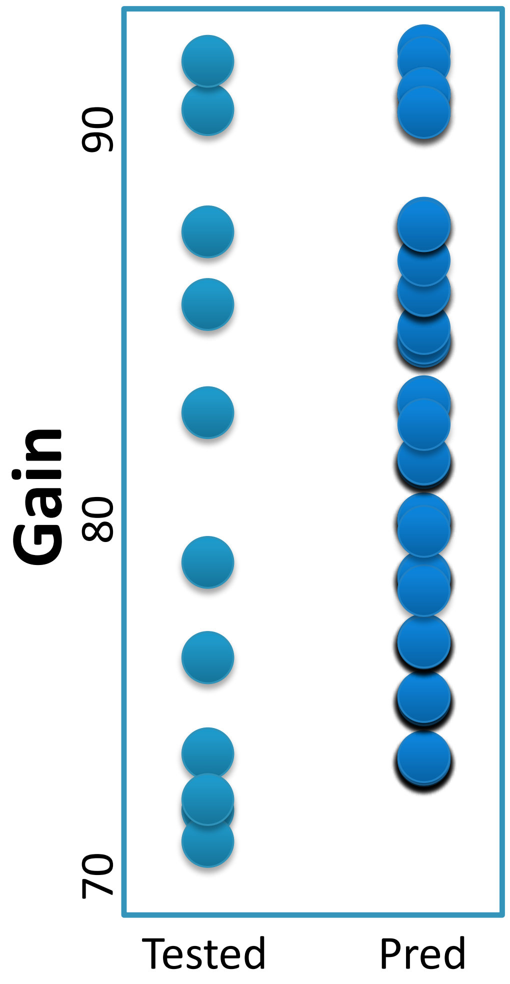
Model Building Optimization

Self-Verification

Knowledge Extraction

Basic Fast PVT Example: Knowledge Extraction





Fast PVT:
Value

- 2-50X faster (more speedups with more corners)
- SPICE-accurate
- Shows cause of problems to help debug

Fast PVT:

More real-world requirements

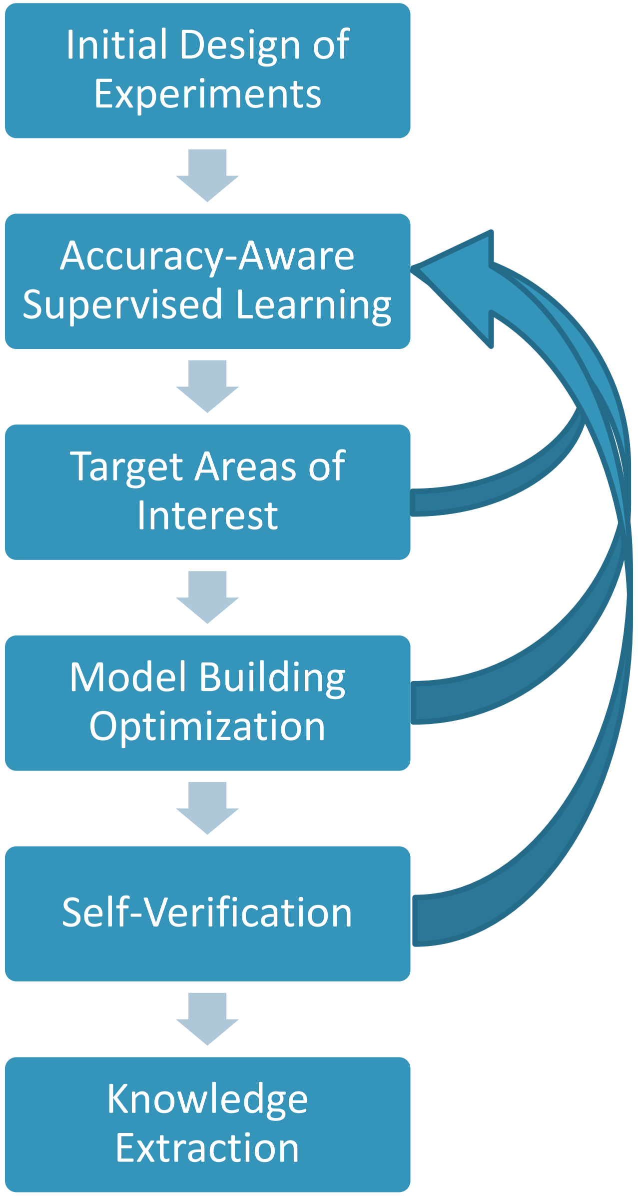
- Lots of outputs (e.g. 100)
- Tricky responses (i.e. n-ary, multi-modal)
- Scale: Variables (e.g. 20) and corners (e.g. 10K)
- Fully utilize cluster resources (e.g. 100 CPUs)
- Recover when SPICE fails
- Differentiate between outliers and errors
- Automatically verify that the answer is right
- No mistakes, ever!

Case study 2: High-Sigma Monte Carlo

- Challenge: Monte Carlo and SPICE accurate high-sigma analysis
  - Need an order of magnitude more simulations for every 0.5 sigma!
    - 4 sigma: ~1M simulations
    - 4.5 sigma: ~10M simulations
    - 5 sigma: ~100M simulations
    - 5.5 sigma: ~1B simulations
    - 6 sigma: ~10B simulations
- Goal: MC and SPICE accuracy in 1000s of simulations (because that is all we have time for in production flows!)

Brute-Force Solution

Run millions or billions of Monte Carlo samples in SPICE ;)



Generate (don't simulate) millions or billions of MC samples;
Simulate a small, intelligently selected population

Build a model that predicts the order of the samples in output space

Simulate starting from the high-sigma tail, working inward

Run more simulations in areas of uncertainty, if needed
Run simulations to determine full PDF

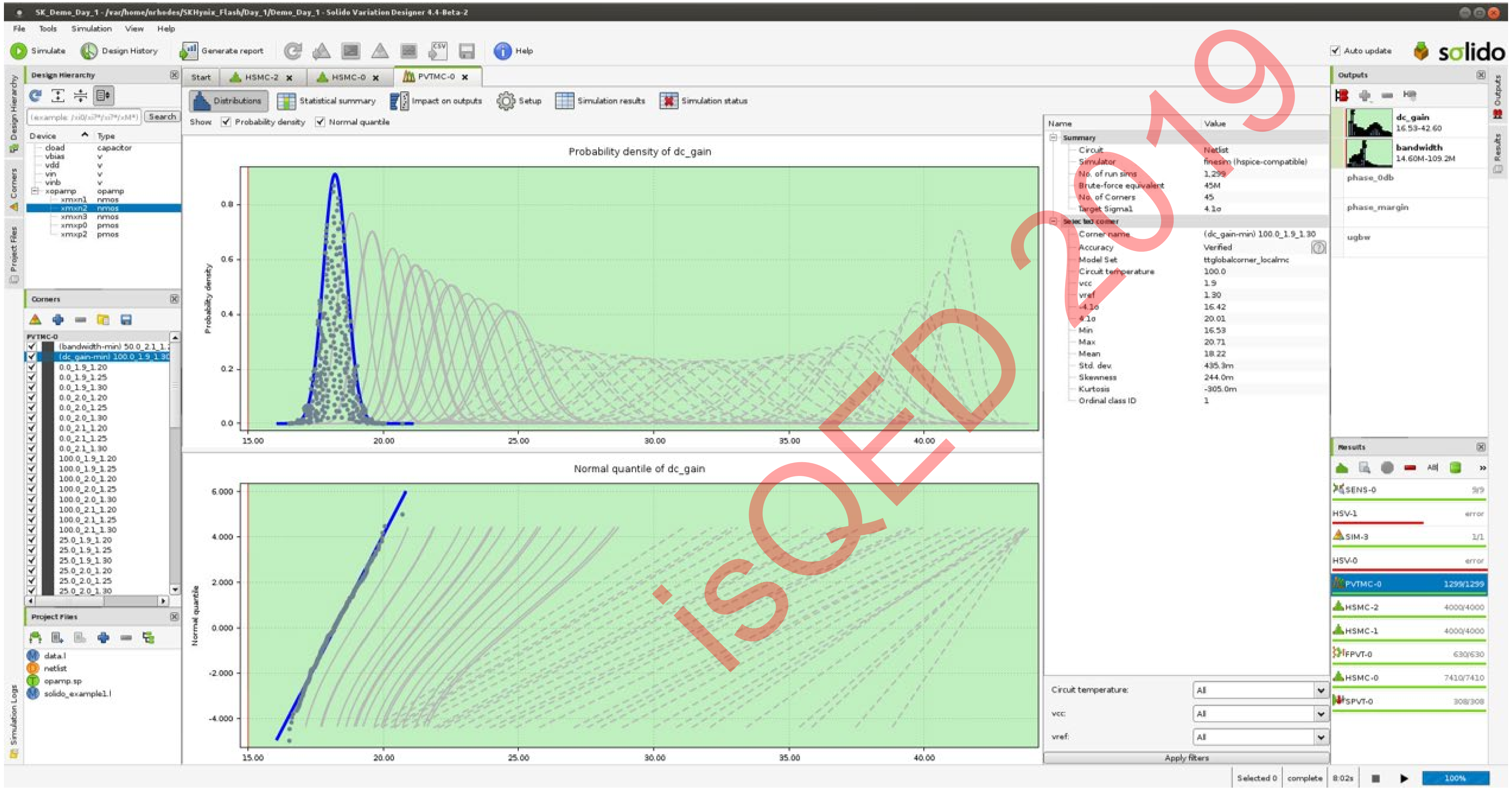
Ensure that predicted order and actual order from SPICE align

Reveal dominant terms in sorting models to show where problem areas are

HSMC: Things That Were Hard

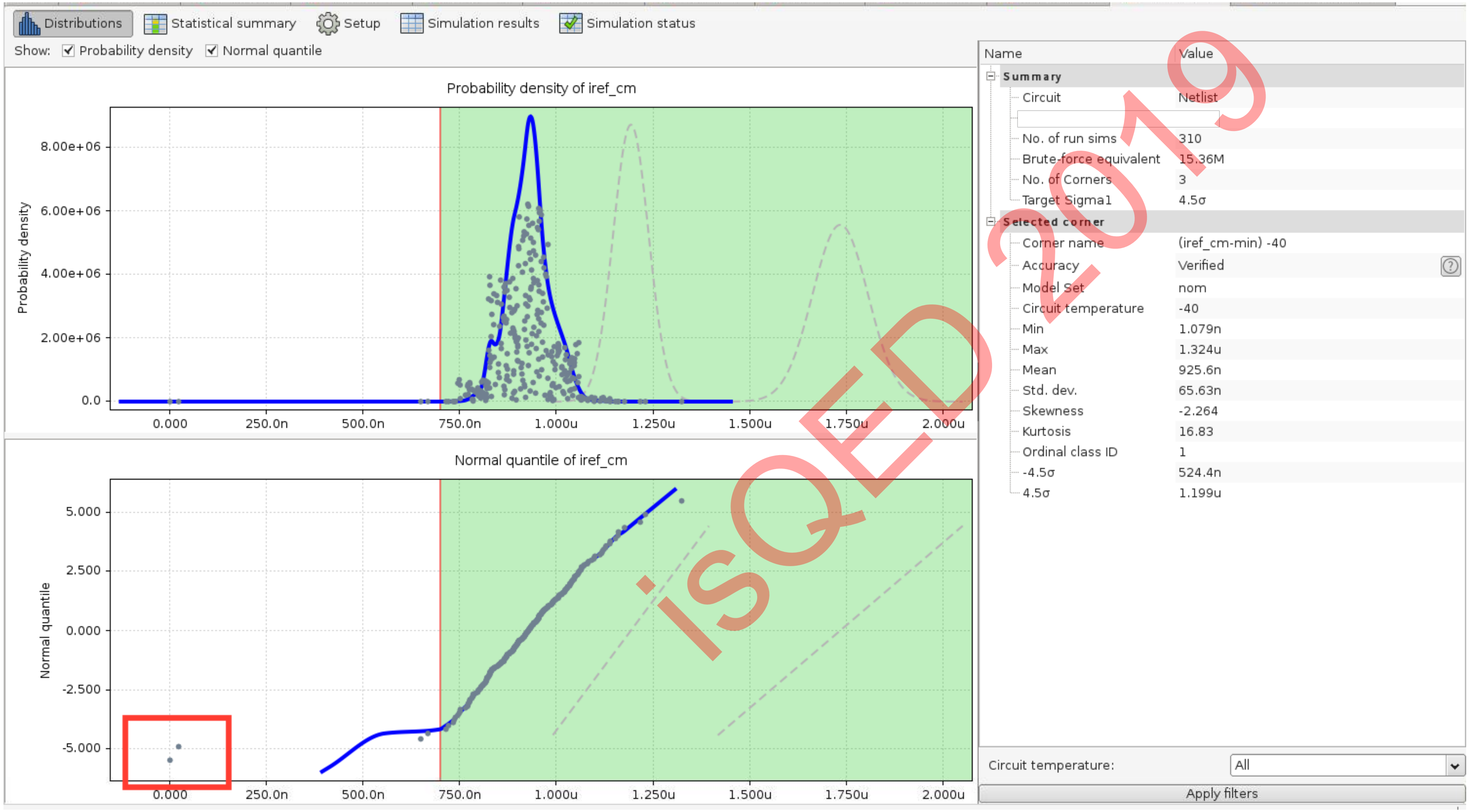
Scaling to 1T samples, 100K process variables
Demonstrating correctness
Corner cases
Binary outputs
Fully adaptive operation
Building trust

PVTMC Verifier Example



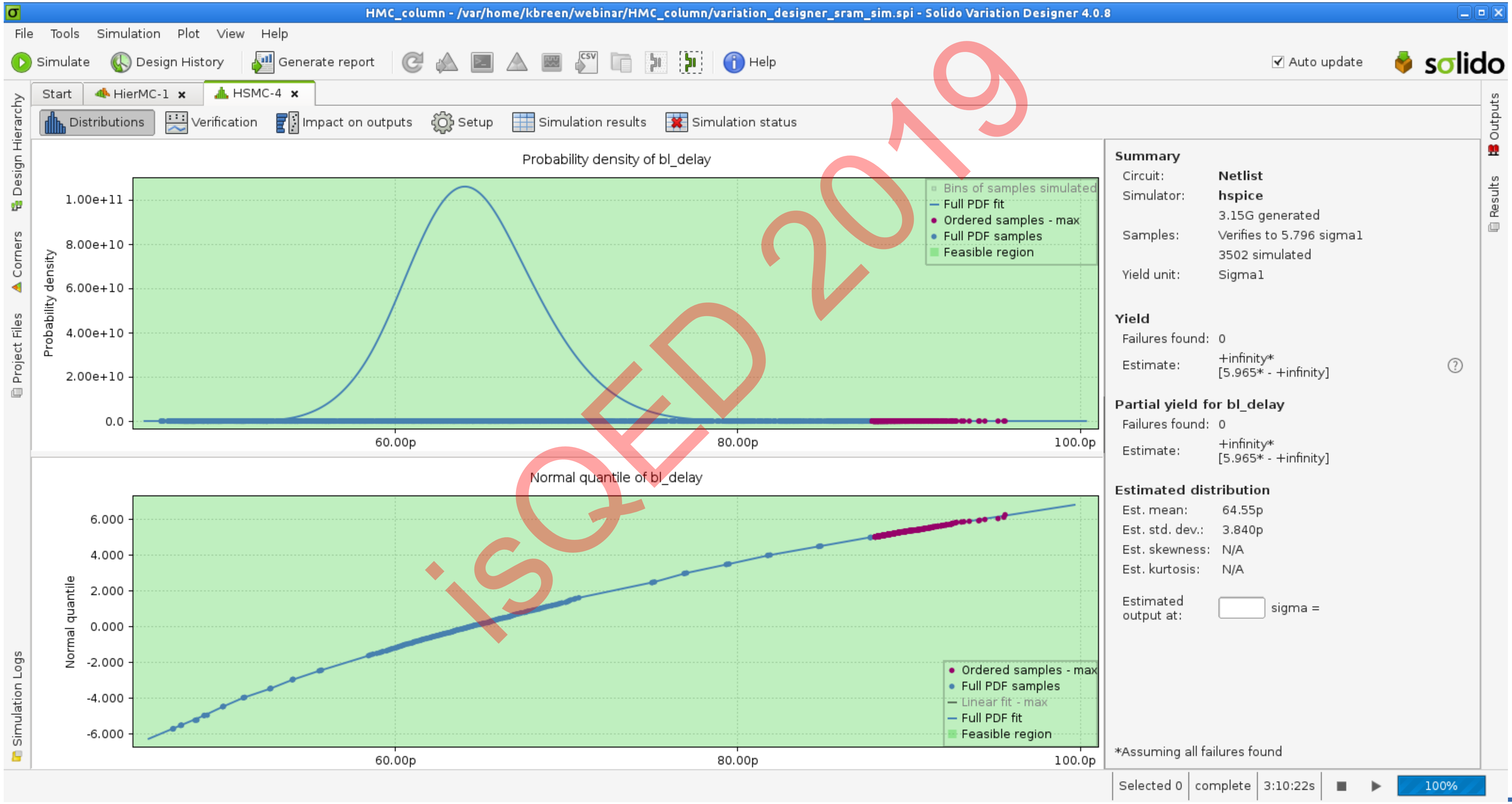
- Verification equivalent to **45M** brute force simulations
- In only **1,299** simulations – fewer than a single Monte Carlo analysis at a single corner
- Full 4-sigma verification across all operating conditions
- **> 30,000x faster**

PVTMC Verifier Example

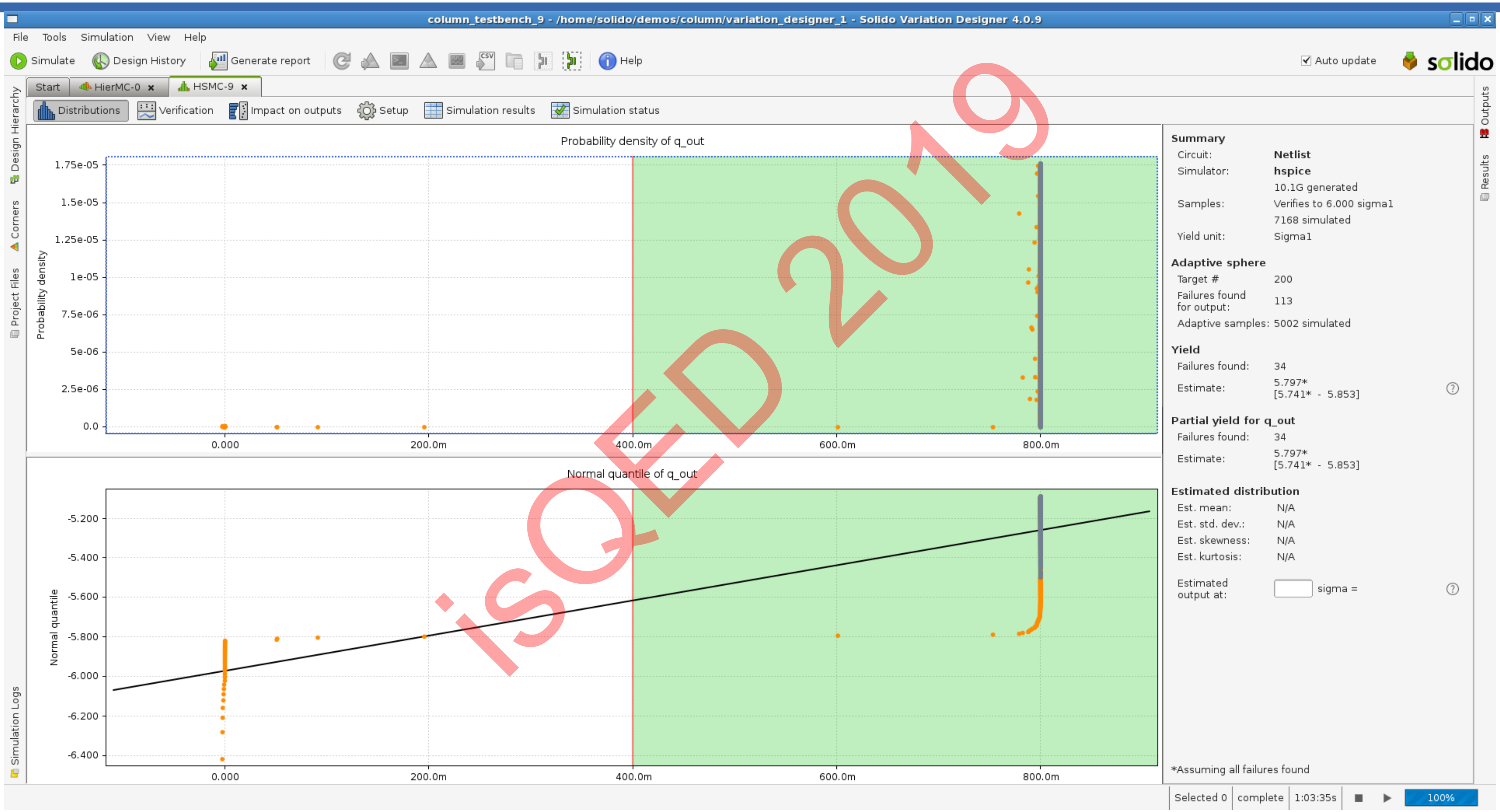


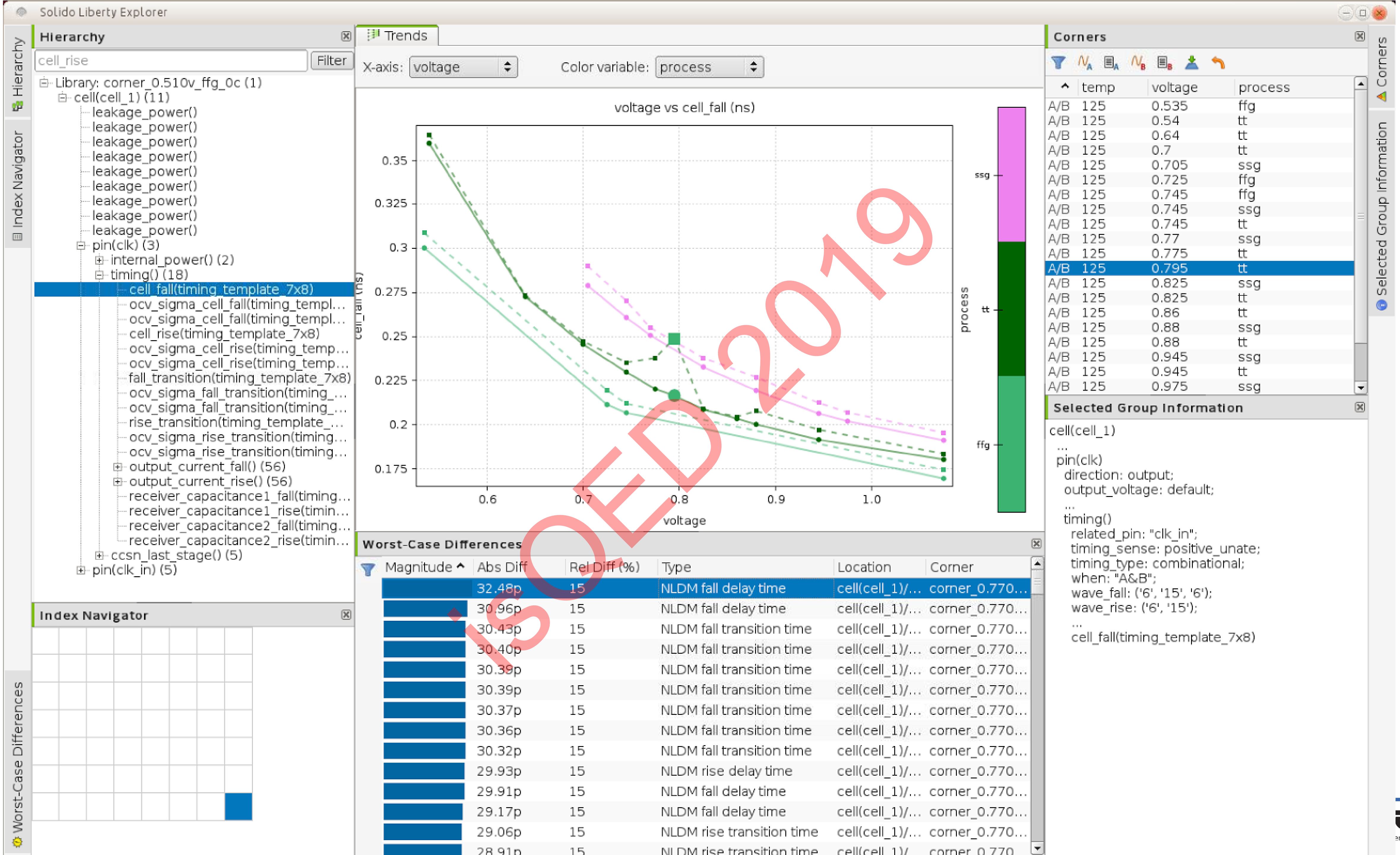
- Verification equivalent to **15.36M** brute force simulations
- In only **310** simulations – fewer than a single Monte Carlo analysis at a single corner
- Full 4.5-sigma verification across all operating conditions
- **> 45,000x faster**

Solido High-Sigma Monte Carlo – bl_delay



Memory – Column – q_out (pass/fail output) – Solido HSMC





Solido Liberty Explorer
Hierarchy
cell_rise
Filter
Library: corner_0.510v_ffg_0c (1)
cell(cell_1) (11)
leakage_power()
pin(clk) (3)
internal_power() (2)
timing() (18)
cell_fall(timing_template_7x8)
ocv_sigma_cell_fall(timing_templ...
cell_rise(timing_template_7x8)
ocv_sigma_cell_rise(timing_temp...
fall_transition(timing_template_7x8)
ocv_sigma_fall_transition(timing_...
rise_transition(timing_template_...
ocv_sigma_rise_transition(timing...
output_current_fall() (56)
output_current_rise() (56)
receiver_capacitance1_fall(timing...
receiver_capacitance1_rise(timin...
receiver_capacitance2_fall(timing...
receiver_capacitance2_rise(timin...
ccsn_last_stage() (5)
pin(clk_in) (5)
Index Navigator
Worst-Case Differences
Trends
X-axis: voltage
Color variable: process
voltage vs cell_fall (ns)
cell_fall (ns)
voltage
process
ssg
tt
ffg
Magnitude
Abs Diff
Rel Diff (%)
Type
Location
Corner
32.48p 15 NLDM fall delay time cell(cell_1)/... corner_0.770...
30.96p 15 NLDM fall delay time cell(cell_1)/... corner_0.770...
30.43p 15 NLDM fall transition time cell(cell_1)/... corner_0.770...
30.40p 15 NLDM fall transition time cell(cell_1)/... corner_0.770...
30.39p 15 NLDM fall transition time cell(cell_1)/... corner_0.770...
30.39p 15 NLDM fall transition time cell(cell_1)/... corner_0.770...
30.37p 15 NLDM fall transition time cell(cell_1)/... corner_0.770...
30.36p 15 NLDM fall transition time cell(cell_1)/... corner_0.770...
30.32p 15 NLDM fall transition time cell(cell_1)/... corner_0.770...
29.93p 15 NLDM rise delay time cell(cell_1)/... corner_0.770...
29.91p 15 NLDM fall delay time cell(cell_1)/... corner_0.770...
29.17p 15 NLDM fall delay time cell(cell_1)/... corner_0.770...
29.06p 15 NLDM rise transition time cell(cell_1)/... corner_0.770...
Corners
temp voltage process
A/B 125 0.535 ffg
A/B 125 0.54 tt
A/B 125 0.64 tt
A/B 125 0.7 tt
A/B 125 0.705 ssg
A/B 125 0.725 ffg
A/B 125 0.745 ffg
A/B 125 0.745 ssg
A/B 125 0.745 tt
A/B 125 0.77 ssg
A/B 125 0.775 tt
A/B 125 0.795 tt
A/B 125 0.825 ssg
A/B 125 0.825 tt
A/B 125 0.86 tt
A/B 125 0.88 ssg
A/B 125 0.88 tt
A/B 125 0.945 ssg
A/B 125 0.945 tt
A/B 125 0.975 ssg
Selected Group Information
cell(cell_1)
pin(clk)
direction: output;
output_voltage: default;
timing()
related_pin: "clk_in";
timing_sense: positive_unate;
timing_type: combinational;
when: "A&B";
wave_fall: ('6', '15', '6');
wave_rise: ('6', '15');
cell_fall(timing_template_7x8)

Adaptive ML For Engineering: Challenges & Solutions

Big, real-time data

- Optimized streaming parsers
- Parallelizable algorithms
- Massively scalable solutions
- Automated recovery and repair
- Big data debugging

Complexity

- Advanced supervised learning
- Big toolbox of modeling technologies
- Smart screening and filtering

Correctness

- Accuracy-aware modeling
- Reinforcement Learning
- Self-verifying algorithms
- Benchmarking Infrastructure

Usability

- Easy for users with little to no ML training
- Make it defensible in design reviews
- Delight users!

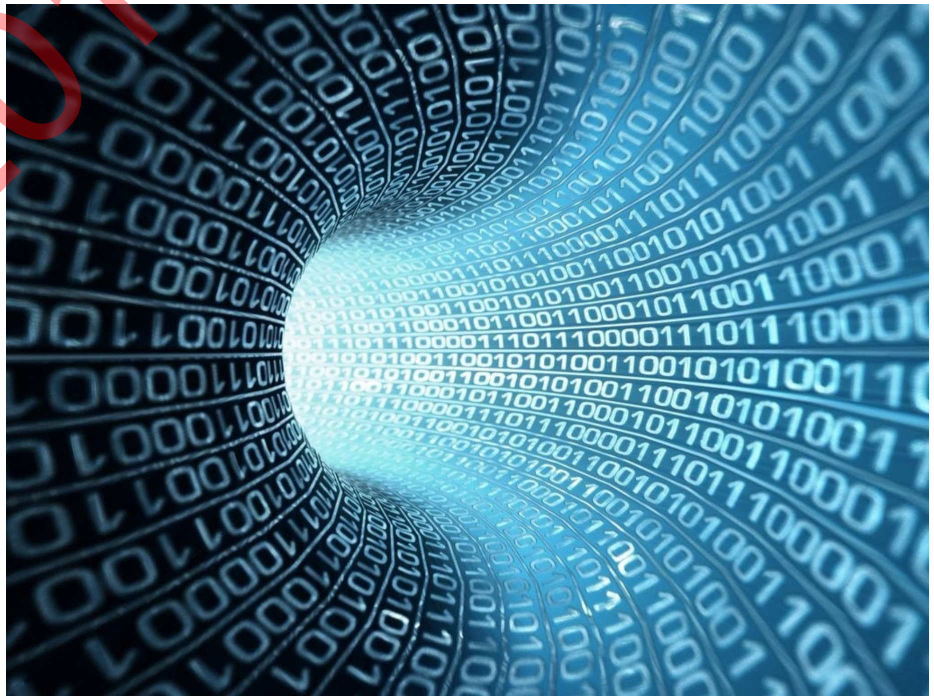
Adaptive ML for Engineering Challenges: Big, real-time data

- **Challenge:**
  - Schedule-driven chip development
  - High streaming data rates and massive data archives

- **Key technologies:**
  - *Optimized streaming parsers*
  - *Parallelizable algorithms*
  - *Efficient and scalable cluster management*
  - *Automated recovery and repair*
  - *Big data debugging*

Adaptive ML for Engineering Challenges: Complexity

- **Challenge:**
  - High dimensionality, high-order interactions, discontinuities, non-linearities



- **Key technologies:**
  - *Design of experiments tech*
  - *Advanced supervised learning*
  - *Intelligent screening and filtering*
  - *Outstanding benchmarking infrastructure*
  - *Big toolbox with lots of experience with tools*

Adaptive ML for Engineering Challenges: Correctness

- **Challenge:**
  - Engineering problems require the *right* answer

- **Key technologies:**
  - *Accuracy-aware modeling*
  - *Reinforcement learning*
  - *Self-verifying algorithms*
  - *Extensive internal benchmarking infrastructure*
  - *Customer-side benchmarking infrastructure*

Adaptive ML for Engineering Challenges: Usability

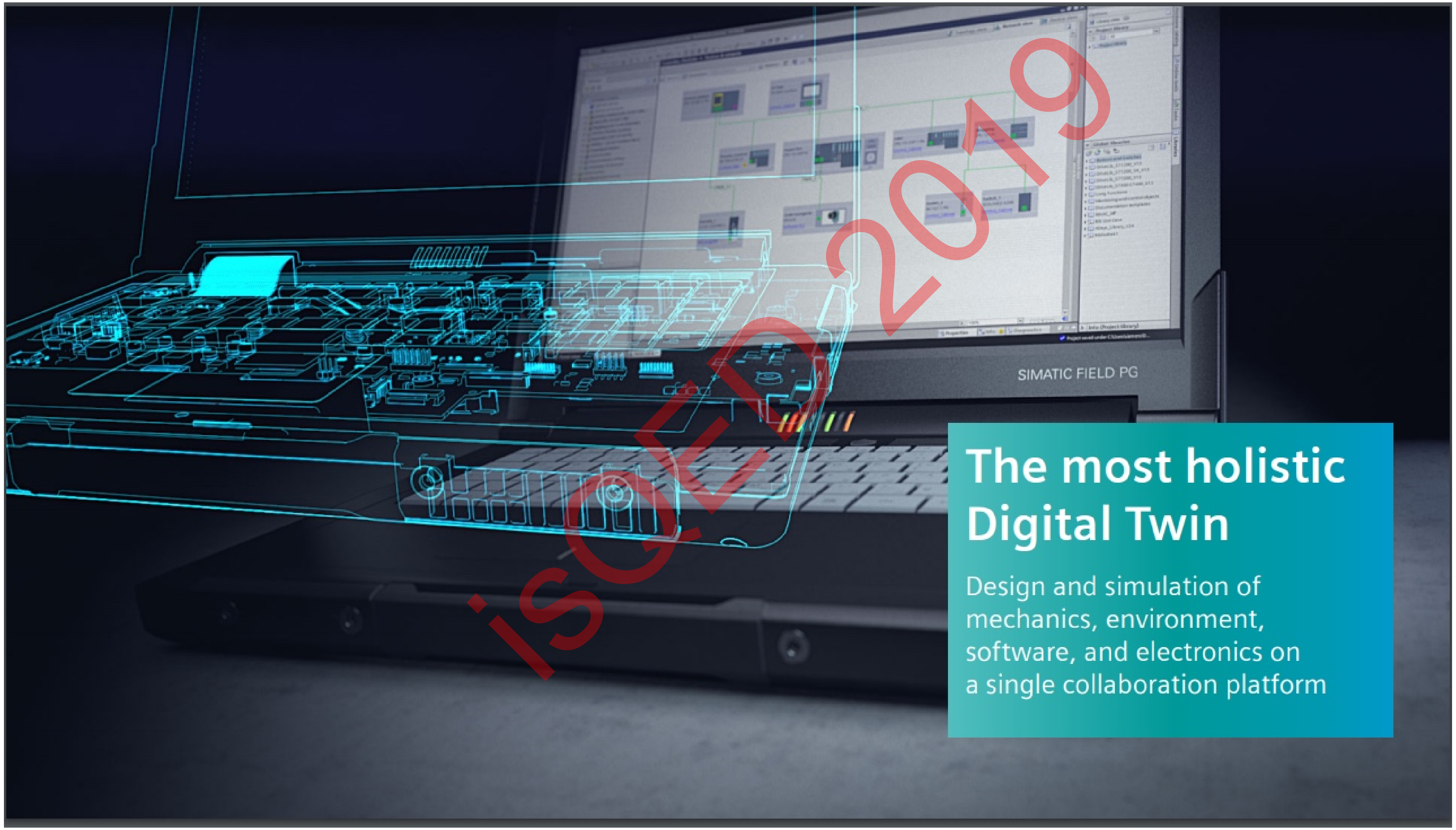
- **Challenge:**
  - Engineers are not ML experts
- **Key technologies:**
  - *Simple configurations that ask users questions they know the answer to*
  - *Adaptive ML algorithms that "do the right thing"*
  - *Results and visualizations that are easy to understand and defend*
  - *Actionable and automated knowledge extraction with intuitive visualizations*

Some other Machine Learning acceleration opportunities in EDA

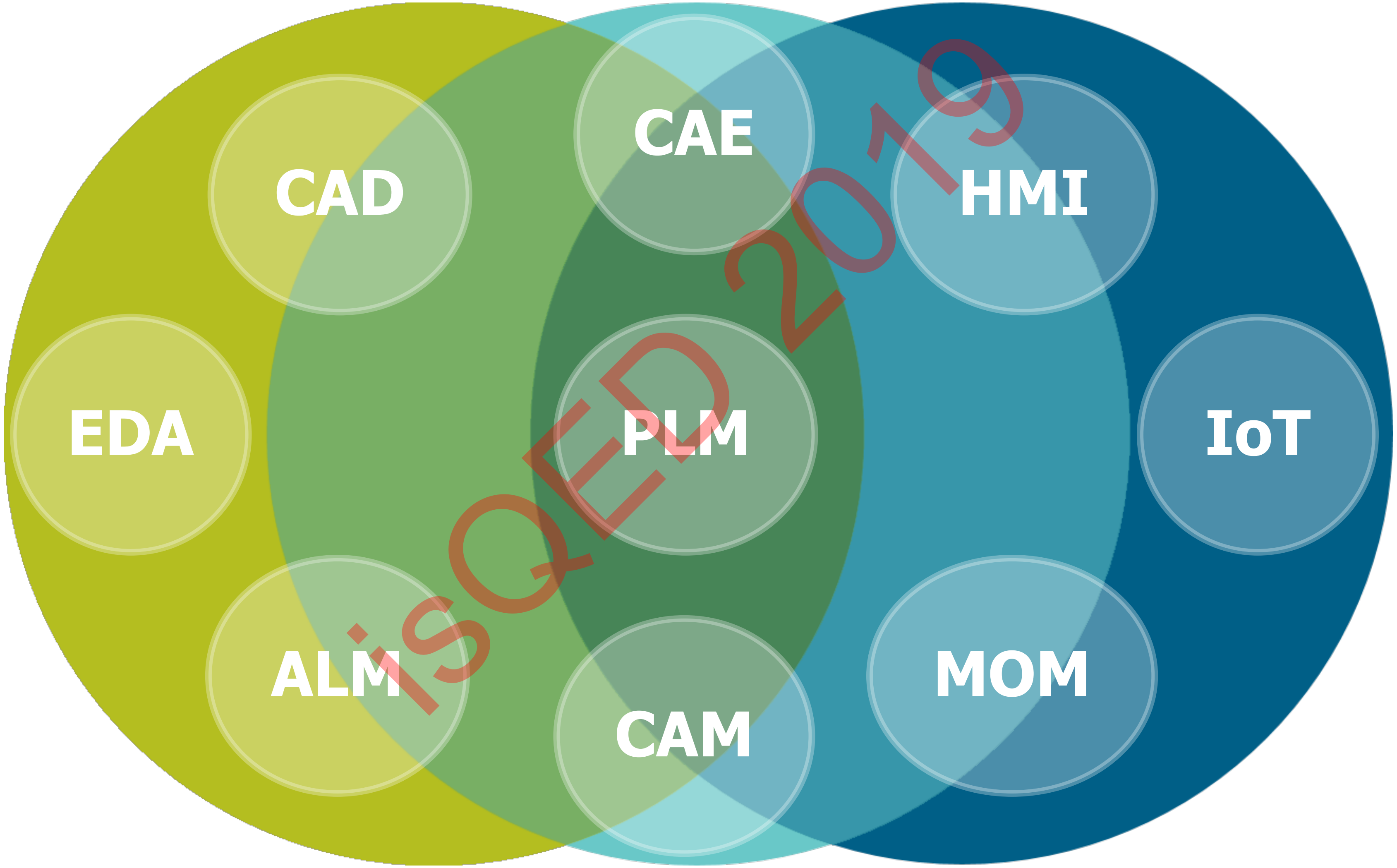
- SPICE Simulation
- Digital Simulation
- Extraction
- Behavioral modeling
- Equivalence checking
- Place & Route
- Design Rule Checking

- Ref: Center for Advanced Electronics Through Machine Learning

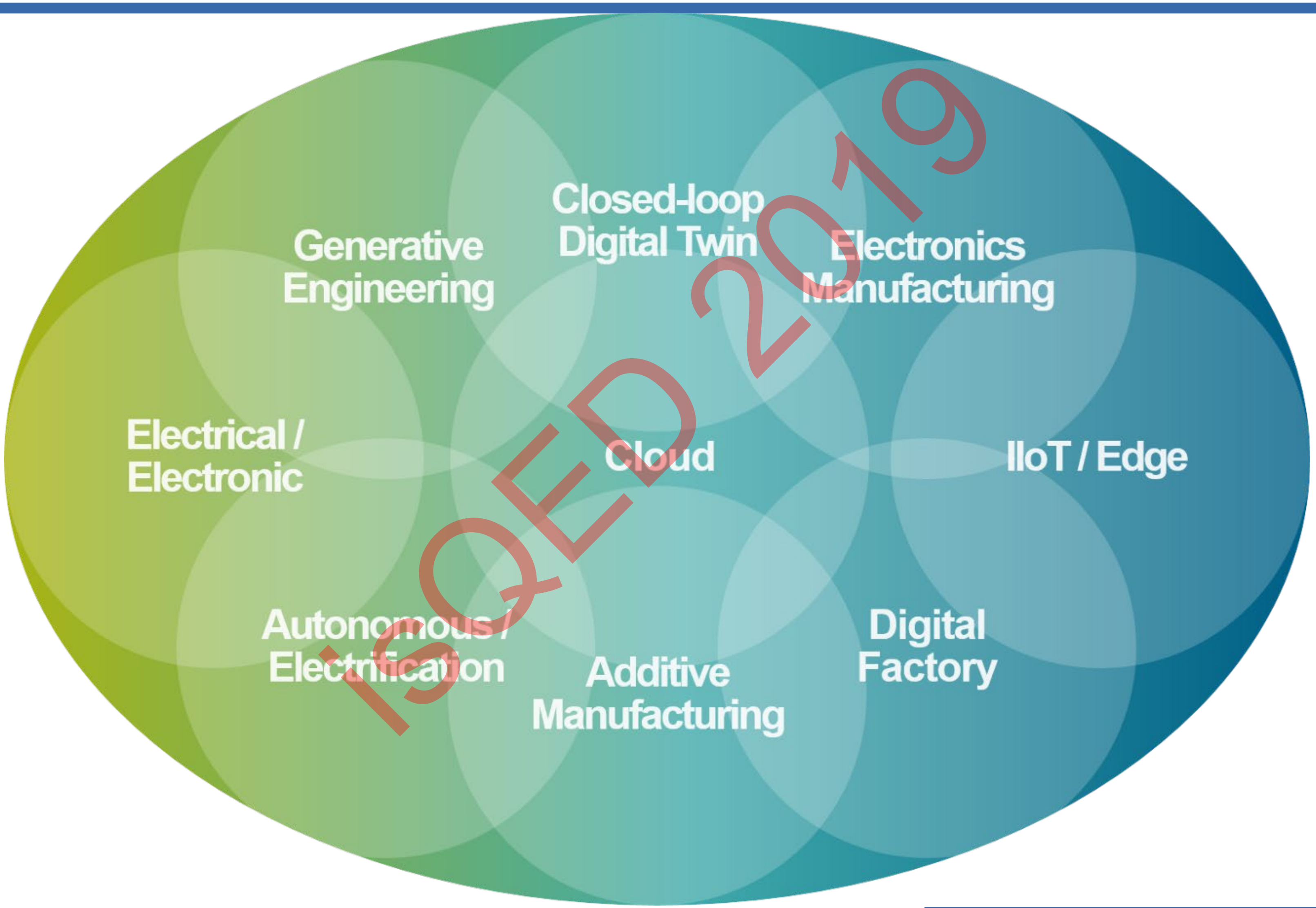
Siemens Vision – The Digital Twin



The old rigid labels are dissolving



Merging into new, disruptive solutions



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