Final Program

AI/ML & Electronic Design, Security, IoT, Autonomous Vehicles, Quantum Computing

25 YEARS ANNIVERSARY

ISQED

2024
25th International Symposium on

QUALITY ELECTRONIC DESIGN

April 3-5, 2024
Seven Hills Conference Center
San Francisco State University
San Francisco, CA US

IEEE Electron Devices Society CAS ISQED www.ISQED.com Since 1999

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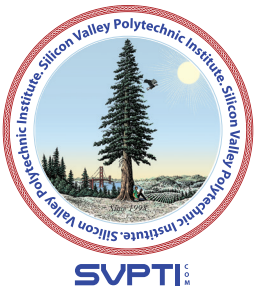

ISQED'24 is produced and sponsored by the
International Society for Quality Electronic Design

WELCOME TO ISQED'24

It is with great enthusiasm that we, on behalf of the ISQED conference and technical committees, extend a warm welcome to all attendees of the 25th anniversary of the International Symposium on Quality Electronic Design (ISQED'24). This year, we commemorate a quarter-century of innovation, leadership, and continuous dialogue on the crucial role of Quality Electronic Design (QED) in navigating the complexities of modern semiconductor technologies.

Embracing the spirit of inclusivity and accessibility, ISQED'24 continues to adopt a hybrid format, combining the best of in-person engagement with the flexibility of virtual participation. This approach allows us to convene at the esteemed Seven Hills Conference Center at San Francisco State University, located at 800 Font Blvd, San Francisco, CA 94132, while extending our reach to a global audience.

Over the past 25 years, ISQED has emerged as a vanguard in advocating for QED principles, contributing significantly to the advancement of semiconductor technology design. As we celebrate this landmark anniversary, ISQED'24 is dedicated to furthering this legacy, offering an expansive program featuring keynotes, panels, tutorials, and more than 100 peer-reviewed papers that echo our commitment to excellence in electronic design.

This year's symposium is supported by the technical sponsorship of esteemed IEEE societies—namely, the Electron Devices Society, and the Circuits and Systems Society—as well as the collaboration with ACM/SigDA. Reflecting our ongoing commitment to scholarly excellence, all conference proceedings and papers will be made available in the IEEE Xplore digital library and indexed by Scopus.

ISQED'24 is tailored to address the pivotal trends that are shaping the future of our industry, including AI/ML, Autonomous Vehicles, Security, IoT, and Quantum Computing. Our curated program encompasses two keynote speeches, embedded tutorials, a panel discussion, and a multitude of peer-reviewed technical papers, spotlighting emerging innovations in electronic circuit and system design, automation, testing, verification, and beyond.

The enthusiasm and quality of submissions for this year's conference have been exceptional, leading to a two and a half-day technical program that features four parallel sessions. Over 100 peer-reviewed papers will be presented, highlighting cutting-edge developments across various domains, including sensors, security, semiconductor technologies, and cyber-physical systems. Adhering to our hybrid format, all technical presentations, plenary sessions, panel discussions, and tutorials will be accessible both in-person and virtually, ensuring a comprehensive and inclusive experience for all participants from April 3-5, Pacific Daylight Time (PDT).

We are profoundly grateful to our corporate sponsors, Innovotek and Silicon Valley Polytechnic Institute, for their generous support, which has been crucial in bringing the vision of ISQED'24 to life. Their contribution not only facilitates this year's conference but also nurtures the future of quality electronic design.

Welcome to ISQED'24—where tradition meets innovation at the crossroads of a shared vision for a future defined by excellence in electronic design.

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ISQED'24 Best Papers

3A.2

Toward Early Stage Dynamic Power Estimation: Exploring Alternative Machine Learning Methods and Simulation Schemes

Philipp Fengler[†], Sani Nassif[†‡], Ulf Schlichtman[*]*

[*]Chair of Electronic Design Automation; [†]Institute for Advanced Study, [‡]Technical University of Munich, Germany

5A.5

Reprogrammable Time-Domain RRAM Based Vector Matrix Multiplier for In-Memory Computing

Bipul Boro, Rushik Parmar, Ashvinikumar Dongre, Gaurav Trivedi

Indian Institute of Technology Guwahati, Assam, India

5B.1

AutoAnnotate: Reinforcement Learning based Code Annotation for High Level Synthesis

Hafsah Shahzad[*],Ahmed Sanaullah[†], Sanjay Arora[†], Uli Drepper[†], Martin Herbordt[*]

[*]ECE Dept., Boston University [+]Red Hat, Inc.

6B.1

EASI-CiM: Event-driven Asynchronous Stream-based Image Classifier with Compute-in-Memory Kernels

Rahul Sreekumar[1], Minseong Park[1], Mohammad Nazmus Sakib[1], Bhupendra Singh Reniwal[2], Kyusang Lee1, Mircea R Stan[1]

[1]University of Virginia, [2]Indian Institute of Technology Jodhpur

Authors of best papers are acknowledged during the morning plenary session on Wednesday April 3.
ISQED'24 best papers are sponsored by Silicon Valley Polytechnic Institute.

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Dimitris Nikolos - University of Patras
Ernesto Sanchez - Politecnico di Torino
Yiorgos Tsiatouhas - University of Ioannina
Miroslav Velev - Aries Design Automation
Arnaud Virazel - LIRMM

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GENERAL INFORMATION
ISQED'24

April 3-5, 2024
Seven Hills Conference Center
San Francisco State University

AWARDS & RECOGNITIONS

Wednesday April 3, 8:40 AM - 9:00 AM
Track A - Nob Hill Room

Best Paper Awards

Recipients of the ISQED'24 Best Paper Awards will be recognized in this segment of the program. The best papers are shown in Page 2 of this document.

Keynotes

Keynote 1P.1

Wednesday, April 3, 9:00 AM - 9:35 AM

Cross-Layer Optimization of Energy Harvesting and Storage

Naehyuck Chang
Executive Vice President, Samsung SDI America

Keynote 1P.2

Wednesday, April 3, 11:45 AM - 12:20 PM

Why we did not have flying cars for 100 years

Jim Dukhovny
CEO, Alef Aeronautics

Panel Discussion

Wednesday, April 3, 3:15 PM - 4:45 PM
Track A - Nob Hill Room

AI Hardware: Opportunities and Challenges

In the contemporary fabric of our civilization, artificial intelligence (AI) has emerged as a pivotal force, permeating various facets of our daily lives. Its significance lies in its ability to augment human capabilities, streamline processes, and catalyze breakthroughs in fields ranging from healthcare to finance. As AI applications become increasingly sophisticated, the importance of dedicated hardware tailored to meet the unique computational demands of these intelligent systems has come to the forefront. The growing complexity of AI algorithms, particularly in the realm of deep learning, necessitates specialized hardware architectures. Such dedicated AI hardware serves as the backbone for processing vast amounts of data and executing intricate calculations with remarkable speed and efficiency. This optimized hardware not only accelerates the training and inference processes but also contributes to the scalability and practicality of AI applications. As AI continues to evolve, researchers are uncovering novel algorithms and models that push the boundaries of what is achievable. In this dynamic landscape, the hardware supporting AI must adapt and innovate to fully realize the potential of emerging technologies. The symbiotic relationship between AI advancements and specialized hardware underscores the critical role that hardware research plays in shaping the trajectory of artificial intelligence, ensuring its seamless integration into the fabric of our technologically driven civilization. Embark on a riveting exploration of AI hardware with our expert panel. Explore the expansive potential of advanced processors and innovative accelerators, dissecting the intricate landscape that defines artificial intelligence hardware. Seasoned experts guide the audience through the dual lens of opportunities and challenges, addressing key facets such as scalability, energy efficiency, and the symbiotic interplay with software. This panel promises a compelling journey into the forefront of AI hardware, where challenges are viewed as gateways to innovation, shaping the future of computational prowess. Join us for a captivating exploration of the evolving landscape at the intersection of hardware technology and artificial intelligence.

Panelists:

Arnab Raha - Intel
Garrett S. Rose - University of Tennessee Knoxville
Akhilesh Jaiswal - University of Wisconsin Madison
Syed Shakib Sarwar - Meta Inc.
Cindy Yi - Virginia Tech

Modedrator & Chair:

Ahmedullah Aziz - University of Tennessee Knoxville

Embedded Tutorials

Chair & Moderators:
Zhen Zhou - Intel (Chair)
Hechen Wang - Intel (Co-Chair)

Track A - Nob Hill Room

Tutorial 1
Wednesday, April 3, 12:25 PM -1:25 PM

Advanced Packaging for Heterogenous Integration

Tolga Acikalin
Intel Labs

.....

Tutorial 2
Thursday April 4, 1:05 PM -2:05 PM

Securing Ubiquitous Devices with Lightweight Circuit Primitives

Prof. Kaiyuan Yang
Rice University

.....

TECHNICAL SESSIONS

There are a total of 20 paper sessions held on Wednesday to Friday. Technical sessions are held in the format of three parallel tracks **A, B, C** located respectively in Nob Hill Room, Russian Hill Room, and Mt. Davidson room.

ON-SITE REGISTRATION

Tentative time schedule of on-site registration is as follows:

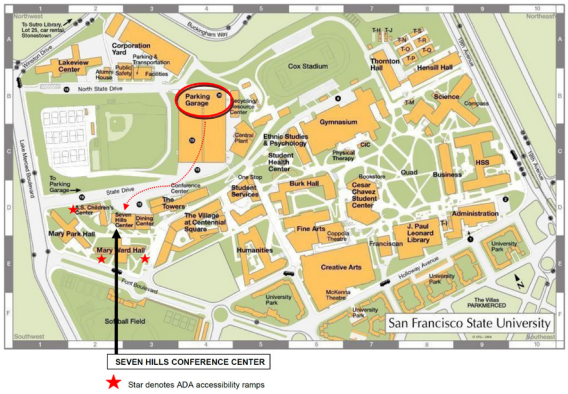
Wednesday, April 3, 8:00 AM - 2:00 PM
Thursday , April 4, 8:00 AM -12:00 PM

Registration desk location will be at the conference center lobby.

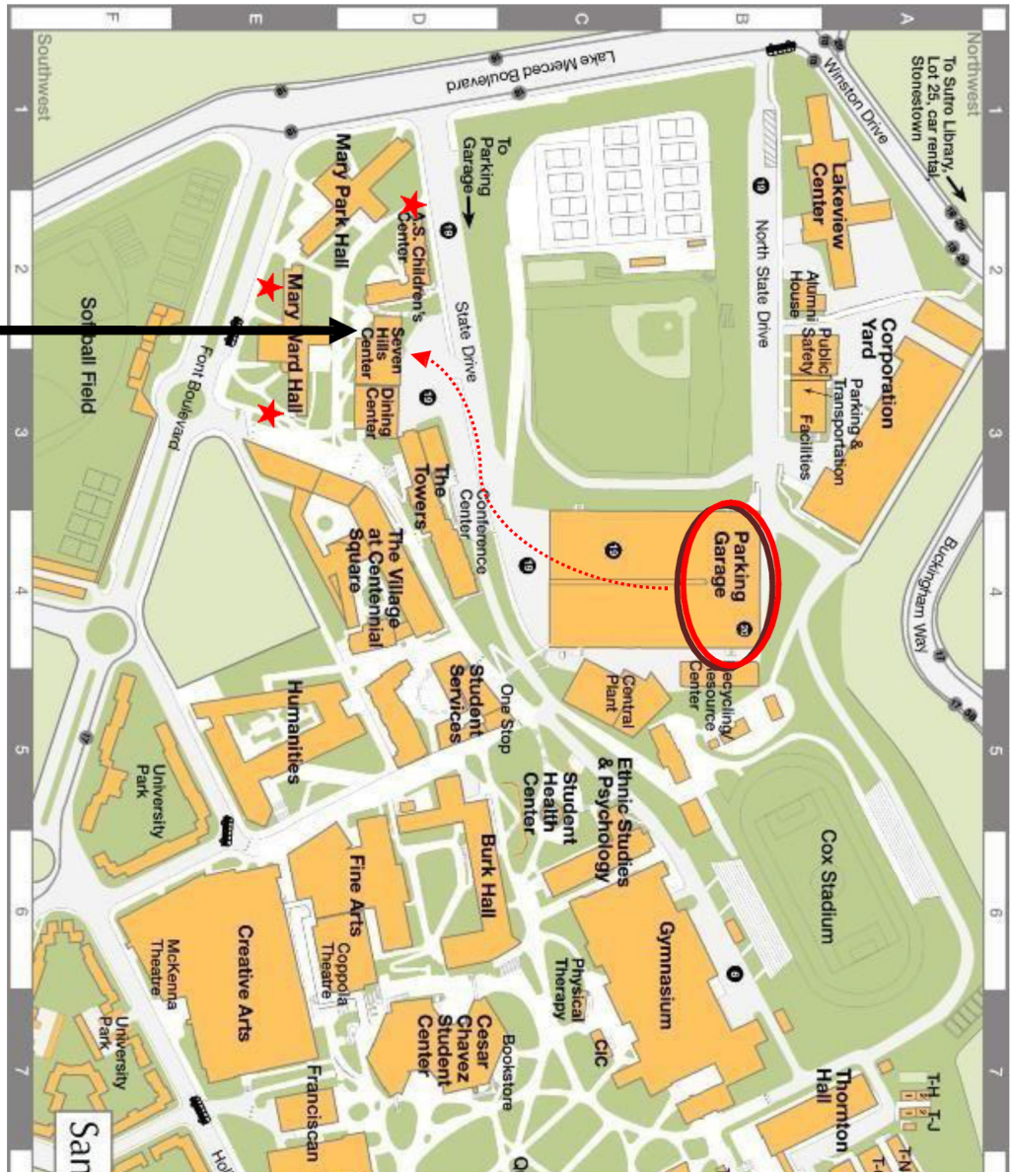
Seven Hills Conference Center

ISQED'24 conference will be held in Seven Hills Conference Center, located in San Francisco State University, 800 Font Blvd, San Francisco, CA 94132.

If you are using navigator the best address to use is: 796 state drive, San Francisco, CA 94132. (Note: make sure to use Google Maps app) At the end of State Drive is the Public Parking Lot ("Lot 20"). Parking is $6.25 for less than 2 hours, and $10 for 2+ hours. Pay stations on each floor accept $1, $5 and $10 bills as well as credit/debit cards. Be advised, pay stations do not provide change. Please have exact amount. From the garage, Seven Hills' entrance can be accessed from State Drive by walking Southwest towards the A.S. Children's Center and taking the staircase beside it up one flight. Wheelchair access: go past the A.S. Children's Center and take a left onto the path. Follow to the entrance to the Seven Hills Conference Center.



UNIVERSITY MAP & CONFERENCE CENTER LOCATION+



WEDNESDAY APRIL 3

Wednesday, April 3, 2024

Please note all shown times are Pacific Daylight Time (PDT)

8:40am–9:00am	**Plenary Session 1: (Track A- Nob Hill Room)** **Introduction, Committee Recognitions, Best Paper Awards**		
9:00am-9:35am	**Keynote:** Cross-Layer Optimization of Energy Harvesting and Storage **Naehyuck Chang, *Executive Vice President, Samsung SDI America***		
9:35am–10:10am			
10:10am–10:20am	**Break**		
10:20am–11:40am	**Session 1A (Nob Hill Room)** **Novel Integrated Circuits and Systems**	**Session 1B (Russian Hill Room)** **Rapid Circuit Simulation, Verification and Test**	**Session 1C (Mt. Davidson Room)** **Hardware Security Primitives**
11:40am-12:25pm	**ISQED Lunch Keynote** Why we did not have flying cars for 100 years **Jim Dukhovny, *CEO, Alef Aeronautics***		
12:25pm-13:25am	**Embedded Tutorial 1 (Track A)** Advanced Packaging for Heterogenous Integration *Presenter:* Tolga Acikalin, Intel Labs		
13:25pm-13:30pm	**Break**		
13:30pm-15:10pm	**Session 2A (Nob Hill Room)** **Upstream Synthesis and Machine Learning**	**Session 2B (Russian Hill Room)** **Hardware Trojan Attacks and Detection**	**Session 2C (Mt. Davidson Room)** **DNN Acceleration**
15:10pm-15:15pm	**Break**		
15:15pm-16:45pm	**Panel Discussion - (Track A - Nob Hill Room)** AI Hardware: Opportunities and Challenges		

THURSDAY APRIL 4

Thursday, April 4, 2024

Please note all shown times are Pacific Daylight Time (PDT)

	Plenary Session 2: (Track A - Nob Hill Room)		
8:45am–9:00am	**Welcome**		
9:00am–9:35am	**Keynote:** **Reflections on Microelectronic and Microelectromechanical Technologies and the Challenges of Implementing Emerging Technologies** **Clare D. Thiem, *Air Force Research Laboratory/RITB***		
9:35am–9:40am	**Break**		
9:40am-10:35am	**Session PW1 (Nob Hill Room, Track A)** **Poster & WIP Session 1**	**Session PW2 (Russian Hill Room, Track B)** **Poster & WIP Session 2**	**Session PW3 (Mt. Davidson Room, Track C)** **Poster & WIP Session 3**
10:35am-10:45am	**Break**		
10:45am–12:25pm	**Session 3A (Nob Hill Room)** **Simulation and Estimation Automation**	**Session 3B (Russian Hill Room)** **Novel Computing**	**Session 3C (Mt. Davidson Room)** **Algorithms, Architectures, and Circuits for Efficient AI/ML Computing**
12:25pm-13:05	**Lunch Break**		
13:05pm-14:05pm	**Embedded Tutorial 2 (Track A - Nob Hill Room)** **Securing Ubiquitous Devices with Lightweight Circuit Primitives** *Presenter:* Kaiyuan Yang, Rice University		
14:05pm-14:10pm	**Break**		
14:10pm-15:50pm	**Session 4A (Nob Hill Room)** **Advances in Physical Design Automation**	**Session 4B (Russian Hill Room)** **Side channel Signals in Hardware Security**	**Session 4C (Mt. Davidson Room)** **Next Generation IoT**

FRIDAY APRIL 5

Friday, April 5, 2024

Please note all shown times are Pacific Daylight Time (PDT)

9:00am-10:40am	**Session 5A** (Nob Hill Room) **Emerging Computing Paradigms**	**Session 5B** (Russian Hill Room) **Learning on the Edge**	**Session 5C** (Mt. Davidson Room) **AI for Cyber Security**
10:40am-10:45am	**Break**		
10:45am–12:05pm	**Session 6A** (Nob Hill Room) **FAQ: FPGAs, Accelerators, Quantum**	**Session 6B** (Russian Hill Room) **AI Accelerator Hardware Design**	**Session 6C** (Mt. Davidson Room) **Quantum Computing**

Wednesday April 3

9:00 AM - 9:35 AM

Room: Nob Hill

Cross-Layer Optimization of Energy Harvesting and Storage

Naehyuck Chang

Executive Vice President, Samsung SDI America

The use of energy harvesting is mandatory for carbon-neutral ecosystems. For portable systems, energy harvesting makes it possible to operate them without full-capacity batteries. Energy harvesting generally lacks load-following capability; harvesting-storage-use is a typical energy harvesting system structure. Appropriate power conversion processes are commonly used during the transition between harvesting, storage, and use. Material and device research is the mainstream for energy harvesting, which provides fundamental solutions for more efficient energy harvesting. However, proper system-level management is also vital. This talk will introduce several cross-layer optimization practices of the harvesting-storage-use systems for a range of applications, from wearable devices to electric vehicles and grid-connected energy storage systems. First, we will introduce the online reconfiguration of photovoltaic arrays combating partial shading with examples of stationary and onboard energy harvesting for electric vehicles. We will also mention the online reconfiguration of thermoelectric device arrays dealing with the temperature gradient of the vehicle radiator. Second, we will address radical cross-layer optimization of a wearable solar energy harvesting system, deleting the entire storage and conversion processes. We demonstrate that aggressive dynamic power management can delete the energy storage and power converters. While load following is a typical setup of the energy harvesting system, such a radical cross-layer optimization makes the load (a UV detector) follow the energy harvesting of a photovoltaic cell. Finally, we will introduce solar energy harvesting with energy storage, one of the most promising ways to overcome the Duck Curve.

About Naehyuck Chang

Naehyuck Chang is an Executive Vice President at Samsung SDI America. He was the previous Head of Development at Samsung SDI Headquarters from 2021 to 2023. Dr. Chang was in charge of all the automotive and energy-storage product developments, from cells to systems. From 1997 to 2014, he was with the Department of Computer Science and Engineering at Seoul National University. Since 2014, he has been a Full Professor at the Department of Electrical Engineering, Korea Advanced Institute of Science and Technology. Dr. Chang is a Fellow of the ACM and a Fellow of IEEE for his contributions to low-power systems. Dr. Chang is a member of the National Academy of Engineering of Korea. Dr. Chang's research interests include low-power cyber-physical systems and Design Automation of Things, such as systematic design and optimization of fuel cell systems, energy storage systems, electric vehicles, drones, and energy harvesting. Dr. Chang is specifically interested in mobility electrification in terms of design, optimization, and management of the power, energy, and lifetime of the battery cells. Dr. Chang was the Chair and the Past Chair of the ACM Special Interest Group on Design Automation. Dr. Chang was the TPC Co-Chair of DAC 2016, ASP-DAC 2015, ICCD 2014, CODES+ISSS 2012, and ISLPED 2009, and the General Co-Chair of VLSI-SoC 2015, ICCD 2015 and 2014, and ISLPED 2011. He was the recipient of the 2014 ISLPED Best Paper Award, the 2011 SAE Vincent Bendix Automotive Electronics Engineering Award, the 2011 Sinyang Academic Award, the 2009 IEEE SSCS International SoC Design Conference Seoul Chapter Award, and various ISLPED Low-Power Design Contest Awards in 2002, 2003, 2004, 2007, 2012, 2014, and 2017, respectively. Dr. Chang was the Editor-in-Chief of the ACM Transactions on Design Automation of Electronics Systems. He was an Associated Editor for the IEEE Transactions on VLSI, IEEE Transactions on CAD, ACM Transactions on Embedded Computing Systems, IEEE Embedded Systems Letters, and IEEE Transactions on Circuits and Systems Part I.

ISQED Keynote 1P.2

Wednesday April 3

11:45 AM - 12:20 PM

Room: Nob Hill

Why we did not have flying cars for 100 years

Jim Dukhovny

CEO, Alef Aeronautics

For more than a hundred years, the concept of flying cars has captured the imagination of innovators, engineers, and the general populace, promising a revolution in how we perceive personal and city travel. However, despite the long-held aspirations and technological progress, our cityscapes are yet to witness the bustling activity of airborne vehicles that many had envisioned. In his keynote speech, Jim Dukhovny, CEO of Alef Aeronautics, provides an insightful analysis into why the vision of flying cars has not materialized over the past century, dissecting the intricate array of technical, regulatory, and societal obstacles that have impeded their fruition. The presentation delves into the substantial barriers that have historically derailed this innovation. It highlights the formidable engineering feats required to produce vehicles that are both airworthy and road-ready, ensuring safety, efficiency, and reliability, alongside navigating the complex regulatory frameworks that oversee both airspace and terrestrial mobility. This exploration sheds light on the numerous elements that have maintained flying cars as a futuristic concept rather than a present-day reality.

About Jim Dukhovny

Jim Dukhovny is the CEO of Alef Aeronautics, a sustainable electric transportation company that is designing and developing the world's first flying car. Dukhovny has received education from UC Berkeley, Santa Clara University, and Stanford University. Influenced by his father, Leonid Dukhovny, a well-known singer-songwriter, poet, scientist, and avid science fiction lover, Jim Dukhovny has created a number of organizations spanning the entertainment, software, and non-profit industries. Among his notable achievements, Dukhovny co-founded and led startups such as Intellectual Casino, Transcoder, DjWizard Presents, was the president of the Science Fiction Society of Silicon Valley and contributed to the architecture of Windows 10, Walmart's online imaging system, and a number of Yahoo products. In 2015, Dukhovny, together with Constantine Kisly, Pavel Markin, and Oleg Petrov, founded Alef Aeronautics to develop the world's first flying car. The prototype of this car successfully debuted in 2022 and through pre-sales became the world's best-selling aircraft in 2023.

ISQED Keynote 2P.1

Thursday April 4

9:00 AM - 9:35 AM

Room: Nob Hill

Reflections on Microelectronic and Microelectromechanical Technologies and the Challenges of Implementing Emerging Technologies

Clare D. Thiem

Air Force Research Laboratory (AFRL)

Mr. Clare D. Thiem's keynote at ISQED'24, titled "Reflections on Microelectronic and Microelectromechanical Technologies and the Challenges of Implementing Emerging Technologies," provides a comprehensive exploration of the complex landscape surrounding the integration of emerging technologies into microelectronic and microelectromechanical systems. Leveraging extensive expertise cultivated at the Air Force Research Laboratory (AFRL), Mr. Thiem offers nuanced insights into the multifaceted challenges and opportunities inherent in this dynamic domain. By examining the intricate interplay between technological innovation and practical implementation, Thiem equips attendees with invaluable perspectives and strategies essential for navigating the ever-evolving landscape of modern engineering.

About Clare D. Thiem

Mr. Thiem is a Senior Electronics Engineer in the Air Force Research Laboratory's (AFRL's) Information Directorate's High Performance Systems Branch (RITB). His current research interests pursue the development of practical, hardware-based, biologically inspired computing technology for Department of Air Force for size, weight, and power constrained systems. He currently serves as the Air Force Program Manager for the OUSD(R&E) funded Tri-Service, A Combined Development Pipeline for Novel Neuromorphic Hardware (NeuroPipe) Tri-Service Advanced Research for the Advancement of S&T Priorities (ARAP). He is the Program Manager for the Day 1 Deployable Machine Learning Program and Chief Engineer/ Deputy Program Manager for the Emerging Nanotechnology for Autonomous Systems Program. He is an AFRL/RI Topic Lead for the Extreme Neuromorphic Materials and Computing Center of Excellence (CoE), and the AFRL Lead for Computational Efficiency in the Efficient and Robust Machine Learning (ERML) CoE. Mr. Thiem leverages over 36 years of technical experience and leadership within the Department of Defense working with a variety of technologies. He earned a Master of Science, 2002, Mechanical Engineering, National Technological University, Fort Collins, CO; and a Bachelor of Science in Engineering, 1986, Aerospace Engineering, College of Engineering, The University of Michigan, Ann Arbor, MI. He has authored/co-authored over 40 publications.

Panel Discussion

Wednesday April 3

3:15 PM–4:45 PM

Room: Nob Hill

AI Hardware: Opportunities and Challenges

Panelists:

Arnab Raha - Intel
Garrett S. Rose - University of Tennessee Knoxville
Akhilesh Jaiswal - University of Wisconsin Madison
Syed Shakib Sarwar - Meta Inc.
Cindy Yi - Virginia Tech

Modedrator/Chair:

Ahmedullah Aziz - University of Tennessee Knoxville

Summary:
In the contemporary fabric of our civilization, artificial intelligence (AI) has emerged as a pivotal force, permeating various facets of our daily lives. Its significance lies in its ability to augment human capabilities, streamline processes, and catalyze breakthroughs in fields ranging from healthcare to finance. As AI applications become increasingly sophisticated, the importance of dedicated hardware tailored to meet the unique computational demands of these intelligent systems has come to the forefront. The growing complexity of AI algorithms, particularly in the realm of deep learning, necessitates specialized hardware architectures. Such dedicated AI hardware serves as the backbone for processing vast amounts of data and executing intricate calculations with remarkable speed and efficiency. This optimized hardware not only accelerates the training and inference processes but also contributes to the scalability and practicality of AI applications. As AI continues to evolve, researchers are uncovering novel algorithms and models that push the boundaries of what is achievable. In this dynamic landscape, the hardware supporting AI must adapt and innovate to fully realize the potential of emerging technologies. The symbiotic relationship between AI advancements and specialized hardware underscores the critical role that hardware research plays in shaping the trajectory of artificial intelligence, ensuring its seamless integration into the fabric of our technologically driven civilization. Embark on a riveting exploration of AI hardware with our expert panel. Explore the expansive potential of advanced processors and innovative accelerators, dissecting the intricate landscape that defines artificial intelligence hardware. Seasoned experts guide the audience through the dual lens of opportunities and challenges, addressing key facets such as scalability, energy efficiency, and the symbiotic interplay with software. This panel promises a compelling journey into the forefront of AI hardware, where challenges are viewed as gateways to innovation, shaping the future of computational prowess. Join us for a captivating exploration of the evolving landscape at the intersection of hardware technology and artificial intelligence.

Embedded Tutorial 1

Wednesday April 3

12:25 AM - 1:25 PM

Nob Hill Room

Advanced Packaging for Heterogenous Integration

Tolga Acikalin

Intel Labs

Summary:

Emergence of artificial intelligence and machine learning, specifically recent developments on large language models, along with trends in internet of things and big data is driving new wave of growth in semiconductors. Heterogeneous integration (HI) is a powerful and key enabler to meet the demands of continued growth of computing and communication performance. Heterogeneous integration involves the integration of separately manufactured components with different functions into a higher-level assembly that, in aggregate, provides enhanced functionality and improved operating characteristics. System level co-design and optimization will be key to achieve the best performance where packaging plays a key role. This tutorial will provide a brief evolution of packaging technologies, and focus on advanced packaging architectures for HI. Key features in 2D and 3D interconnects will be presented along with novel packaging materials (e.g. glass) as well as co-packaged optics using silicon photonics. Furthermore in this tutorial, power-delivery and thermal considerations in advanced packaging will be discussed from a system design perspective.

About Tolga Acikalin

Tolga Acikalin earned his Bachelor of Science degree in Mechanical Engineering from Middle East Technical University, Ankara, Turkey, and his Master of Science. and Ph.D. degrees from Purdue University, West Lafayette, IN. Joining Intel in 2007 as a Research and Development Engineer, he worked on various assembly and test pathfinding projects in the Technology and Manufacturing Group, Chandler, AZ. Since 2013, he has been at Intel Labs in Santa Clara, CA. He is currently a Principal Engineer with Intel Labs, driving innovative strategies for heterogeneous system integration from package to wafer scale with an emphasis on next generation interconnect technologies. His research focuses on glass for heterogenous integration, co-packaged optics and silicon photonics, optical and sub-THz to THz RF high-speed interconnects, and their respective package architectures. Tolga has authored or co-authored more than 15 peer-reviewed conference and journal papers in leading APS, ASME, and IEEE publications and holds 5 issued patents along with over 30 filed patents.

Embedded Tutorial 2

Thursday April 4

1:05 PM - 2:05 PM

Nob Hill Room

Securing Ubiquitous Devices with Lightweight Circuit Primitives

Prof. Kaiyuan Yang

Rice University

Summary:

Security and privacy are critical challenges to overcome for ubiquitous electronics, including IoT and wearable/implantable devices. Securing these systems faces not only new challenges at system and network levels due to a vast variance of applications, system constructions, and attack surfaces, but also severe hardware resource constraints on computation resources, power consumption, and device cost. To tackle these challenges, significant research efforts have been pursuing specialized hardware-enabled security primitives that could help build a reliable, trustful, and energy-efficient foundation for system security. This tutorial will give an overview of the problems and focus on three hardware security challenges that could be dealt with through novel circuit designs, namely entropy generation, countermeasures against side-channel and fault-injection attacks, and lightweight computing for security. I will review state-of-the-art circuit-enabled security primitives, including our recent work towards all-digital, fully synthesizable, and compact circuit techniques that enable agile SoC development and technology portability. Novel circuit principles that cross the boundary of traditional digital and analog designs have led to significant improvements in the performance and overheads of these security primitives.

About Kaiyuan Yang

Kaiyuan Yang is an Associate Professor of Electrical and Computer Engineering at Rice University, USA, where he leads the Secure and Intelligent Micro-Systems (SIMS) lab. He received his B.S. degree in Electronic Engineering from Tsinghua University, China, in 2012, and his Ph.D. degree in Electrical Engineering from the University of Michigan - Ann Arbor, in 2017. His research interests include low-power integrated circuits and system design for secure and intelligent microsystems, bioelectronics, hardware security, and mixed-signal computing. He is a recipient of the NSF CAREER Award, IEEE SSCS Predoctoral Achievement Award, Best Paper Awards at 2022 ACM MobiCom, 2021 IEEE CICC, 2016 IEEE S&P (Oakland), and 2015 IEEE ISCAS, and several best paper award nominations at premier conferences. He has given invited talks at major conferences including ISSCC, IEDM, ICCAD, RFIC, ASSCC, etc. His work was also recognized as the research highlight of Communications of ACM and ACM GetMobile magazines, the cover of Nature Biomedical Engineering, and Top Picks in Hardware and Embedded Security.

SESSION 1A

Wednesday April 3

Novel Integrated Circuits and Systems

Chair: **Suyash Ranjan**, Qualcomm, San Diego

10:20AM
1A.1
HISPE: High-Speed Configurable Floating-Point Multi-Precision Processing Element
Tejas N[1], Rakshit Bhatia[1], Madhav Rao[2]
[1]IIIT-Bangalore, [2]International Institute of Information Technology-Bangalore

10:40AM
1A.2
A 0.186 pJ/bit, 6-Gb/s, Energy-Efficient, Half-Rate Hybrid Circuit Topology in 1.2V, 65 nm CMOS.
Prema Kumar Govindaswamy[1], Mursina Khatun[2], Vijay Shankar Pasupureddi[1]
[1]Indian Institute of Technology Bhubaneswar, [2]a23ec09005@iitbbs.ac.in

11:00AM
1A.3
A 1.2 V Double-Tail StrongARM Latch Comparator with 51 fJ/comparison and 380 µV Input Noise in 65 nm CMOS Technology
Srinivasa Rao Maram[1], Boyapati Subrahmanyam[2], Vijay Shankar Pasupureddi[1]
[1]Indian Institute of Technology Bhubaneswar, [2]FH-Kaernten

11:20AM
1A.4
HiCTL: High Fan-in Differential Capacitive-Threshold-Logic Gate Implementation With An Offset-Compensated Comparator
Abdullah Sahruri[1], Martin Margala[1], Ugur Cilingiroglu[2]
[1]University of Louisiana at Lafayette, [2]Yeditepe University

SESSION 1B

Wednesday April 3

Rapid Circuit Simulation, Verification and Test

Chair: **Chidhambaranathan R**, Synopsys Inc.

10:20AM
1B.1
Quantum Circuit Simulation with Fast Tensor Decision Diagram
Qirui Zhang, Mehdi Saligane, Hun Seok Kim, David Blaauw, Georgios Tzimpragos, Dennis Sylvester
University of Michigan

10:40AM
1B.2
Dual Use Circuitry for Early Failure Warning and Test
Alexander Coyle[1], Hui Jiang[1], Jennifer Dworak[1], Theodore Manikas[1], Kundan Nepal[2]
[1]Southern Methodist University, [2]University of St Thomas

11:00AM
1B.3
RTL Simulation Acceleration with Machine Learning Models
Chandan Karfa[1], Surajit Das[2], Hetang Patel[3], Disha Puri[4], Anshul Jain[4], Kartheek Bellamkonda[3], Rahul Reddy[3], Arijit Sur[3], Pradip Prajapati[5]
[1]Indian Institute of Technology Guwahati, [2]Postdoctoral Research Associate, [3]IIT Guwahati, [4]Intel, [5]Inrtel

11:20AM
1B.4
Automated Assertion Checker Generator and Information Flow Tracking for Security Verification
Miguel Alfaro Zapata, Amirhossein Shahshahani, Zeljko Zilic
McGill University

SESSION 1C

Wednesday April 3

Hardware Security Primitives

Chair: **Hossein Sayadi**, California State University, Long Beach

10:20AM
1C.1
DECOR: Enhancing Logic Locking Against Machine Learning-Based Attacks
Yinghua Hu[1], Kaixin Yang[2], Subhajit Dutta Chowdhury[2], Pierluigi Nuzzo[2]
[1]Synopsys, [2]University of Southern California

10:40AM
1C.2
TEE-Time: A Dynamic Cache Timing Analysis Tool for Trusted Execution Environments
Quentin Forcioli, Sumanta Chaudhuri, Jean-luc Danger
Telecom Paris

11:00AM
1C.3
Obfuscating Quantum Hybrid-Classical Algorithms for Security and Privacy
Suryansh Upadhyay[1] and Swaroop Ghosh[2]
[1]Penn State University, [2]Pennsylvania State University

11:20AM
1C.4
A 5T Half-SRAM Design for Cold CMOS Physical Unclonable Function Applications and Beyond
Rouwaida Kanj[1] and Jamil Kawa[2]
[1]Synopsys (American University of Beirut, on leave), [2]Synopsys

11:40AM
1C.5
Model Extraction Attack against On-device Deep Learning with Power Side Channel
Jialin Liu and han wang
Temple University

SESSION 2A

Wednesday April 3

Upstream Synthesis and Machine Learning

Chair: **Murthy Palla**, Synopsys
Co-Chair: **Huan Yu**, Apple

1:30PM
2A.1
Fake Timer: An Engine for Accurate Timing Estimation in Register Transfer Level Designs
Daniela Sanchez Lopera[1], Robert Kunzelmann[1], Endri Kaja[2], Wolfgang Ecker[1]
[1]Technical University of Munich & Infineon Technologies AG, [2]Technische Universität Kaiserslautern & Infineon Technologies AG

1:50PM
2A.2
High-Level Synthesis for Microfluidic Biochips Considering Actual Volume Management and Channel Storage
Zhengyang Chen[1], Yuhan Zhu[1], Zhen Chen[1], Zhisheng Chen[2], Genggeng Liu[1]
[1]College of Computer and Data Science, Fuzhou University, [2]School of Informatics, Xiamen University

2:10PM
2A.3
Exploration of Activation Fault Reliability in Quantized Systolic Array-Based DNN Accelerators
Mahdi Taheri[1], Natalia cherezova[2], Mohammad Saeed Ansari[3], Maksim Jenihhin[2], ALI Mahani[4], Masoud Daneshtalab[5], Jaan Raik[2]
[1]PhD researcher at Tallinn university of Technology, [2]Tallinn University of Technology, [3]University of Alberta, [4]Shahid Bahonar University of Kerman, [5]KTH Royal Institute of Technology

2:30PM
2A.4
Comparative Analysis of Graph Isomorphism and Graph Neural Networks for Analog Hierarchy Labeling
Zhengfeng Wu and Ioannis Savidis
Drexel University

2:50PM
2A.5
SRAM-PG: Power Delivery Network Benchmarks from SRAM Circuits
Shan Shen, Zhiqiang Liu, Wenjian Yu
Tsinghua University

SESSION 2B

Wednesday April 3

Hardware Trojan Attacks and Detection

Chair: **Mohammad Ashiqur Rahman**, Florida International University

1:30PM
2B.1
A Needle in the Haystack: Inspecting Circuit Layout to Identify Hardware Trojans
Xingyu Meng[1], Abhrajit Sengupta[2], Kanad Basu[1]
[1]University of Texas at Dallas, [2]New York University

1:50PM
2B.2
Trojan Assets and Attack Vectors in Processors
Czea Sie Chuah[1], Alexander Hepp[2], Christian Appold[1], Tim Leinmüller[1]
[1]DENSO Automotive Deutschland GmbH, [2]Technical University of Munich, TUM School of Computation, Information and Technology

2:10PM
2B.3
Trojan Attacks on Variational Quantum Circuits and Countermeasures
Subrata Das and Swaroop Ghosh
The Pennsylvania State University

2:30PM
2B.4
FAST-GO: Fast, Accurate, and Scalable Hardware Trojan Detection using Graph Convolutional Networks
Ali Imangholi[1], Mona Hashemi[2], Amirabbas Momeni[1], Siamak Mohammadi[3], Trevor E. Carlson[4]
[1]School of ECE, College of Eng., University of Tehran, [2]School of ECE, College of Eng., University of Tehran, and School of Computing, National University of Singapore, [3]School of ECE, College of Eng., University of Tehran, and School of Computing Science, IPM, [4]National University of Singapore

SESSION 2C

Wednesday April 3

DNN Acceleration

Chair: **Cheng Tan**, Google

1:30PM
2C.1
Optimizing Layer-Fused Scheduling of Transformer Networks on Multi-accelerator Platforms
Steven Colleman[1], Arne Symons[1], Victor Jung[2], Marian Verhelst[1]
[1]KULeuven, [2]ETH Zurich

1:50PM
2C.2
Roofline Performance Analysis of DNN Architectures on CPU and GPU Systems
Prashanth H C[1] and Madhav Rao[2]
[1]IIIT-Bangalore, [2]International Institute of Information Technology-Bangalore

2:10PM
2C.3
PSO Optimized Design of Error Balanced Weight Stationary Systolic Array Architecture for CNN
Dantu Nandini Devi[1], Gandi Ajay Kumar[2], Bindu G Gowda[2], Madhav Rao[3]
[1]International Institute of Information Technology Bangalore, [2]international institute of information technology, bangalore, [3]International Institute of Information Technology-Bangalore

2:30PM
2C.4
DNN Memory Footprint Reduction via Post-Training Intra-Layer Multi-Precision Quantization
Behnam Ghavami[1], Amin Kamjoo[1], Lesley Shannon[1], Steve Wilton[2]
[1]Simon Fraser University, [2]UBC

SESSION PW1

Thursday April 4

Poster & WIP Session 1

Chair: **Cindy Yang Yi**, Virginia Tech

9:40AM
PW1.1
Error Distribution Estimation for Fixed-point Arithmetic using Program Derivatives
Soramichi Akiyama[1], Ryota Shioya[2], Yuto Miyatake[3], Tongxin Yang[4]
[1]Ritsumeikan University, [2]The University of Tokyo, [3]Osaka University, [4]Sony Semiconductor Solutions Corporation

9:45AM
PW1.2
An Automated Exhaustive Fault Analysis Technique guided by Processor Formal Verification Methods
Endri Kaja[1], Nicolas Gerlin[1], Bihan Zhao[1], Daniela Lopera[1], Jad Halabi[1], Azam Khan[1], Sebastian Prebeck[1], Dominik Stoffel[2], Wolfgang Kunz[2], Wolfgang Ecker[1]
[1]Infineon Technologies AG, [2]Rheinland-Pfalzische Technische Universität Kaiserslautern-Landau

9:50AM
PW1.3
Timing-Driven High-Level Synthesis for Continuous-Flow Microfluidic Biochips
ZhengYang Ye[1], Zhisheng Chen[2], Youlin Pan[3], Genggeng Liu[3], Wenzhong Guo[3], Tsung-Yi Ho[4], Xing Huang[5]
[1]Fuzhou University, [2]Xiamen University, Xiamen, [3]Fuzhou University, Fuzhou, [4]Department of Computer Science and Engineering, The Chinese University of Hong Kong, Hong Kong, [5]School of Computer Science, Northwestern Polytechnical University, Xi'an

9:55AM
PW1.4
Swarm - A VLSI Timing, Fanout-aware Clustering Algorithm
Christos Sotiriou[1], George Goudroumanis[1], Nikolaos Sketopoulos[1], Christos Georgakidis[2]
[1]Univesity of Thessaly - Department of Electrical and Computer Engineering (EECE), [2]University of Thessaly

10:00AM
PW1.5
FastPASE: An AI-Driven Fast PPA Speculation Engine for RTL Design Space Optimization
Akash Levy[1], Joe Walston[2], Sourav Samanta[2], Priyanka Raina[1], Stelios Diamantidis[2]
[1]Stanford University, [2]Synopsys, Inc.

10:05AM
PW1.6
MORE-Router+: Multilayer Multi-capacity ORdered Escape Routing via Bus-oriented Layer Assignment
Zhenyi Gao, Sheqin Dong, Zifei Cheng, Wenjian Yu
Tsinghua University

10:10AM
PW1.7
EDA-ML: Graph Representation Learning Framework for Digital IC Design Automation
Pratik Shrestha and Ioannis Savidis
Drexel University

10:15AM
PW1.8
Graph Neural Network-Based Detailed Placement Optimization Framework
DhoUI Lim[1] and Heechun Park[2]
[1]Kookmin University, School of Electrical Engineering, [2]UNIST

10:20AM
PW1.9
Ultra-Low Voltage Enablement for Standard Cells with Moment based LVF
ROHIT GUPTA, Chiranjeev Grover, Etienne Maurin, Olivier Minez, Jean-arnaud Francois, Sebastien Marchal
STMicroelectronics

10:25AM
PW1.10
Advancing Analog Reservoir Computing through Temporal Attention and MLP Integration
Khalil Sedki and Yang Yi
Virginia Tech

SESSION PW2

Thursday April 4

Poster & WIP Session 2

Chair: **Hossein Sayadi**, California State University, Long Beach

9:40AM
PW2.1
Unleashing Energy-Efficiency: Neural Architecture Search without Training for Spiking Neural Networks on Loihi Chip
Shiya Liu and Yang Yi
Virginia Tech

9:45AM
PW2.2
Composite Sub-surface Model for RF GaN-HEMTs
Xing Zhou[1], Wanlan Yang[1], Siau Ben Chiah[2]
[1]Nanyang Technological University, [2]New Silicon Corporation Pte Ltd

9:50AM
PW2.3
RASH: Reliable Deep Learning Acceleration using Sparsity-based Hardware
Shamik Kundu[1], ARNAB RAHA[2], Deepak Mathaikutty[2], Kanad Basu[1]
[1]University of Texas at Dallas, [2]Intel Corporation

9:55AM
PW2.4
Exploring Model Poisoning Attack to Convolutional Neural Network Based Brain Tumor Detection Systems
Kusum Lata[1], Prashant Singh[2], Sandeep Saini[2]
[1]LNMIIT Jaipur, [2]The LNM Institute of Information Technology, Jaipur

10:00AM
PW2.5
Sensitivity Analysis of SOT-MTJs to Manufacturing Process Variation: A Hardware Security Perspective
Mousam Hossain[1], Muhtasim Alam Chowdhury[2], Ronald DeMara[1], Soheil Salehi[3]
[1]University of Central Florida, [2]University of Arizona, [3]Department of Electrical and Computer Engineering, University of Arizona

10:05AM
PW2.6
Lightweight Multicast Authentication in NoC-based SoCs
Hansika Weersena and Prabhat Mishra
University of Florida

10:15AM
PW2.7
Trimming The Fat: A Minimum-Security Architecture for Protecting SoC Designs Against Supply Chain Threats
Kshitij Raj[1], Aritra Bhattacharyay[2], Swarup Bhunia[3], Sandip Ray[4]
[1]University of Florida, [2]Department of Electrical and Computer Engineering, University of Florida, [3]Department of Electrical and Computer Engineering, University of Florida, [4]Department of Electrical and Computer Engineering, University of Florida, Gainesville

10:20AM
PW2.8
Blending Scheduling Barriers: A Hybrid Approach for FPGA-based Post-Quantum Cryptography
Capucine Berger-Sigrist[1] and Andrea Guerrieri[2]
[1]EPFL, [2]EPFL and HES-SO

10:25AM
PW2.9
A Low-cost keyword spotting architecture based on wavelet packets feature extraction for edge devices
Sayed Salehi and Prakash Dhungana
University of Kentucky

SESSION PW3

Thursday April 4

Poster & WIP Session 3

Chair: **Deliang Fan**, Johns Hopkins University

9:40AM
PW3.1
SCORCH: Neural Architecture Search and Hardware Accelerator Co-design with Reinforcement Learning
Siqin Liu and Avinash Karanth
Ohio University

9:45AM
PW3.2
SpotLight: A Hotspot-Greedy, Light-Weighted, and Automated Thermal Modeling Framework for Early Smartphone Design
Chin-Wei Wu[1], Yu-Min Lee[2], Pei-Yu Huang[2], Bo-Jiun Yang[1], Tai-Yu Chen[1], Ting-Chang Huang[1], Yen-Lin Lee[1]
[1]MediaTek Inc., [2]National Yang Ming Chiao Tung University

9:50AM
PW3.3
Performance-Aware Design of Approximate Integrated MAC Factored Systolic Array Accelerators
Dantu Nandini Devi[1], Gandi Ajay Kumar[2], Bindu G Gowda[2], Madhav Rao[3]
[1]International Institute of Information Technology Bangalore, [2]international institute of information technology, bangalore, [3]International Institute of Information Technology-Bangalore

9:55AM
PW3.4
An Energy-Efficient time Domain Based Compute In-Memory Architecture for Binary Neural Network
Subhradip Chakraborty[1], Dinesh Kushwaha[2], Abhishek Goel[3], Anmol Singla[4], Anand Bulusu[3], Sudeb Dasgupta[3]
[1]RGIPT Uttar Pradesh, [2]Student, [3]IIT Roorkee, [4]NIT Uttarakhand

10:00AM
PW3.5
A multi band flexible N-path filter suited for non-contiguous channel aggregation
Chadi Jabbour
Telecom Paris

10:05AM
PW3.6
Hardware Trojans in Quantum Circuits, Their Impacts, and Defense
Rupshali Roy[1], Subrata Das[2], Swaroop Ghosh[1]
[1]Pennsylvania State University, [2]The Pennsylvania State University

10:10AM
PW3.7
Thinking Outside the Clock: Physical Design for Field-coupled Nanocomputing with Deep Reinforcement Learning
Simon Hofmann, Marcel Walter, Lorenzo Servadei, Robert Wille
Technical University of Munich

10:15AM
PW3.8
Non-parametric Greedy Optimization of Parametric Quantum Circuits
Koustubh Phalak and Swaroop Ghosh
Pennsylvania State University

10:20AM
PW3.9
Merits of Time-Domain Computing for VMM - A Quantitative Comparison
Florian Freye[1], Jie Lou[1], Christian Lanius[1], Tobias Gemmeke[2]
[1]Chair of Integrated Digital Systems and Circuit Design at RWTH Aachen University, [2]RWTH Aachen University

10:25AM
PW3.10
nvXNOR Design with Enhanced Store Capability for BNN Applications
Zeinab Soueidan[1] and Rouwaida Kanj[2]
[1]American University of Beirut, [2]Synopsys, American University of Beirut on Leave

SESSION 3A

Thursday April 4

Simulation and Estimation Automation

Chair: **Chidhambaranathan Rajamanikkam**, Synopsys
Co-Chair: **Zhong Guan**, UC Santa Barbara

10:45AM
3A.1
Fast Current Constraints Generation for Chip Safety
Cedric Feghali and Farid Najm
University of Toronto

11:05AM
3A.2
Toward Early Stage Dynamic Power Estimation: Exploring Alternative Machine Learning Methods and Simulation Schemes
Philipp Fengler[1], Sani Nassif[2], Ulf Schlichtmann[1]
[1]Technical University of Munich, [2]Technical University of Munich & Radyalis

11:25AM
3A.3
A novel virtual prototyping methodology for timing-accurate simulation of AMS circuits
Teo Vallone[1], Hayri Hasou[2], Ernesto Colizzi[2], Sara Vinco[3], Davide Zoni[1]
[1]Politecnico di Milano, [2]Infineon Technologies, [3]Politecnico di Torino

11:45AM
3A.4
GridVAE: Fast Power Grid EM-Aware IR Drop Prediction and Fixing Accelerated by Variational AutoEncoder
Yibo Liu and Sheldon Tan
University of Califronia, Riverside

12:05PM
3A.5
Full Stage Delay Calculation Using Full Waveform Propagation and Standard Library CCS Model
Stavros Simoglou[1], Iordanis Lilitsis[2], Nikolaos Blias[2], Christos Sotiriou[2]
[1]Synopsys, [2]Univesity of Thessaly - Department of Electrical and Computer Engineering (EECE)

SESSION 3B

Thursday April 4

Novel Computing

Chair: **Kang Jun Bai**, Air Force Research Laboratory

10:45AM
3B.1
An FPGA-based Max-K-Cut Accelerator Exploiting Oscillator Synchronization Model
Mohammad Khairul Bashar[1], Zheyu Li[2], Vijaykrishnan Narayanan[2], Nikhil Shukla[1]
[1]University of Virginia, [2]Pennsylvania State University

11:05AM
3B.2
A Comparative Analysis of Microrings Based Incoherent Photonic GEMM Accelerators
Sairam Sri Vatsavai, Venkata Sai Praneeth Karempudi, Oluwaseun Alo, Ishan Thakkar
University of Kentucky

11:25AM
3B.3
A SIMD Dynamic Fixed Point Processing Engine for DNN Accelerators
Gopal Raut[1], PRANOSE EDAVOOR[2], DAVID SELVAKUMAR[3], ritambhara thakur[1]
[1]CDAC Bangalore, [2]CENTRE FOR DEVELOPMENT OF ADVANCED COMPUTING, [3]C-DAC, BANGALORE

11:45AM
3B.4
Exploring Hardware Activation Function Design: CORDIC Architecture in Diverse Floating Formats
Mahati Basavaraju[1], Vinay R[1], Madhav Rao[2]
[1]International Institute of Information Technology, Bangalore, [2]International Institute of Information Technology-Bangalore

SESSION 3C

Thursday April 4

Algorithms, Architectures, and Circuits for Efficient AI/ML Computing

Chair: **Jeff Zhang**, Arizona State University

10:45AM
3C.1
Single-Ferroelectric FET based Associative Memory for Data-Intensive Pattern Matching
Jiayi Wang, Songyu Sun, Xunzhao Yin
Zhejiang University

11:05AM
3C.2
sLLM: Accelerating LLM Inference using Semantic Load Balancing with Shared Memory Data Structures
Jieyu Lin[1], Sai Qian Zhang[2], Alberto Leon-Garcia[1]
[1]University of Toronto, [2]New York University

11:25AM
3C.3
Hyperdimensional Computing vs. Neural Networks: Comparing Architecture and Learning Process
Dongning Ma[1], Cong Hao[2], Xun Jiao[1]
[1]Villanova University, [2]Georgia Institute of Technology

11:45AM
3C.4
Fused Functional Units for Area-Efficient CGRAs
Ron Jokai, Cheng Tan, Jeff Zhang
ASU

12:05PM
3C.5
Hardware Support for Trustworthy Machine Learning: A Survey
Md Shohidul Islam[1], Ihsen Alouani[2], Khaled N. Khasawneh[1]
[1]George Mason University, [2]CSIT, Queen's University Belfast, UK

SESSION 4A

Thursday April 4

Advances in Physical Design Automation

Chair: **Zhong Guan**, UC Santa Barbara
Co-Chair: **Ioannis Savidis**, Drexel University

2:10PM
4A.1
Design-Technology Co-Optimization with Standard Cell Layout Generator for Pin Configurations
Junghyun Yoon[1] and Heechun Park[2]
[1]Kookmin University, School of Electrical Engineering, [2]UNIST

2:30PM
4A.2
Routing Intent Aware Pin Access Point Selection for Standard Cell Designs
Po-Chun Wang, Kai-Jie Ton, Rung-Bin Lin
Yuan Ze University

2:50PM
4A.3
SLO-ECO: Single-Line-Open Aware ECO Detailed Placement and Detailed Routing Co-Optimization
Joong-Won Jeon[1], Andrew Kahng[2], Jae-Hyun Kang[1], Jaehwan Kim[1], Mingyu Woo[2]
[1]Samsung Foundry, [2]UCSD

3:10PM
4A.4
Parasitic Capacitance Patterns Grid Density Binarization and Shifted Reflection Step Sequence Encoding for Dimensionality Reduction
Ping Li and Zhong Guan
Sun Yat-sen University

SESSION 4B

Thursday April 4

Side channel Signals in Hardwrare Security

Chair: **Ujjwal Guin**, Auburn University

2:10PM
4B.1
Side-channel-driven Intrusion Detection System for Mission Critical Unmanned Aerial Vehicles
Alejandro Almeida, Muneeba Asif, Md Tauhidur Rahman, Mohammad Rahman
Florida International University

2:30PM
4B.2
Deep Learning Enhanced Side Chanel Analysis on CRYSTALS-Kyber
Tuan Hoang, Mark Kennaway, Dung Pham, Son Mai, Ayesha Khalid, Ciara Rafferty, Maire O'Neill
Queen's University Belfast

2:50PM
4B.3
Thermo-Attack Resiliency: Addressing a New Vulnerability in Opto-Electrical Network-on-Chips
Mahdi Hasanzadeh[1], Meisam Abdollahi[2], Amirali Baniasadi[2], Ahmad Patooghy[3]
[1]North Carolina A & T State University, [2]University of Victoria, [3]North Carolina A&T State University

3:10PM
4B.4
Enhanced Detection of Thermal Covert Channel Attacks in Multicore Processors
Krithika Dhananjay[1], Vasilis Pavlidis[2], Ayse Coskun[3], Emre Salman[1]
[1]Stony Brook University, [2]University of Manchester, [3]Boston University

3:30PM
4B.5
RTL Interconnect Obfuscation By Polymorphic Switch Boxes For Secure Hardware Generation
Haimanti Chakraborty and Ranga Vemuri
University of Cincinnati

SESSION 4C

Thursday April 4

Next Generation IoT

Chair: **Mimi Xie**, University of Texas at San Antonio

2:10PM
4C.1
Enhancing Self-sustaining IoT Systems with Autonomous and Smart UAV Data Ferry
Mason Conkel[1], Wen Zhang[2], Chen Pan[3]
[1]The University of Texas at San Antonio (UTSA), [2]Wright State University, [3]The University of Texas at San Antonio

2:30PM
4C.2
Learning Client Selection Strategy for Federated Learning across Heterogeneous Mobile Devices
Sai Qian Zhang[1], Jieyu Lin[2], Qi Zhang[3], Yu-Jia Chen[4]
[1]New York University, [2]University of Toronto, [3]Microsoft, [4]National Central University

2:50PM
4C.3
Deep Learning Based IoT System for Real-time Traffic Risk Notification
Sahidul Islam[1], Seth Klupka[2], Ramin Mohammadi[2], Yufang Jin[3], Mimi Xie[1]
[1]The University of Texas at San Antonio, [2]UTSA, [3]University of Texas at San Antonio

3:10PM
4C.4
Learning-Based Secure Spectrum Sharing for Intelligent IoT Networks
Amir Alipour-Fanid[1], Monireh Dabaghchian[2], Long Jiao[3], Kai Zeng[4]
[1]University of the District of Columbia, [2]Morgan State University, [3]University of Massachusetts Dartmouth, [4]George Mason University

SESSION 5A

Friday April 5

Emerging Computing Paradigms

Chair: **Ahmedullah Aziz**, The University of Tennessee, Knoxville

9:00AM
5A.1
Design and Evaluation of Parametric NTT Hardware Unit using different Multiplier based Modular Reduction Techniques
Lokesh Maji[1], Aman Prajapati[1], Madhav Rao[2]
[1]International Institute of Information Technology Bangalore, [2]International Institute of Information Technology-Bangalore

9:20AM
5A.2
Multi-ALM: Run-time Multi-Level Reconfigurable Approximate Logarithmic Multiplier
Maliha Tasnim, Chinmay Raje, Sheldon Tan
University of California Riverside

9:40AM
5A.3
SRAM-Based Analog Compute-In-Memory Architecture Using C-2C Ladder And Signal Margin Assisted Design Methodology
Dinesh Kushwaha[1], Ashish Joshi[2], Abhishek Goel[3], Rajiv Joshi[4], Sudeb Dasgupta[3], Anand Bulusu[3]
[1]Student, [2]Intel India, [3]IIT Roorkee, [4]IBM TJ Watson

10:00AM
5A.4
Efficient Radix-4 Approximated Modified Booth Multiplier for Signal Processing and Computer Vision: A Probabilistic Design Approach
Bindu G Gowda[1], Prashanth H C[2], Muralidhara V N[3], Madhav Rao[3]
[1]International Institute of Information Technology, Bangalore, [2]IIIT-Bangalore, [3]International Institute of Information Technology-Bangalore

10:20AM
5A.5
Reprogrammable Time-Domain RRAM Based Vector Matrix Multiplier for In-Memory Computing
Bipul Boro, Rushik Parmar, Ashvinikumar Dongre, Gaurav Trivedi
Indian Institute of Technology Guwahati

SESSION 5B

Friday April 5

Learning on the Edge

Chair: **Jeff (Jun) Zhang**, Arizona State University

9:00AM
5B.1
AutoAnnotate: Reinforcement Learning based Code Annotation for High Level Synthesis
Hafsah Shahzad[1], Ahmed Sanaullah[2], Sanjay Arora[2], Ulrich Drepper[2], Martin Herbordt[1]
[1]Boston University, [2]RedHat Inc.

9:20AM
5B.2
Write Intensity based Foresightful Page Migration for Hybrid memories
Aswathy NS[1] and Hemangee Kapoor[2]
[1]IIT Guwahati, [2]Indian Institute of Technology Guwahati

9:40AM
5B.3
RTKWS: Real-Time Keyword Spotting Based on Integer Arithmetic for Edge Deployment
Prakash Dhungana and Sayed Salehi
University of Kentucky

10:00AM
5B.4
Bring it On: Kinetic Energy Harvesting to Spark Machine Learning Computations in IoTs
sanket shukla and Sai Manoj Pudukotai Dinakarrao
George mason university

10:20AM
5B.5
Code-Based Cryptography for Confidential Inference on FPGAs: An End-to-End Methodology
Rupesh Karn[1], Johann Knechtel[2], Ozgur Sinanoglu[2]
[1]New York University, [2]New York University Abu Dhabi

SESSION 5C

Friday April 5

AI for Cybersecurity

Chair: **Hossein Sayadi**, California State University, Long Beach

9:00AM
5C.1
LLM-FIN: Large Language Models Fingerprinting Attack on Edge Devices
Najmeh Nazari[1], Furi Xiang[1], Chongzhou Fang[2], Hosein Mohammadi Makrani[2], Aditya Puri[1], Kartik Patwari[1], Hossein Sayadi[3], Setareh Rafatirad[4], Chen-Nee Chuah[1], Houman Homayoun[4]
[1]UC Davis, [2]University of California, Davis, [3]California State University, Long Beach, [4]University of California Davis

9:20AM
5C.2
Always be Pre-Training: Representation Learning for Network Intrusion Detection with GNNs
Zhengyao Gu[1], Diego Lopez[1], Lilas Alrahis[2], Ozgur Sinanoglu[2]
[1]New York University, [2]New York University Abu Dhabi

9:40AM
5C.3
NAND Flash-Based Digital Fingerprinting for Robust and Secure Hardware Authentication
Kamrul Hasan[1], Sara Tehranipoor[1], Nima Karimian[1], Surbhi Vasudeva[2]
[1]West Virginia University, [2]San Jose State University

10:00AM
5C.4
Intelligent Malware Detection based on Hardware Performance Counters: A Comprehensive Survey
Hossein Sayadi[1], Zhangying He[1], Hosein Mohammadi Makrani[2], Houman Homayoun[3]
[1]California State University, Long Beach, [2]University of California, Davis, [3]University of California Davis

SESSION 6A

Friday April 5

FAQ: FPGAs, Accelerators, Quantum

Chair: **Rasit Topaloglu**, topallabs & Marist College

10:45AM
6A.1
Emerging Reconfigurable Logic Device Based FPGA Design and Optimization
Sheng Lu, Liuting Shang, Sungyong Jung, Chenyun Pan
The University of Texas at Arlington

11:05AM
6A.2
A Low-Dissipation and Scalable GEMM Accelerator with Silicon Nitride Photonics
Venkata Sai Praneeth Karempudi[1], Sairam Sri Vatsavai[1], Ishan Thakkar[1], Oluwaseun Alo[1], Todd Hastings[1], Justin Woods[2]
[1]University of Kentucky, [2]Argonne National Lab

11:25AM
6A.3
QNSA: Quantum Neural Simulated Annealing for Combinatorial Optimization
Seongbin Kwon, Dohun Kim, Sunghye Park, Seojeong Kim, Seokhyeong Kang
Pohang University of Science and Technology

11:45AM
6A.4
QuEST: Quantum Circuit Output Estimation using Gaussian Distribution Analysis
Shamik Kundu, Navnil Choudhury, Kanad Basu
University of Texas at Dallas

12:05PM
6A.5
BMX-FPCA: 3D Beyond-Moore Flexible Field Programmable Crossbar Array Architecture
Hasita Veluri and Dilip Vasudevan
Lawrence Berkeley National Laboratory

SESSION 6B

Friday April 5

AI Accelerator Hardware Design

Chair: **Zhen Zhou**, Intel

10:45AM
6B.1
EASI-CiM: Event-driven asynchronous Stream-based Image Classifier with Compute-in-Memory kernels
Rahul Sreekumar[1], Minseong Park[1], Mohammad Nazmus Sakib[1], Bhupendra Singh Reniwal[2], Kyusang Lee[1], Mircea Stan[1]
[1]University of Virginia, [2]Indian Institute of Technology Jodhpur

11:05AM
6B.2
Temporal-encoded 6T-RRAM with Bidirectional Control for Future Neuromorphic Systems
Kang Jun Bai[1], Hao Jiang[2], Zhuwei Qin[2], Clare Thiem[1]
[1]Air Force Research Laboratory, [2]San Francisco State University

11:25AM
6B.3
Time-Domain-Based Non-volatile In-Memory Computing Architecture Using FeFETs for Binary Neural Network
Aditya Sharma, Vatsal Dixit, Dinesh Kushwaha, Nitanshu Chauhan, Vishal Saxena, Sudeb Dasgupta, Anand Bulusu
Indian Institute of Technology Roorkee

11:45AM
6B.4
DESPINE: NAS generated Deep Evolutionary Adaptive Spiking Network for Low Power Edge Computing Applications
Ajay BS[1], Phani Pavan Kambhampati[2], Madhav Rao[3]
[1]IntelTechnologyIndiaPvtLtd., [2]International Institute of Information Technology, Bangalore, [3]International Institute of Information Technology-Bangalore

SESSION 6C

Friday April 5

Quantum Computing

Chair: **Ahmedullah Aziz**, University of Tennessee, Knoxville

10:45AM
6C.1
Peephole Optimization for Quantum Approximate Synthesis
Joseph Clark and Himanshu Thapliyal
University of Tennessee

11:05AM
6C.2
Optimal quantum simulations of Hamiltonians with symmetries
Itay Hen and Amir Kalev
University of Southern California

11:25AM
6C.3
Continuous Variable Quantum Machine Learning
Kubra Yeter Aydeniz
MITRE Corporation

11:45AM
6C.4
A SPICE-based Emulator Framework for Quantum Error Correction Circuits using classical LC Resonators
Md Mazharul Islam[1], Md. Shafayat Hossain[2], Ahmedullah Aziz[3]
[1]The University of Tennessee, [2]Princeton University, [3]University of Tennessee, Knoxville

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- ***Advanced & 3D IC Packaging Technology***
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