Call for Papers

ISQED 2011, 12th International Symposium & Exhibits on

QUALITY ELECTRONIC DESIGN

March 14-16, 2011. Santa Clara, CA, USA

The International Symposium on Quality Electronic Design (ISQED) is the leading Electronic Design & Design Automation conference, aimed at bridging the gap among electronic design tools and processes, integrated circuit technologies, processes & manufacturing, to achieve design quality. ISQED is the pioneer and leading international conference dealing with design for manufacturability and quality issues front-to-back. ISQED emphasizes a holistic approach toward electronic design and intends to highlight and accelerate cooperation among the IC Design, EDA, Semiconductor Process Technology and Manufacturing communities. ISQED spans three days, Monday through Wednesday, in three parallel tracks, hosting over 100 technical presentations, several keynote speakers, panel discussions, workshops/ tutorials and other informal meetings. Conference proceedings CDs are published by IEEE and posted in the IEEE Xplore digital library. In addition, continuing the tradition of reaching a wider readership in the IC design community, ISQED will continue to publish special issues in leading journals. The authors of high quality papers will be invited to submit an extended version of their papers for the special IEEE journal issues, such as TCAD, etc.

Papers are accepted in the following areas

A pioneer and leading multidisciplinary conference, ISQED accepts and promotes papers related to the manufacturing, design and EDA. Authors are invited to submit papers in the various disciplines of high level design, circuit design (digital, analog, mixed-signal, RF), test & verification, design automation tools; processes; flows, device modeling, semiconductor technology, advance packaging, and biomedical & bioelectronic devices. The details of various topics of paper submission are as follows:

Design for Manufacturability/Yield & Quality (DFQ)

DFM/DFY/DFQ definitions, methodologies, matrices, and standards. Quality-based design methodologies and flows for custom, semi-custom, ASIC, FPGA, RF, memory, networking circuit, etc. Design flows and methodologies for SoC, and SiP. Analysis, modeling, and abstraction of manufacturing process parameters and effects for highly predictable silicon performance. Design and synthesis of ICs considering factors such as: signal integrity, transmission line effects, OPC, phase shifting, and sub-wavelength lithography, manufacturing yield and technology capability. Design for diagnosability, defect detection and tolerance; self-diagnosis, calibration and repair. Design and manufacturability issues for digital, analog, mixed signal, RF, MEMS, opto-electronic, biochemical-electronic, and nanotechnology based ICs. Redundency and other yield improving techniques. Global, social, and economic implications of design quality. Mask making methods and advances impacting manufacturability and yield.

Physical Design, Methodologies & Tools (PDM)

Physical design for manufacturing; Physical synthesis flows for correct-by-construction quality silicon, implementation of large SoC designs. Tool frameworks and data-models for tightly integrated incremental synthesis, placement, routing, timing analysis and verification. Placement, optimization, and routing techniques for noise sensitivity reduction and fixing. Algorithms and flows for harnessing crosstalk-delay during physical synthesis. Tool flows and techniques for antenna rule and electromigration rule avoidance and fixing. Spare-cell strategies for ECO, decoupling capacitance and antenna rule fixing. Physical planning tools for predictable power-aware circuits. Reliable clock tree generation and clock distribution methodologies for Gigahertz designs. EDA tools, design techniques, and methodologies, dealing with issues such as: timing closure, R, L, C extraction, ground/Vdd bounce, signal noise/cross-talk /substrate noise, voltage drop, power rail integrity, electromigration, hot carriers, EOS/ESD, plasma induced damage and other yield limiting effects, high frequency effects, thermal effects, power estimation, EMI/EMC, proximity correction & phase shift methods, verification (layout, circuit, function, etc.).

Design Verification and Design for Testability (DVFT)

Hardware and software, formal and simulation based design verification techniques to ensure the functional correctness of hardware early in the design cycle. DFT and BIST for digital and SoC. DFT for analog/mixed-signal ICs and systems-on-chip, DFT/BIST for memories. Test synthesis and synthesis for testability. DFT economics, DFT case studies. DFT and ATE. Fault diagnosis, IDDQ test, novel test methods, effectiveness of test methods, fault models and ATPG, and DPPM prediction. SoC/IP testing strategies. Design methodologies dealing with the link between testability and manufacturing.

EDA Methodologies, Tools, Flows & IP Cores; Interoperability and Reuse (EDA)

EDA tools addressing design for manufacturing, yield, and reliability. Management of design process, design flows and design databases. EDA tools interoperability issues and implications. Effect of emerging technologies, processes & devices on design flows, tools, and tool interoperability. Emerging EDA standards. EDA design methodologies and tools that address issues which impact the quality of the realization of designs into physical integrated circuits. IP modeling and abstraction. Design and maintenance of technology independent hard and soft IP blocks. Methods and tools for analysis, comparison and qualification of libraries and hard IP blocks. Challenges and solutions of the integration, testing, qualifying, and manufacturing of IP blocks from multiple vendors. Third party testing of IP blocks. Risk management of IP reuse. IP authoring tools and methodologies.

Robust & Power-conscious Devices, Interconnects, and Circuits (PCC)

Power-conscious design methodologies and tools; low power devices, circuits and systems; power-aware computing and communication; system-level power optimization and management. Design techniques for leakage current management.

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Emerging/Innovative Process & Device Technologies and Design Issues (EDT)

Emerging processes & device technologies and implications on IC design with respect to design's time to market, yield, reliability, and quality. Emerging issues in DSM CMOS: e.g. sub-threshold leakage, gate leakage, technology road mapping and technology extrapolation techniques. New and novel technologies such as SOI, Double-Gate (DG)-MOSFET, Gate-All-Around (GAA)-MOSFET, Vertical-MOSFET, strained CMOS, high-bandwidth metallization, 3D integrated circuits, nanoelectronic, biomedical & bioelectronic devices, etc.

Package - Design Interactions & Co-Design (PDI)

Concurrent circuit, package, and PCB/PWB design and effect on quality. EDA tools and methodologies dealing with the IC Packaging electrical and thermal modeling and simulation for improved quality of product. SoC versus system in a package (SiP): design and technology solutions and tradeoffs; MCM, BGA, Flip Chip, TSV, and other innovative packaging techniques for various applications such as mixed-signal and RFIC.

Design of Reliable Circuits and Systems (DFR)

Device and process reliability issues and effect on design of reliable circuits and systems. ESD design for digital, mixed signal and RF applications. Exploration of critical factors such as noise, substrate coupling, cross-talk and power supply noise. Significance and trends in process reliability effects such as gate oxide integrity, electromigration, ESD, etc., and their relation to electronic design.

System-level Design, Methodologies & Tools (SDM)

Emerging system-level design paradigms, methods and tools aiming at quality. ESL design process and flow management. System-level design modeling, analysis, synthesis, estimation and verification for correct high-quality hardware/software systems. Development of reliable, responsive, secure, and defect-tolerant systems. New concepts, methods and tools addressing the hardware and system design complexity, multitude of aspects, manufacturability, and usage of technology information and manufacturing feedback in the system-, RTL- and logic level design. The influence of the nanometer technologies' issues on the system-, RTL- and logic-level design. System-level trade-off analysis and multi-objective (yield, power, delay, area …) optimization. Effective and efficient development, implementation, analysis and validation of large SoCs integrating IP blocks from multiple vendors. Global, social, and economical implications of Electronic System and Design Quality. Emerging standards and regulations influencing system quality.

Submission of Papers

Paper submission must be done on-line through the conference web site at **www.isqed.org**. The guidelines for the final paper format are provided on the conference web site . Authors should submit FULL-LENGTH, original, unpublished papers (Minimum 4, maximum 8 pages) along with an abstract of about 200 words. To permit a **blind review**, **do not** include name(s) or affiliation(s) of the author(s) on the manuscript and abstract. The complete contact author information needs to be entered separately. Please check the as-printed appearance of your paper before sending your paper. In case of any problems email isqed2011@isqed.org. Please note the following important dates:

Paper Submission Deadline	September 30, 2010
Acceptance Notifications	November 23, 2010
Final Camera-Ready paper	January 10, 2011

www.isqed.org

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Quality Electronic Design
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