"12th International Symposium on Quality Electronic Design (ISQED2011)

For how much longer can Moore's Law hold?

R. Fabian Pease
Stanford University, CA 94305
Pease@stanford.edu

Why Moore's Law is important.

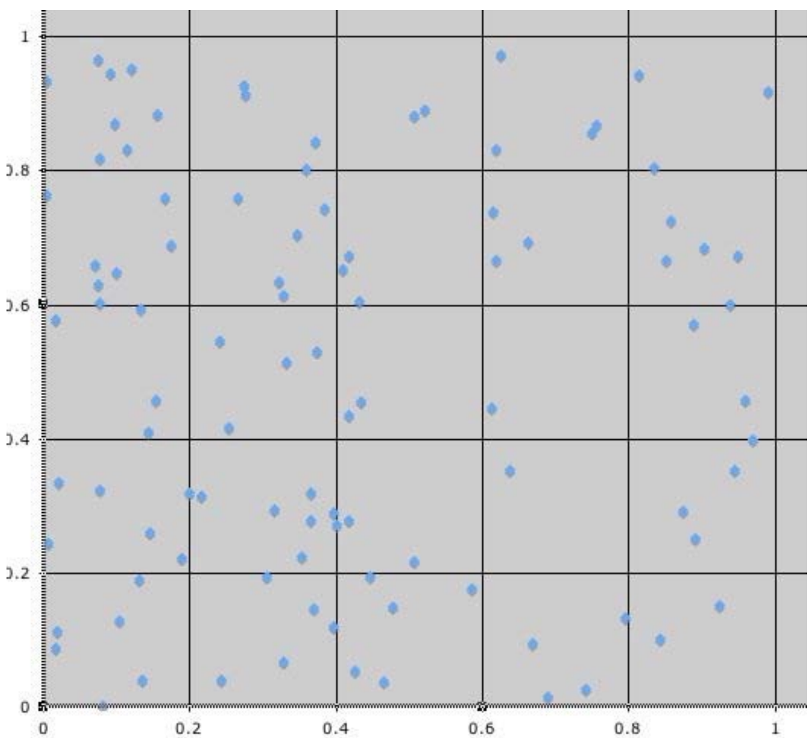
Its not just the transistors it's the wiring.

Limited by: (Design) ? *no*
Defects ? *no longer*
Lithography (Patterning)?

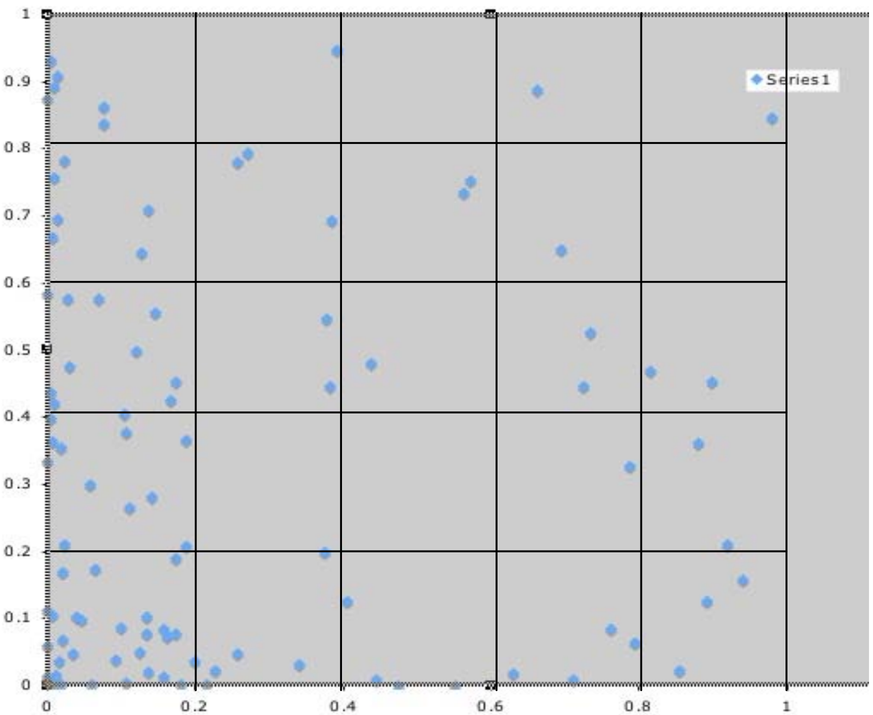
‘64 bits is probably beyond the limit of useful integration’

J. A. Morton, VP Electronics Technology, Bell Labs circa 1969, quoted by C. G. B Garrett

100 defects Poisson distributed among 25 die



100 defects distributed among 25 die non-stationarily



Mid 70’s

Yields <50%

LSI had arrived (4KDRAM), Zilog Z80

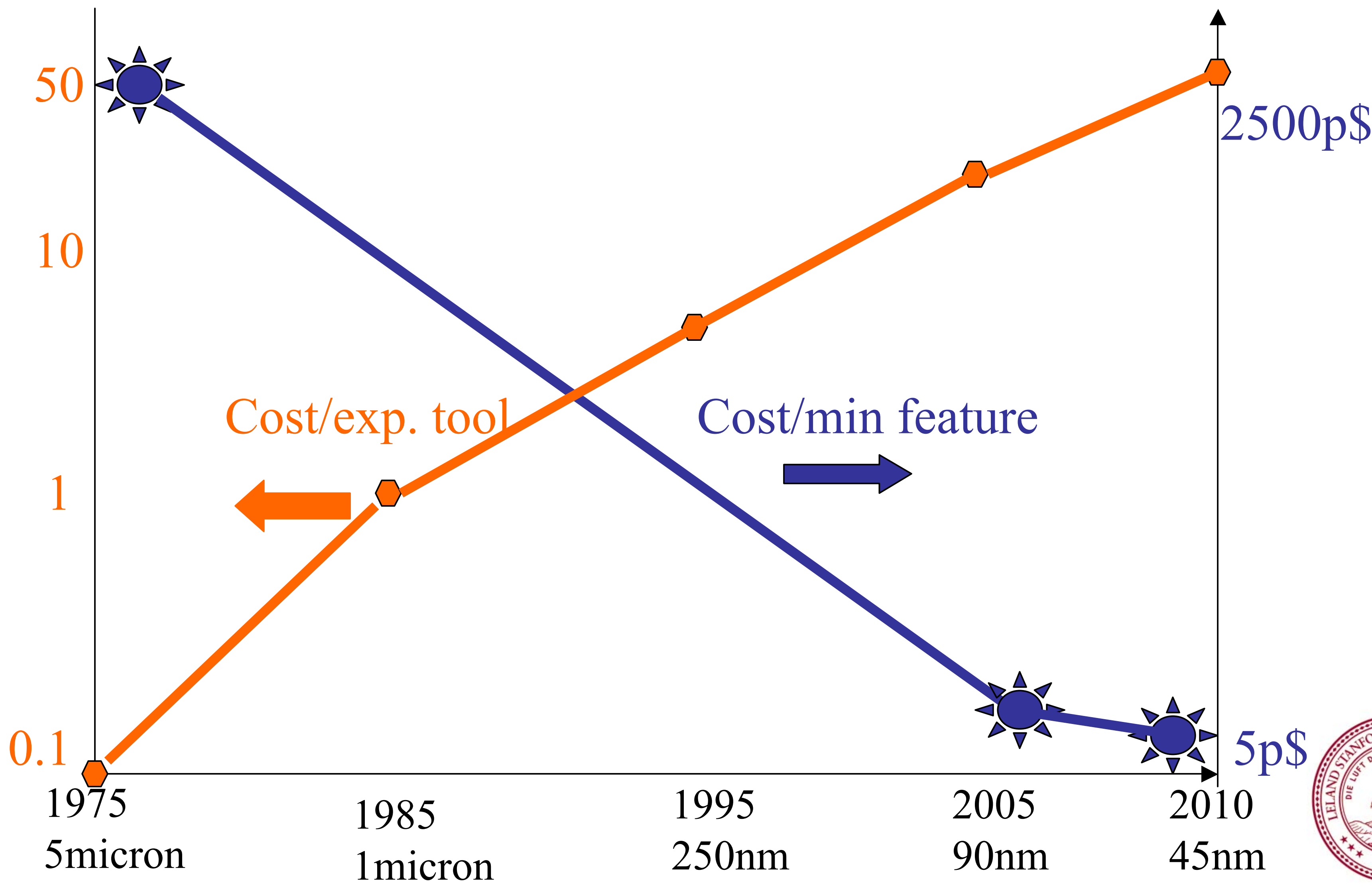
Tohoku University, Prof. Ohmi,

‘solved’ the defect problem

Professor Tadahiro Ohmori, New Industry Creation Hatchery Center, Tohoku University

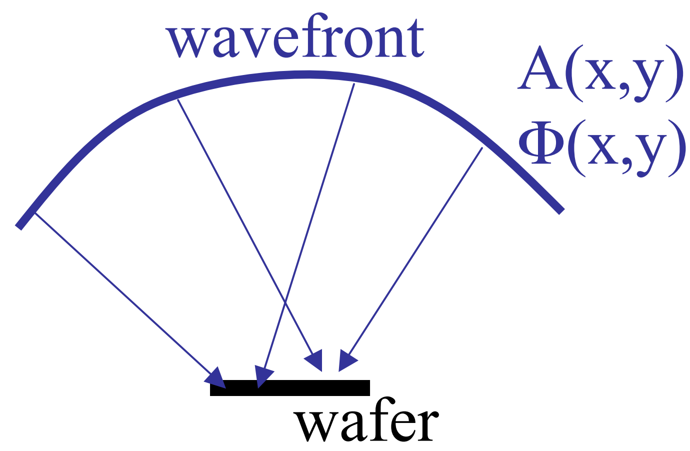
That left lithography as the key pacing technology

‘Everything gets better as we go smaller’



But now we are (getting) stuck

- •Optical lithography is used for manufacture with mfs=wavelength/6
  - •All forms of cheating being employed
    - •RET
    - •Immersion
    - •Double exposure
    - •Double patterning
    - •Design for lithography
  - •Cost/mf may not continue to decrease



- •EBL
  - •Still too slow
- •EUVL
  - •Still not ready
- •NanoPrinting
  - •Curiously downplayed (defects cited as drawback)

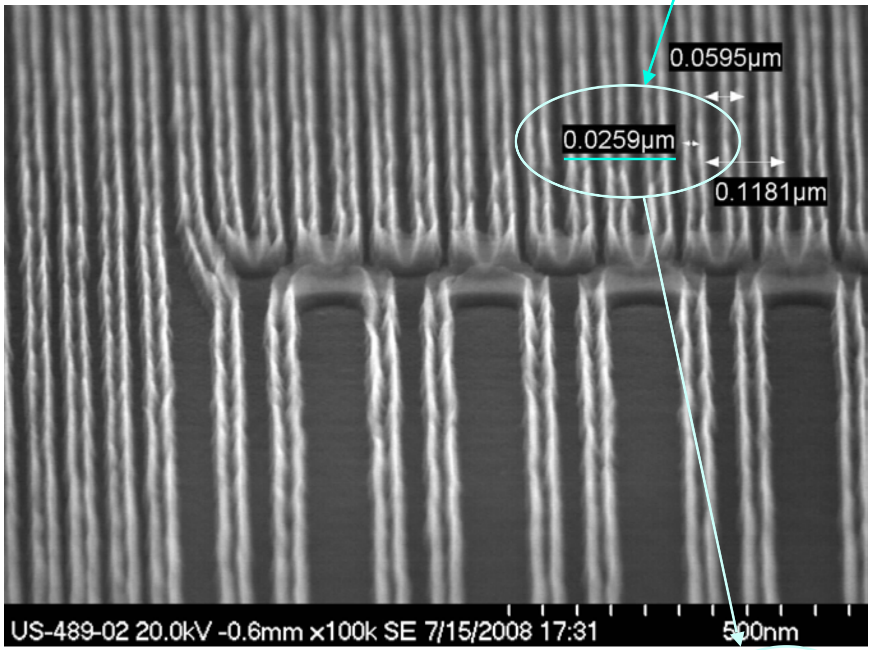
Beyond 2015 - 2017

193i SE	*SE*	*PD P/2*	*PD P/2*	*PD P/4*
32nm	**22nm**	**15nm**	**11nm**	**<u>7nm</u>**
P=112.5nm *0.71		***0.71**	***0.71**	***0.71 = 28nm**

One 193i Expose/1 Mask, several Extra Dep/Etch and Cleans steps.
Nothing Heroic, including added processing cost.

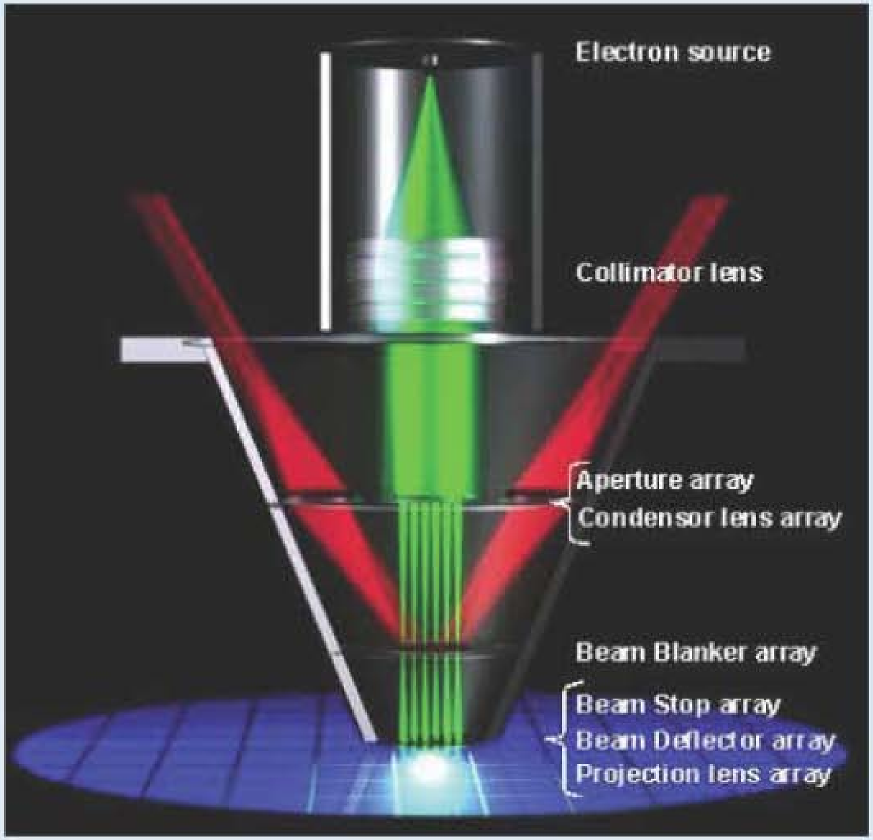
What have we got that is better to replace this?

***ITRS 2008 Reference*:**



Year of Production	2013	2015	2017	2019	2021
MPU Metal 1 Pitch *nm*	64	50	40	31.8	25.2

MAPPER builds a system with 13,000 parallel electron beams for 10 wph



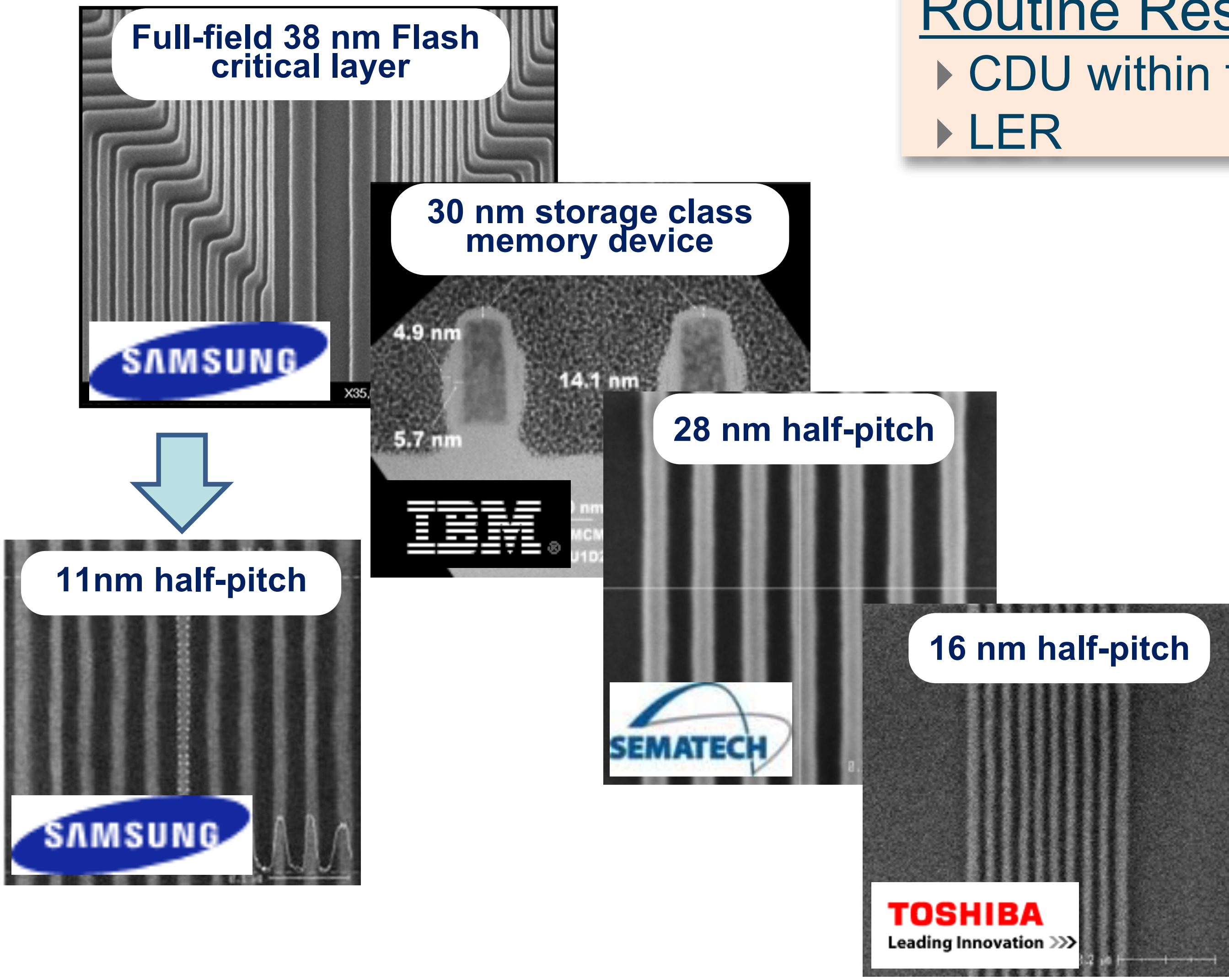
Key numbers 22nm node:

	HVM	pre-alpha
#beams and data channels	13,000	110
Spotsize:	25 nm	35 nm
Beam current:	13 nA	0.3 nA
Datarate/channel	3.5 Gbs	20 MHz
Acceleration voltage	5 kV	5 kV
Nominal dose	30 $\mu C/cm^2$	30 $\mu C/cm^2$
Throughput @ nominal dose	10 wph	0.002 wph
Pixel size @ nominal dose	3.5nm	2.25 nm
Wafer movement	Scanning	Static

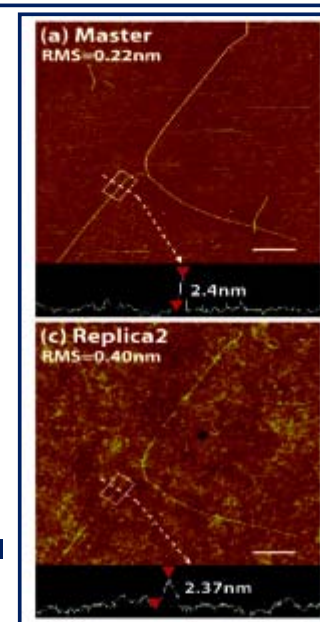
Imprint Evaluations

Routine Results:

- CDU within field <1.5nm
- LER <2.0nm



~2.4 nm Feature
(Rogers et al, Illinois)




EUV

Why go smaller?

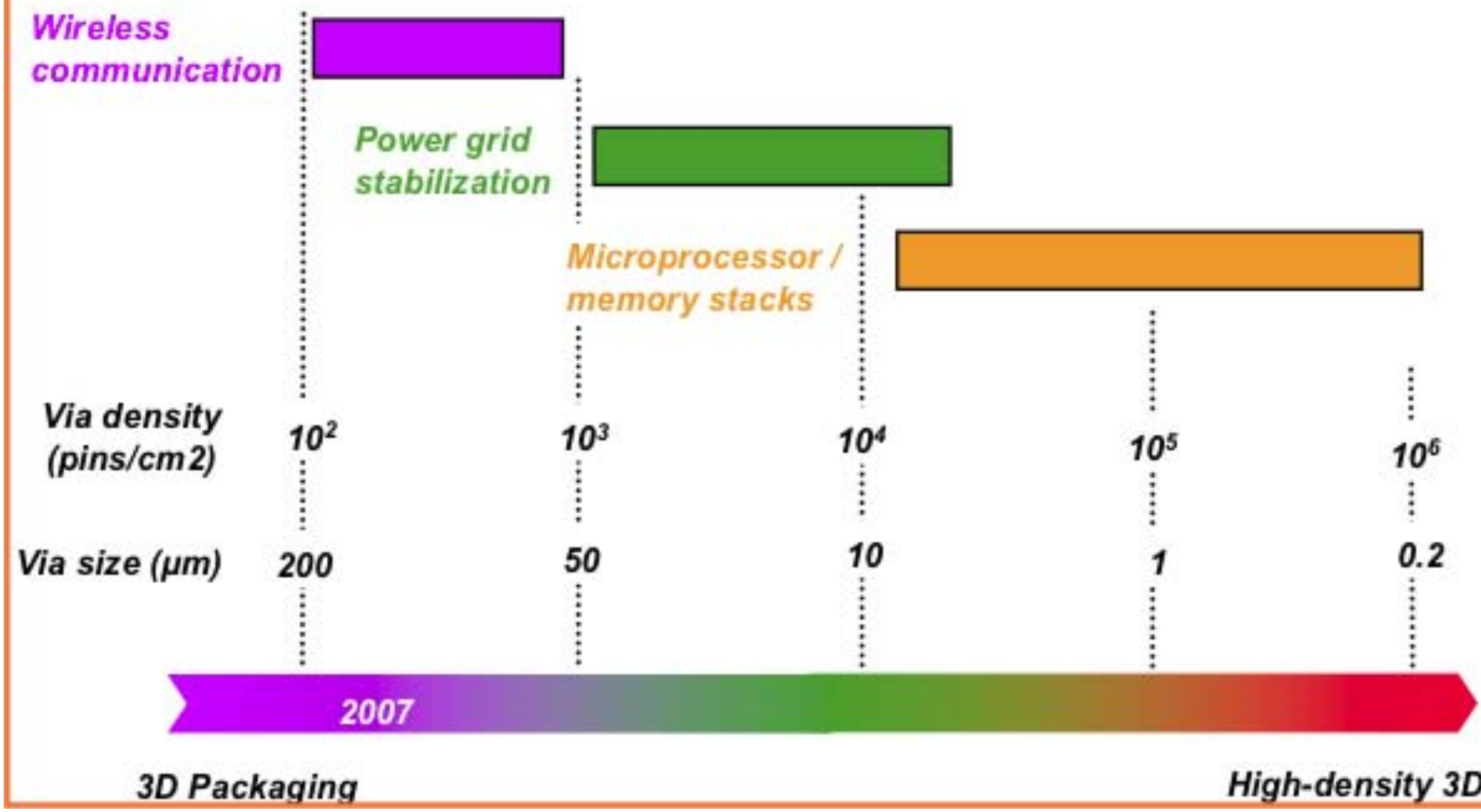
- Do transistors deliver more computation as features shrink below 30nm?
- Inerconnects get worse (L,C, p.u.l. constant, R p.u.l. increases). AND length tends to be a function more of chip size than gate electrode width
- Why not go 3-D (we already are in a ‘disruptive’ sense). Alleviates the interconnect challenge

Avoid the topological tyranny of all transistors in one plane. Go upwards

- 3-D wiring enabled by CMP (been here since the 90's)
- 3-D arrays of transistors (3-DIC) comes in various flavors:
  - Chip stacking (already here)
    - Edge connected
    - Area connected using TSV's
  - Wafer Stacking (IBM, Tezzaron, MIT Lincoln Lab)
  - Monolithic (Stanford University)

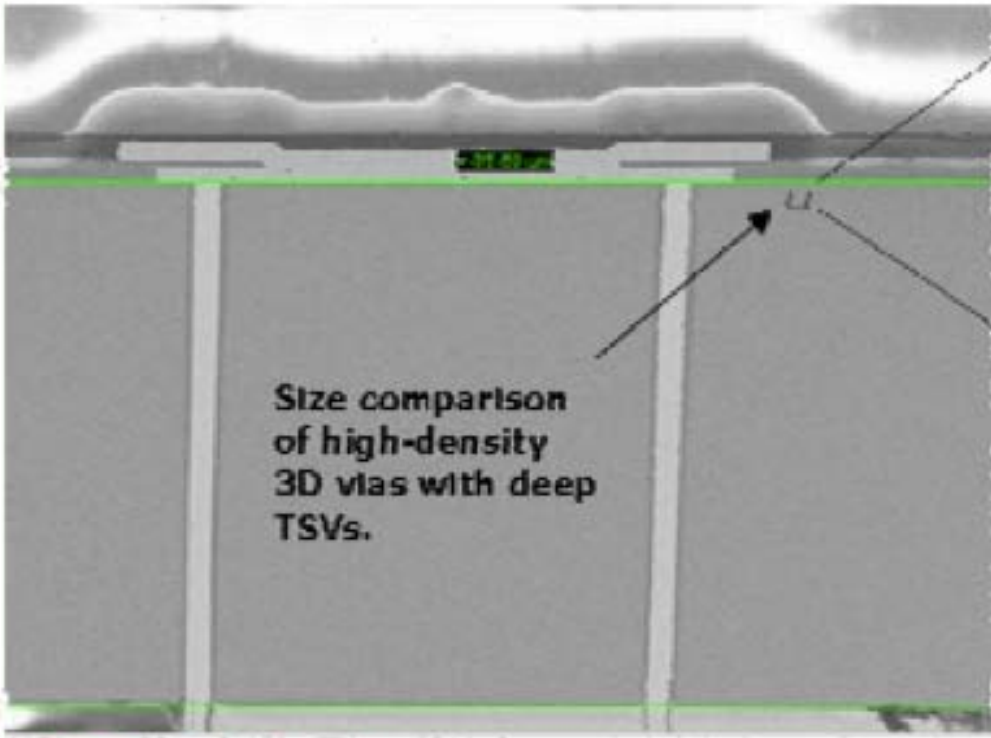
IBM: 3D ICs Roadmap

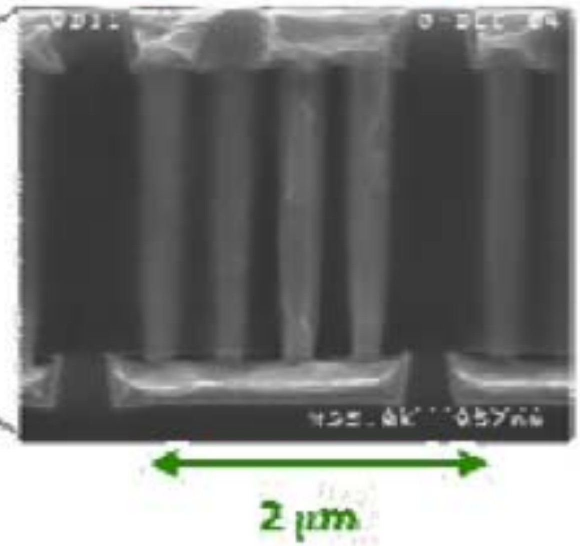
3D integration will be applicable a broad range of technologies and applications, from wireless communication to multi-core microprocessors:



IBM: 3D vias specifications

IBM (US) has developed different type of vias corresponding to different applications:





- *3D Packaging via process*

→ Application: wireless communications (SiGe power amplifiers) to reduce power consumption

→ Via diameter ~ 50 – 100 µm

→ Interconnect density ~ 10^2 pins/cm2

- *High-density 3D via process*

→ Application: cache memory stack on microprocessors to enhance computing performances

→ Via diameter < 1 µm

→ Interconnect density > 10^5 pins/cm2

Courtesy of IBM

Tezzaron 3DIC Technology

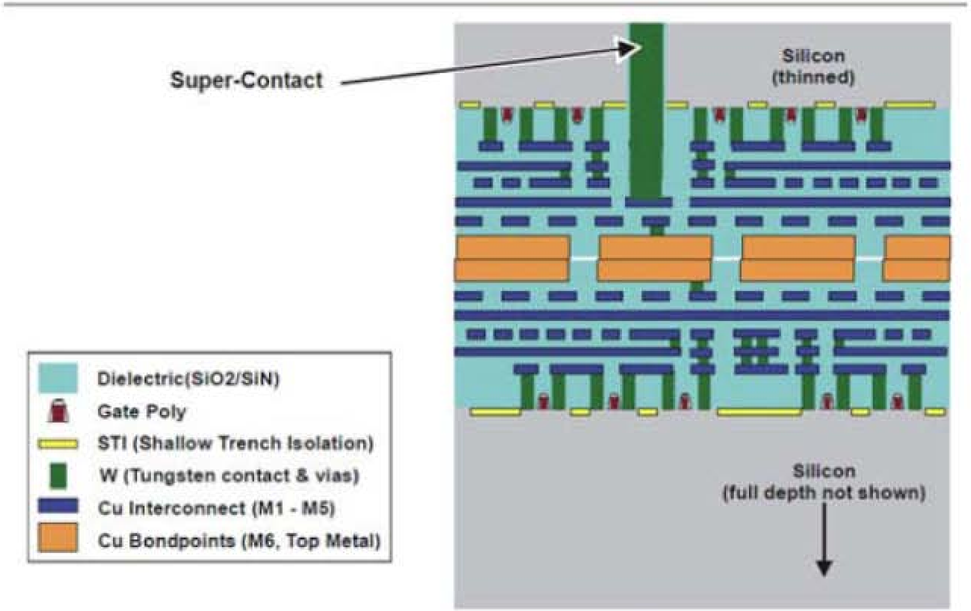
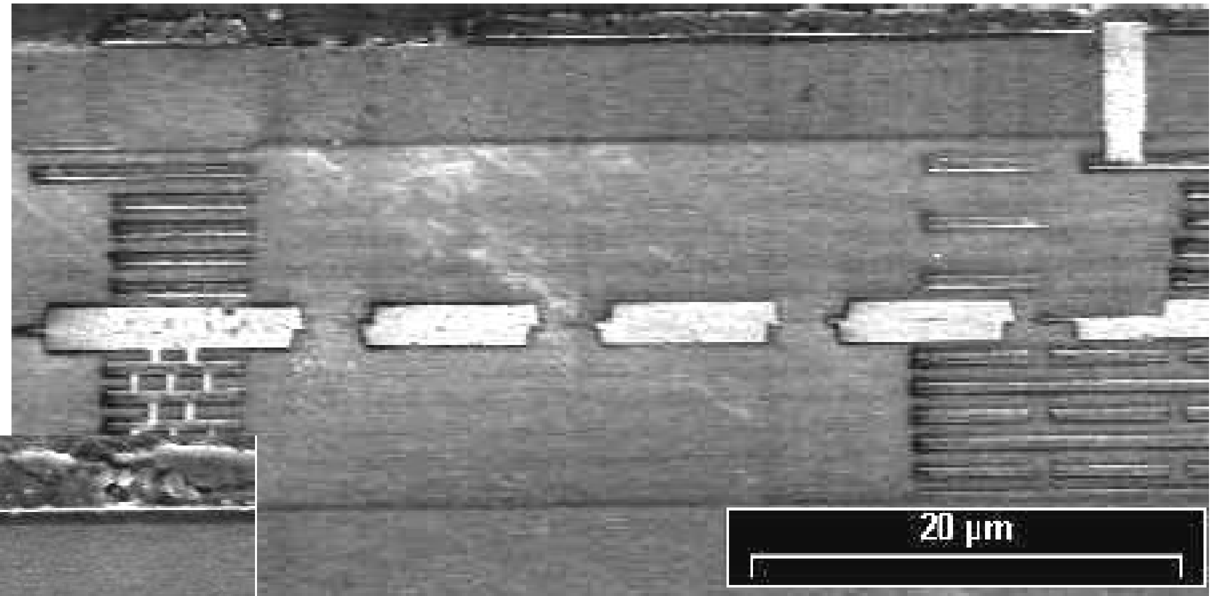


Figure 1 – Cross-section diagram of two bonded wafers after thinning

Top Si typically thinned to < 10 um

Face-to-face Cu thermo-compression bonding

Two face-to-face bonded 130 nm bulk CMOS tiers



re 5 – SEM* photo of a two-wafer stack.

Tezzaron FaStack® Technology

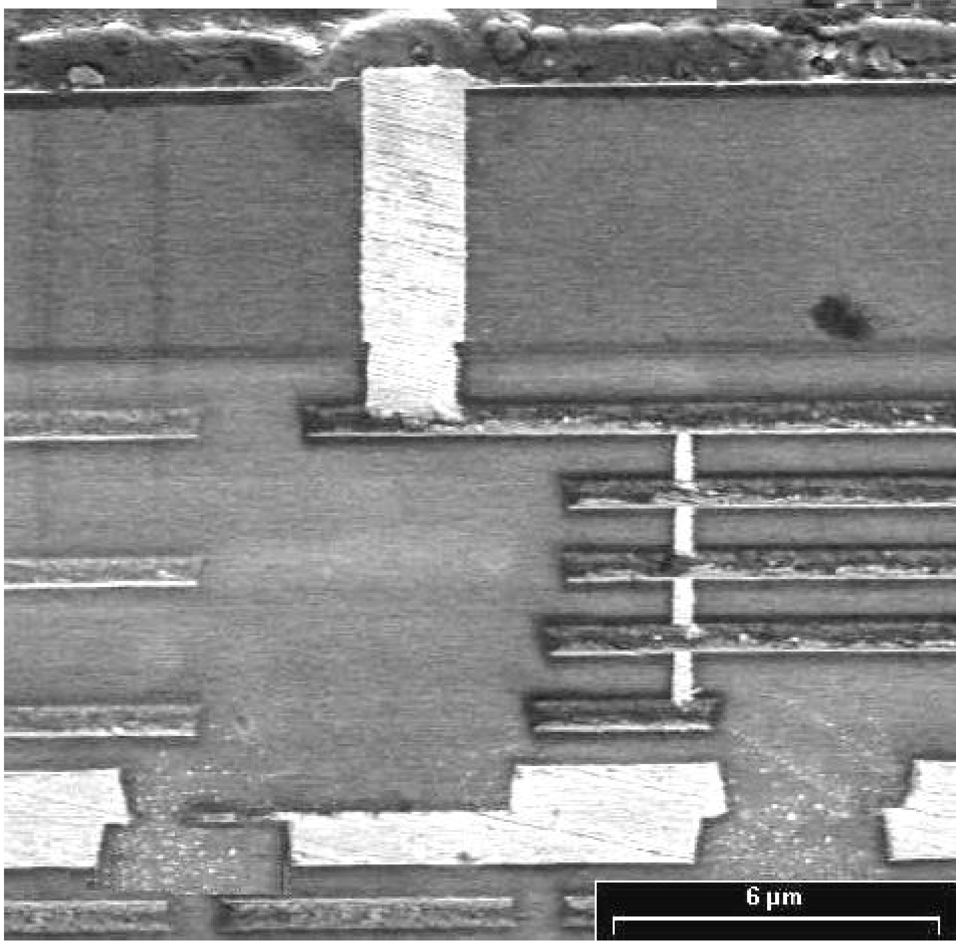
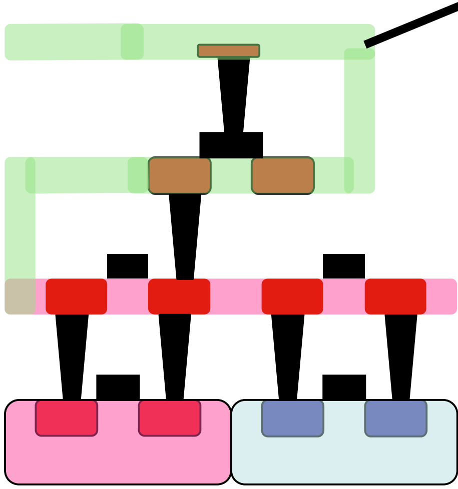
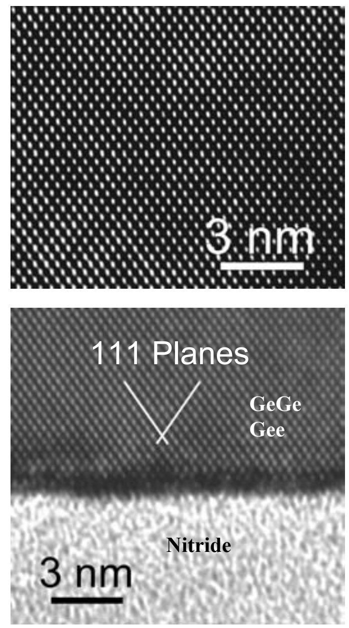


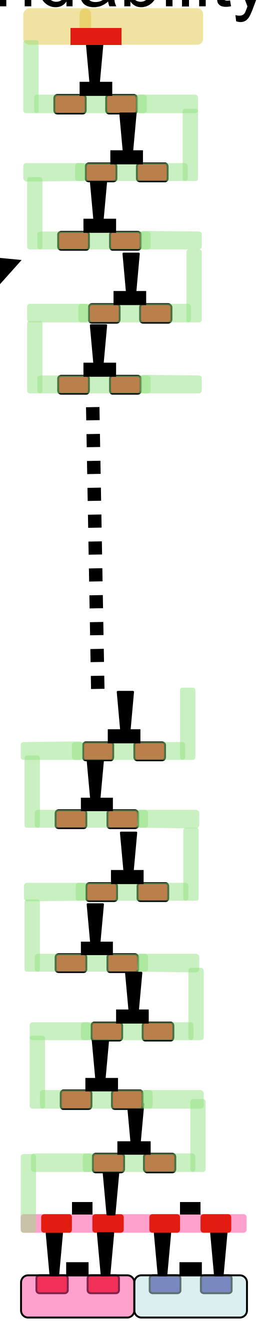
Figure 6 – SEM photo close-up of a Super-Contact.

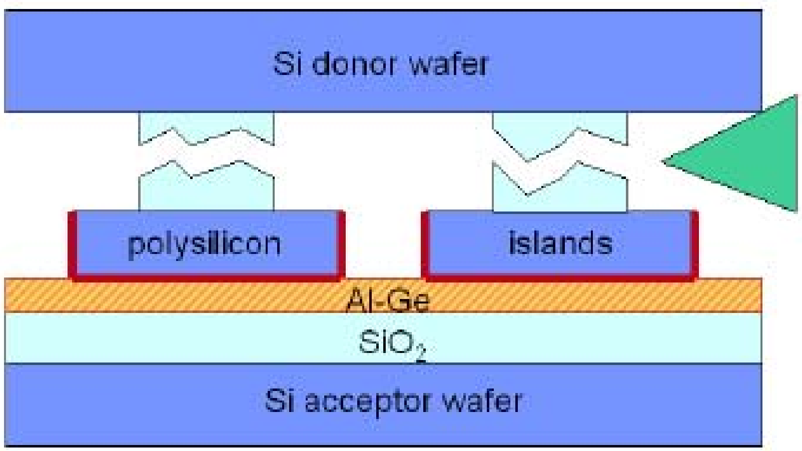
3-D IC's with unlimited upward extendability

Stanford University team









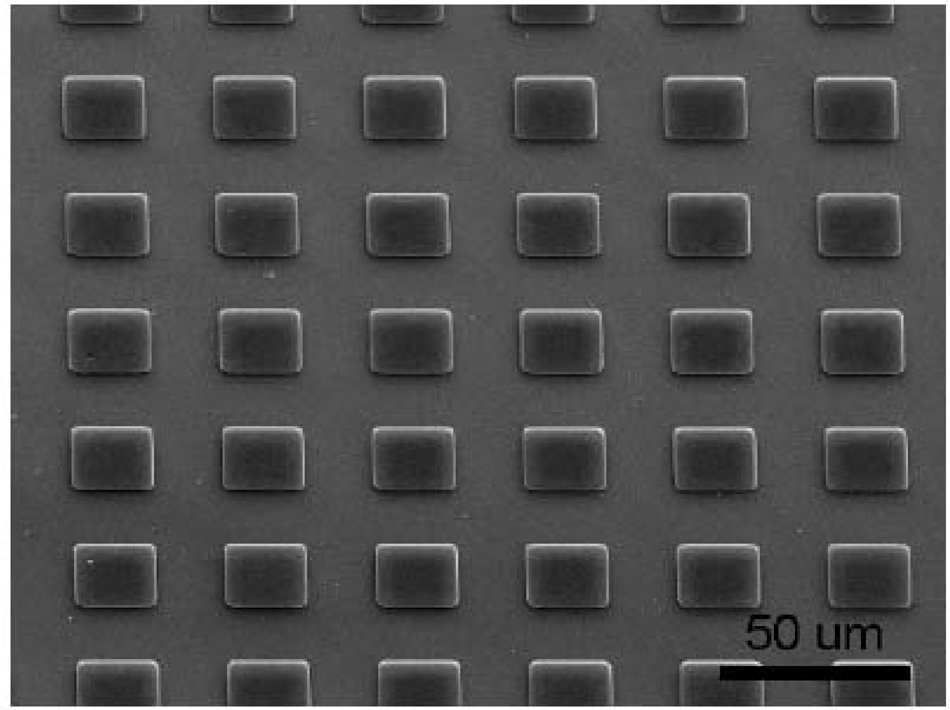
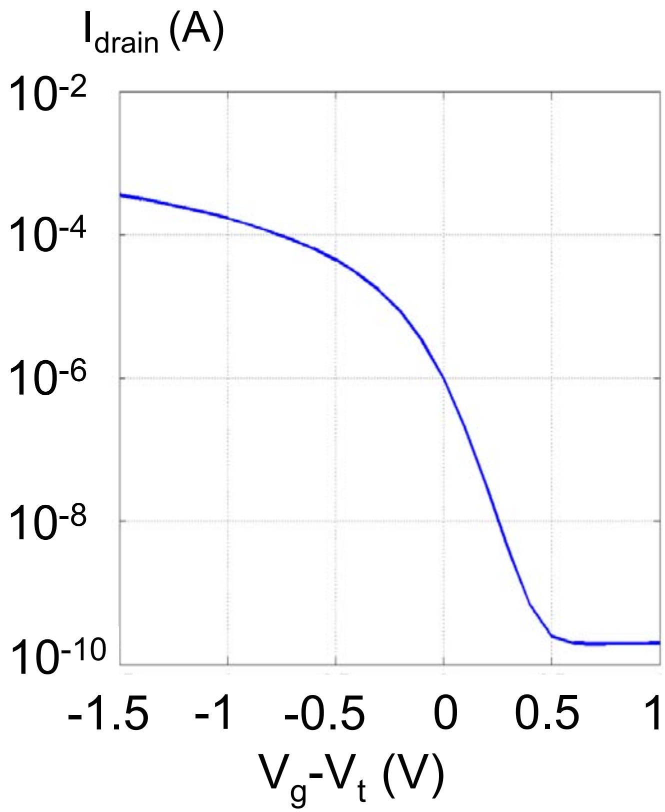


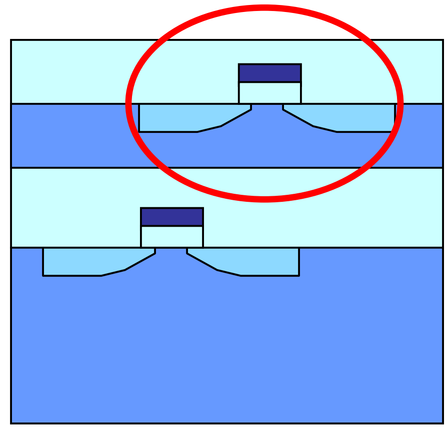
Fig. 6. SEM of an array of polysilicon islands attached to a SiO_2 substrate using Al-Ge eutectic bonding at 435 °C. The excess Al-Ge in between the islands has been etched away.

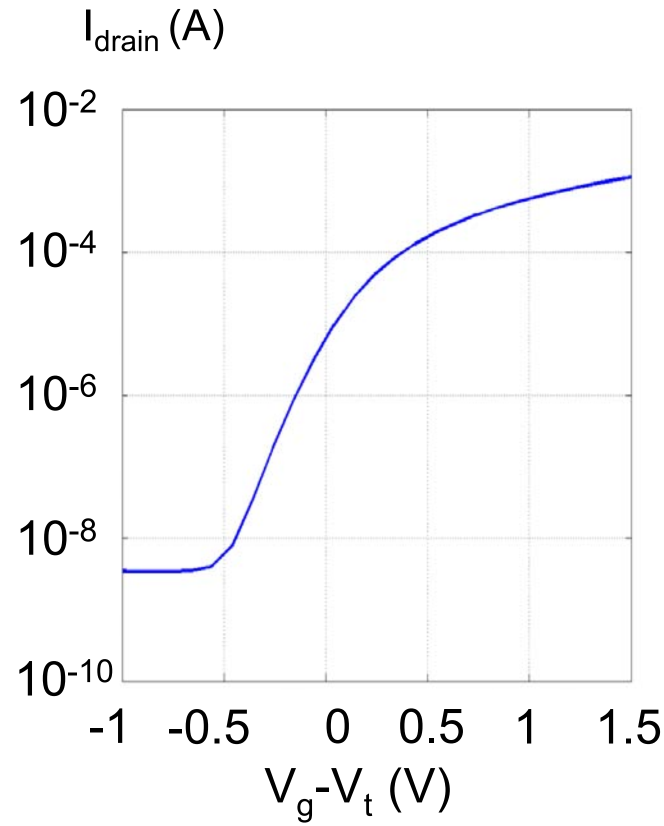
Filip Crnogorac, Stanford University

Process to fabricate transistors on the upper levels

(Rajendran, PhD thesis, 2006)







Dopant activation – Laser annealing (M. O. Thompson, Cornell Univ.)

Gate dielectric formation – LPCVD

Complete melting of implanted regions is necessary to avoid parasitic resistance and poly depletion.

Summary

- Quite a bit longer
- And it's important that it does continue