Beyond 28nm: New Frontiers and Innovations in Design For Manufacturability at the Limits of the Scaling Roadmap

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GLOBALFOUNDRIES

Outline

Challenges

- Variability and the Limits of IC Geometrical Scaling
- Methodology Innovation in Design for Manufacturing

Solutions

- Advanced Rule-Based Verification (Yield Analysis and Yield Enhancement)
- Novel Flow: DRC+
  - 2D Shapes Pattern-Matching Based Physical Design Verification
  - Model Accuracy and Full-Chip Performance without Compromise
- Si-Accurate Model-Based Printability Verification: enabling special ‘tech-cell’ constructs

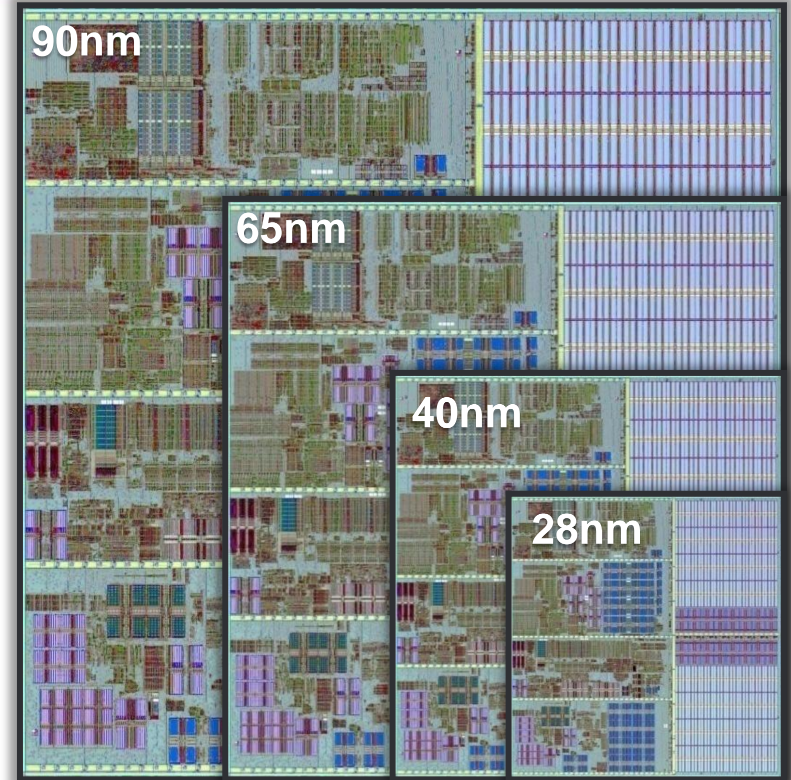
Manufacturing: closing the variability loop

- Design-Enabled Manufacturing:
  - Faster Yield Ramp and Foundry Customer Value

IC Integration State of the Art (today) Scaling and Device Density

Gate First HKMG

- 28nm "Gate First" provides true scaling (relative to 40nm)
  1. ~100% density increase
  2. Up to 50% increased speed and 50% reduction in energy/switch
  3. Sustains 40nm Layout Style Advantages: Bi-directional Poly, Poly Jogs, Large Caps
  4. 10-20% Smaller Die Relative to 28nm "Gate Last"

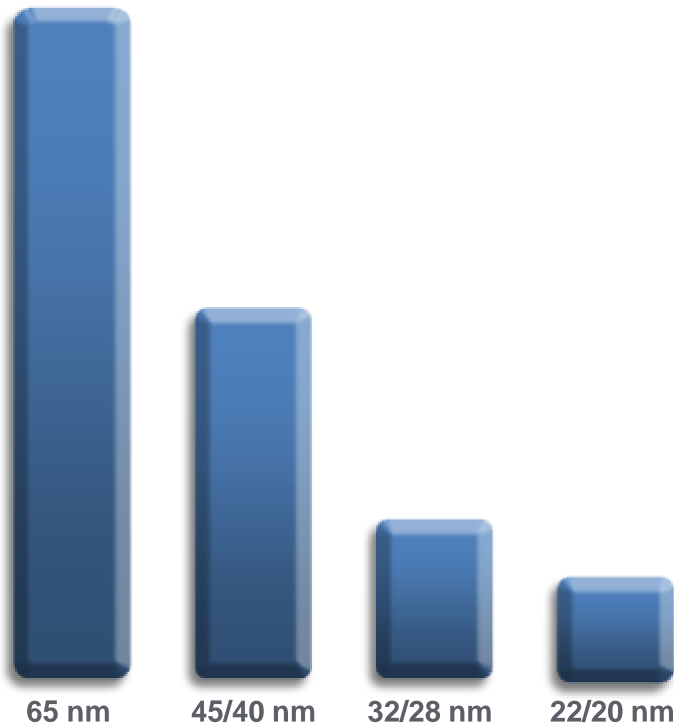


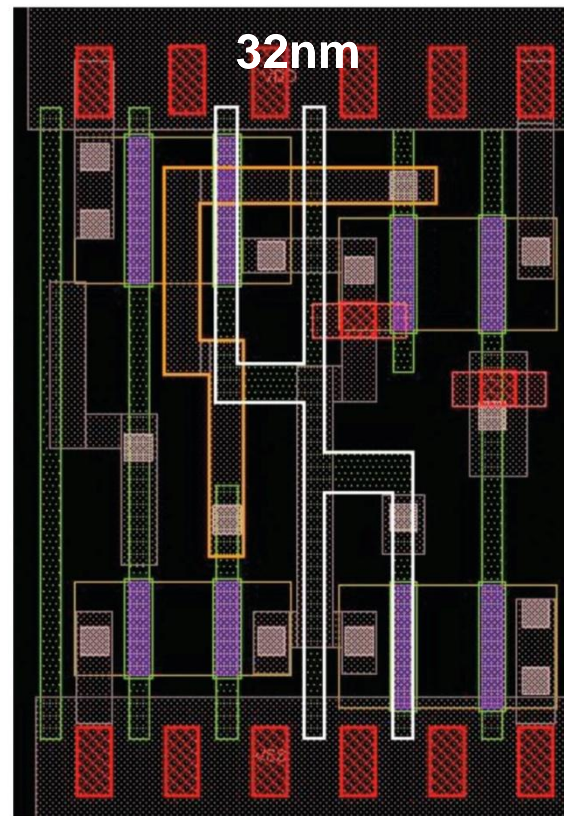
Process	90nm	65nm	40nm	28nm
Device Density	1	2	5	10
Normalized Power per gate	1	0.6	0.36	0.22

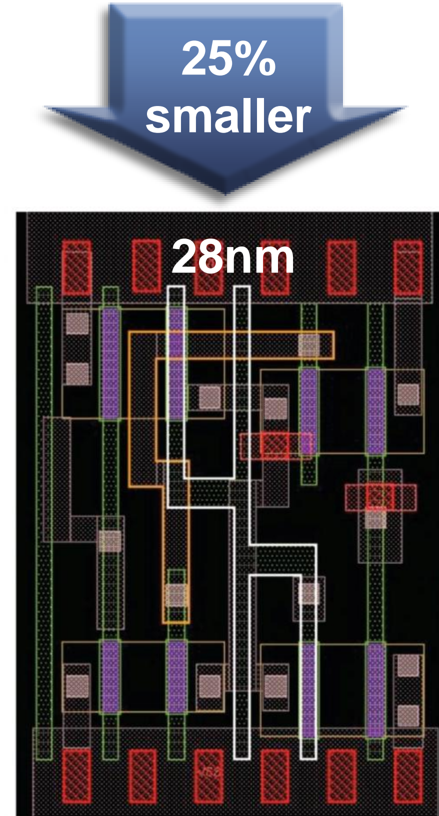
Key Technology Parameters: Innovation and Time-to-Volume

Number of tape-outs is decreasing …

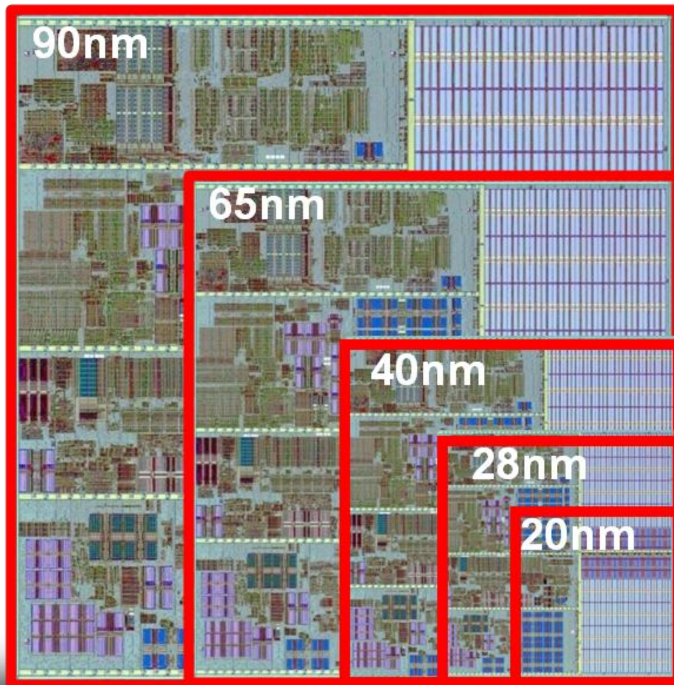
…but advanced technology continues to drive innovation, provide new value and volume is increasing





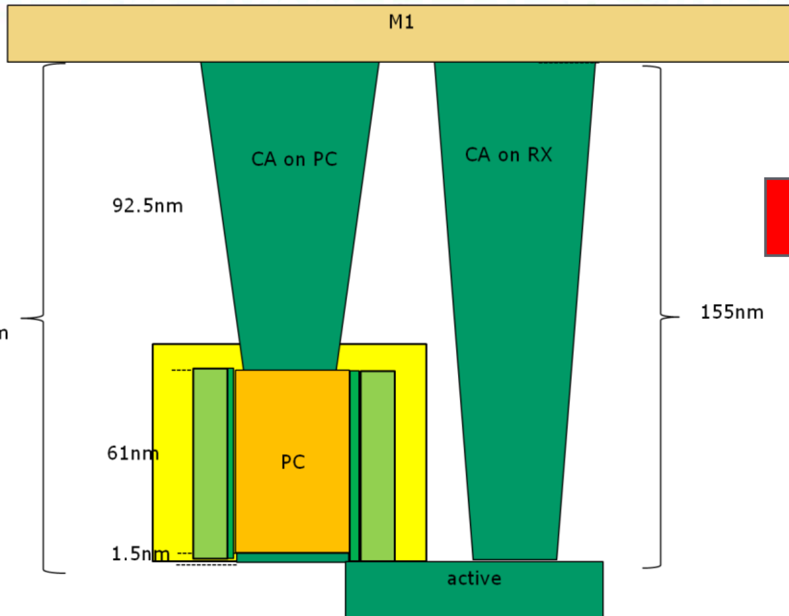


20nm: Scaling and Integration Continue



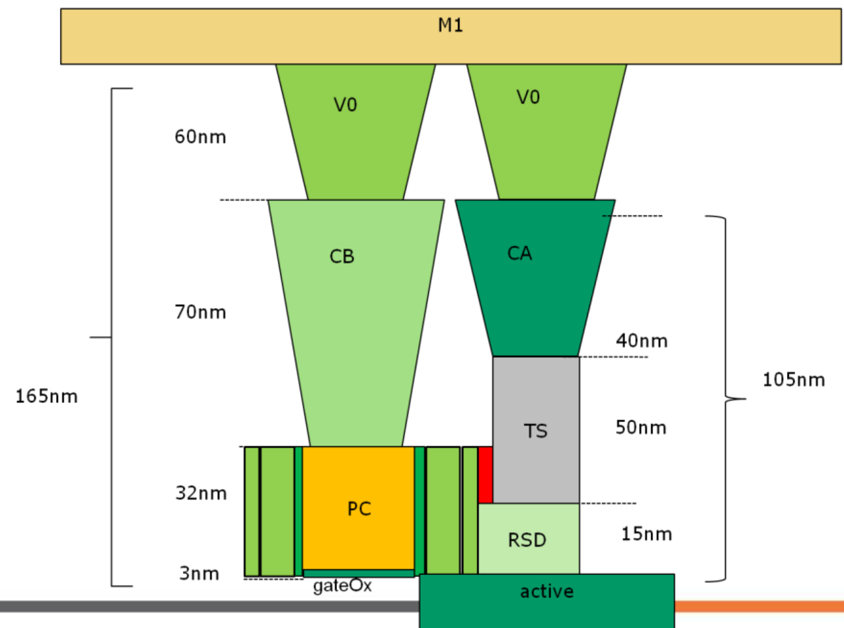
Process	90nm	65nm	40nm	28nm	20nm
Device Density	1	2	5	10	20
Normalized Power per Gate	1	0.6	0.36	0.22	0.14

Disruptive Transition: New Integration Schemes



28nm
Below M1:
- 2 vias
- one PC, one RX

Nxtgrd size: 19M
Carac. Time: 35h



20nm
Below M1:
- 6 vias
- 3 PC, 3 RX, CA, CB, TS

Nxtgrd size: **147M**
Carac. Time: **150h**

Tomorrow's Lithography: Tomorrow

Extreme Ultraviolet (EUV)

- Continuing to drive collaborative R&D
- Early era:1990-2000
  - Founding member of EUV LLC
  - Demonstrated fundamental capabilities
- Today: 2001-2010
  - 2008 SPIE: first full-field EUV patterning on 45nm test chip
  - >60 EUV masks shipped by Dresden mask house
  - Leading efforts to address Line Edge Roughness (LER)
- Tomorrow: 2012-14 and beyond
  - Will be one of early customers for production-level EUV tools

EUV mask produced at AMTC

Alpha Demo Tool at CNSE Albany

Lithographic Scaling Limits

$$MinPitch = \frac{2 \cdot k_1 \cdot \lambda}{NA}$$

193 nm

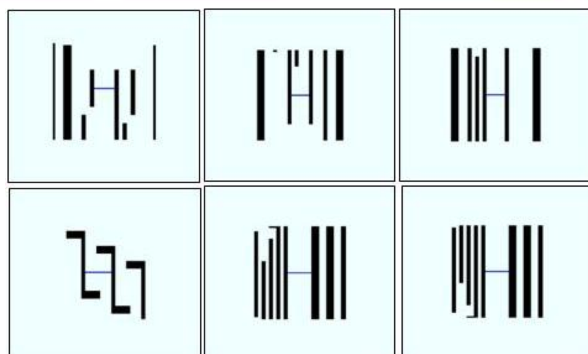
1.35 (max)

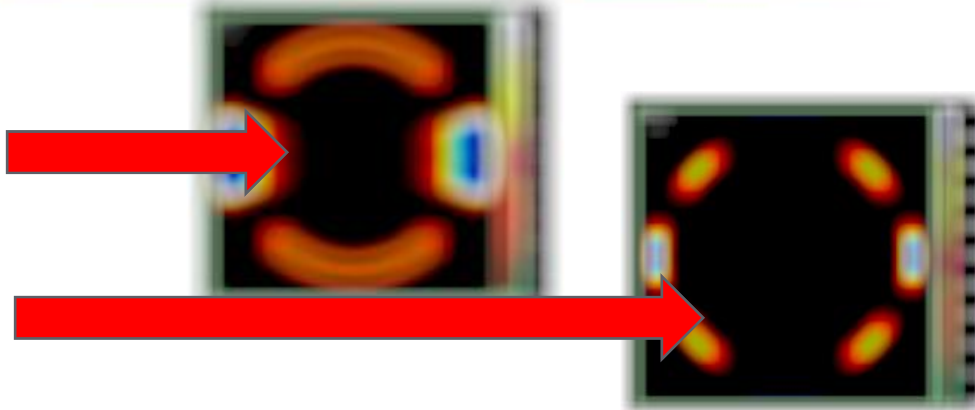
Technology Scaling requires increased process complexity:
i.e. reduction in $\boldsymbol{k_1}$ factor (theoretical min=0.25)

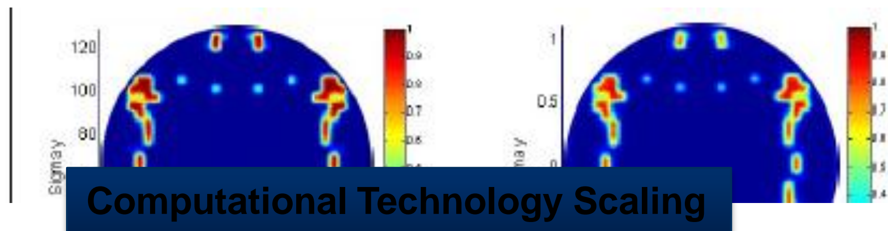
Computational Technology Scaling:
Systematic reduction of k_1 factor by rigorous **Co-Optimization** of:
(1) Physical Design (Layout, Design Rules, Place and Route)
(2) Process (Illumination, Lithography, Mask RET, OPC, etc.)

Computational Scaling is *also* known as: Design-Process-Technology Co-Optimization

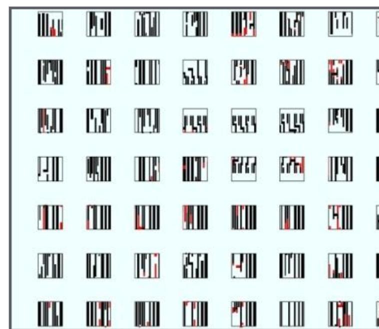
From 28 to 20nm Enablement: SMO Source-Mask Optimization

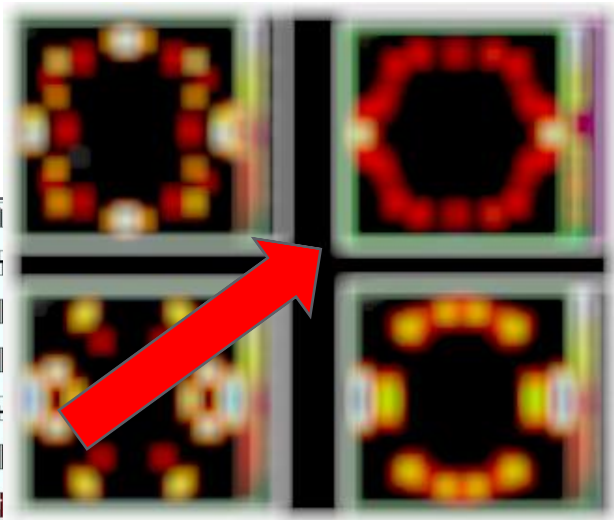






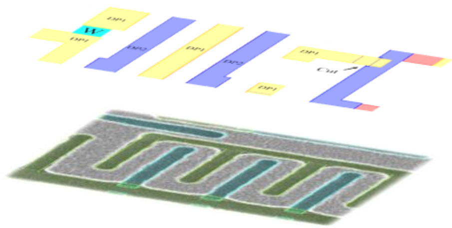
- Algorithm:
  - Optimize illumination source **parameters** based on a library of layout features (1D, 1.5D, 2D)

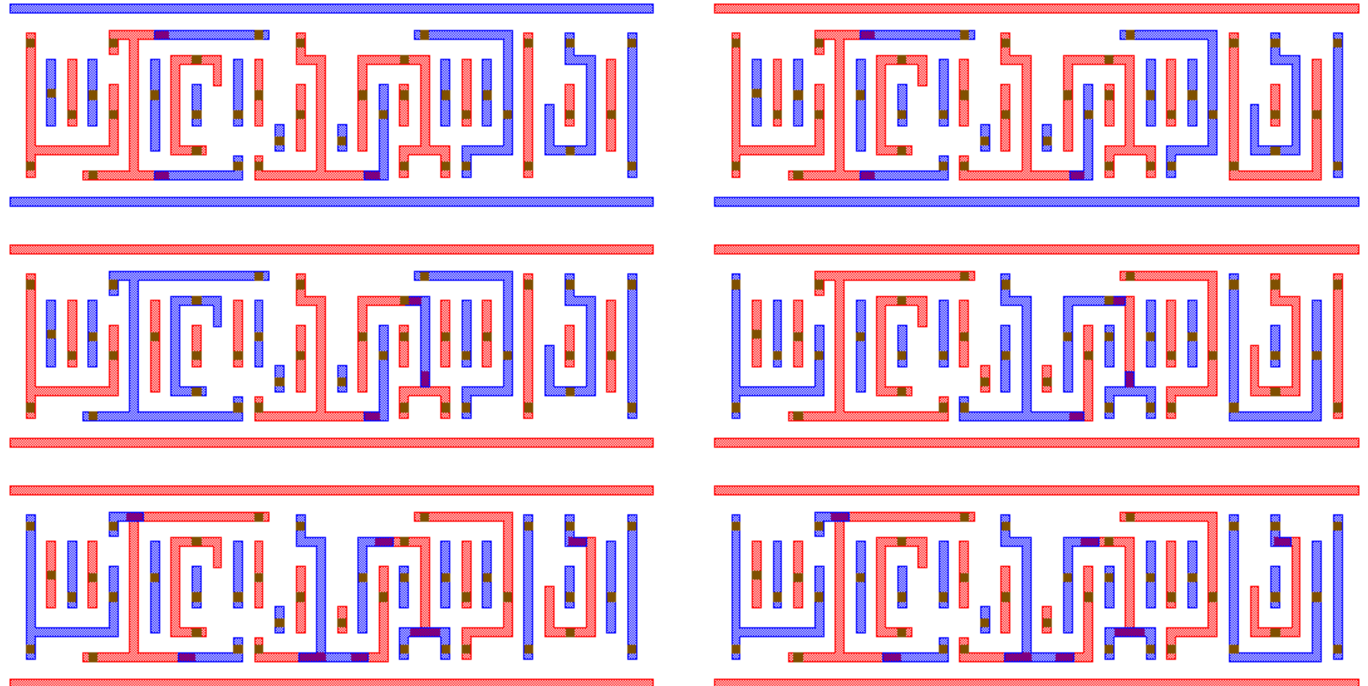




20nm Enablement: Double Patterning and Layout Decomp

- Double Patterning – to pattern sub 80nm features
  - Decomposition tools and algorithms
  - Stitching



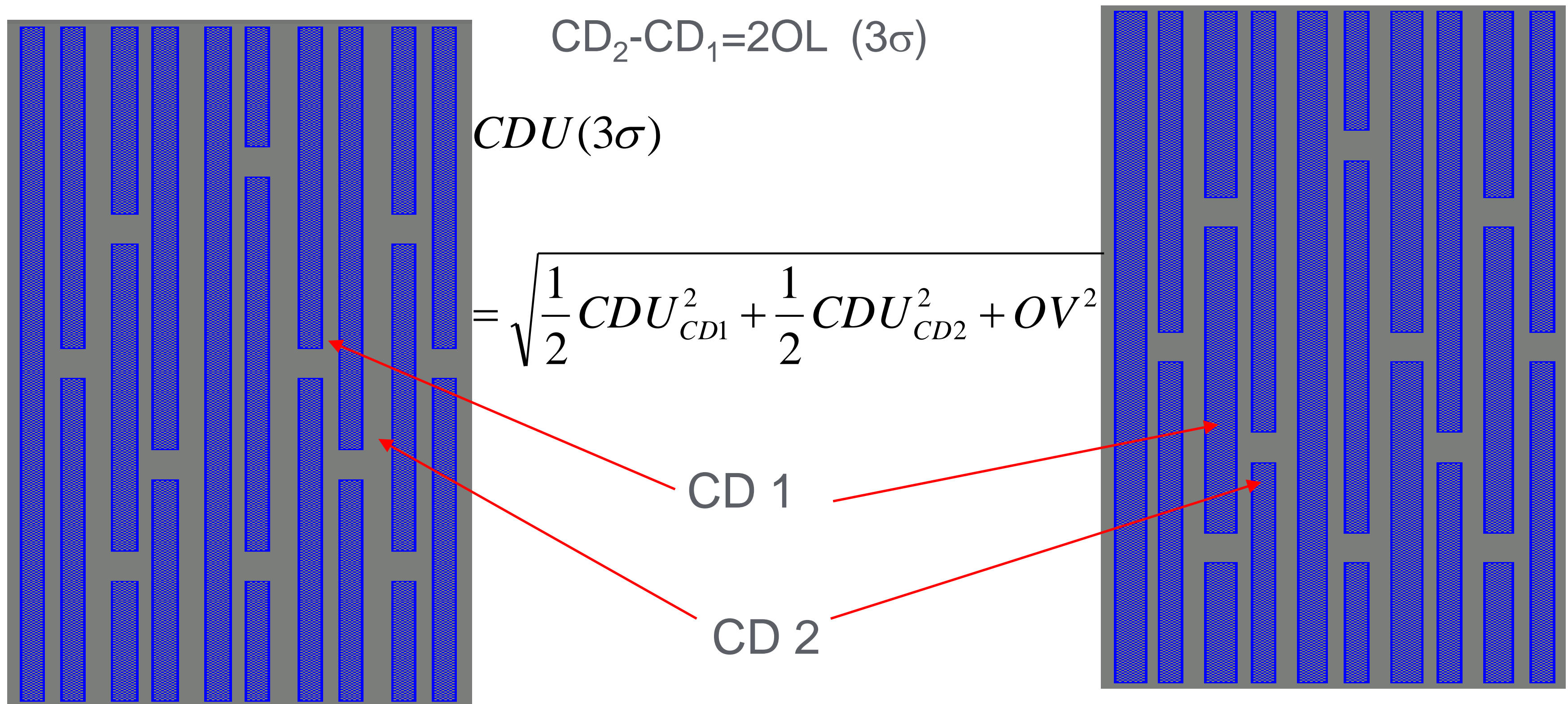


- Single direction gate restriction:
  - *Special constructs* (managed DRC violation) to maintain scale factor

Double patterning: Overlay Implications

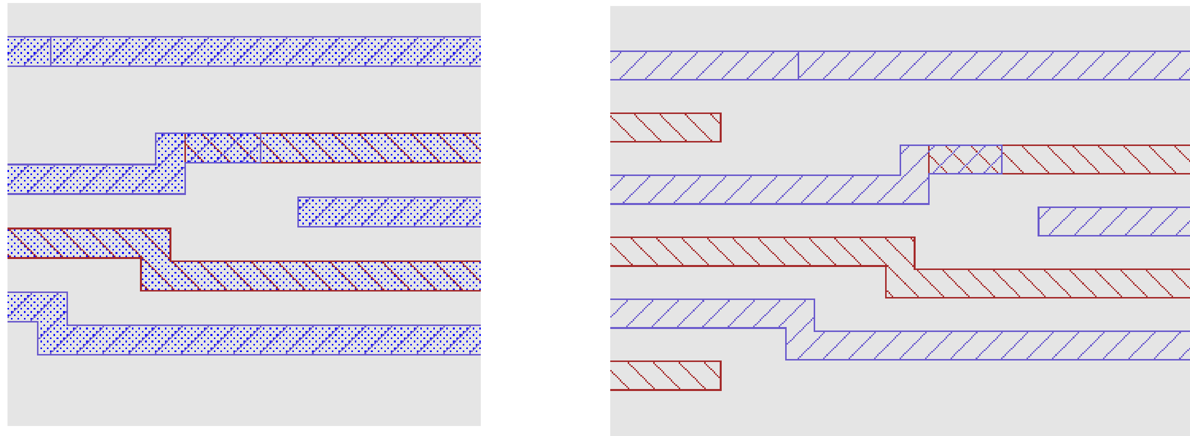
Overlay can cause local line width variations or local space CD variation depending on process scheme, which is translated into electrical performance degradation:

Gate with variation, gate length variation, resistance variation, capacitance variation



Double patterning: Stiching Implications

- Stitching denotes multiple colors on a single line
  - Allows for tighter designs and less coloration conflicts



- Stitching presents challenges for LVS/PEX
  - Fuzzy region where 2 neighboring lines could be like or different colors
  - Stitch is generated virtually
- Possible resistance issues due to stitch
  - At the point of merging between the 2 colors on the same line
  - Mis-alignment impact on resistance
- How to model for resistance?
  - PEX tool would need to know location of stitch

Retargeting (Physical Design)

- **Retargeting** denotes the operation of taking physical design shapes provided by the designer and turning them into “target shapes”.

- Motivation for retargeting functions in PEX
  - Decreased Complication For Designers
  - Improved Extraction run-time
  - Support of all input types, including GDS and LEF/DEF
  - Common PEX tech files for transistor and cell level extractions
  - Possible accuracy and simulation run-time improvements
- Motivation for retargeting functions in LVS
  - Remove need for separate module
  - Eliminate issues caused by integrating separate module with LVS
  - No special license requirements

Managed Variability through DFM

DFM brings manufacturing ***variability awareness*** into design through EDA tools enablement

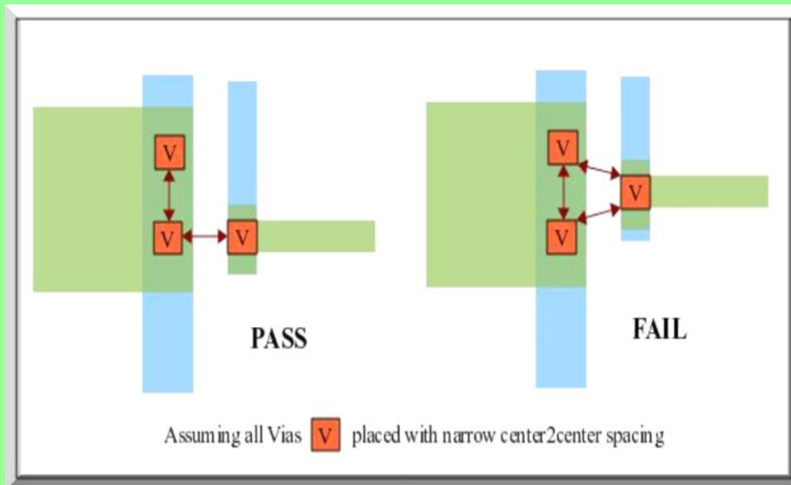
- Advanced Rule-Based Verification (Yield Analysis/Scoring and Automated Yield Enhancement)
- Novel Flow: DRC+
  - 2D Shapes Pattern-Matching Based Physical Design Verification
  - Model Accuracy and Full-Chip Performance
  - Seamless Integration in P&R Flow
- Si-Accurate Model-Based Printability Verification with Applications to *Special Constructs* (tech-cells)

Physical Verification: Beyond Design I

- Traditional Geometrical Design Rules

  Set of **geometrical constraints**, necessary to guarantee yield, defined over polygonal shapes and edges in the layout

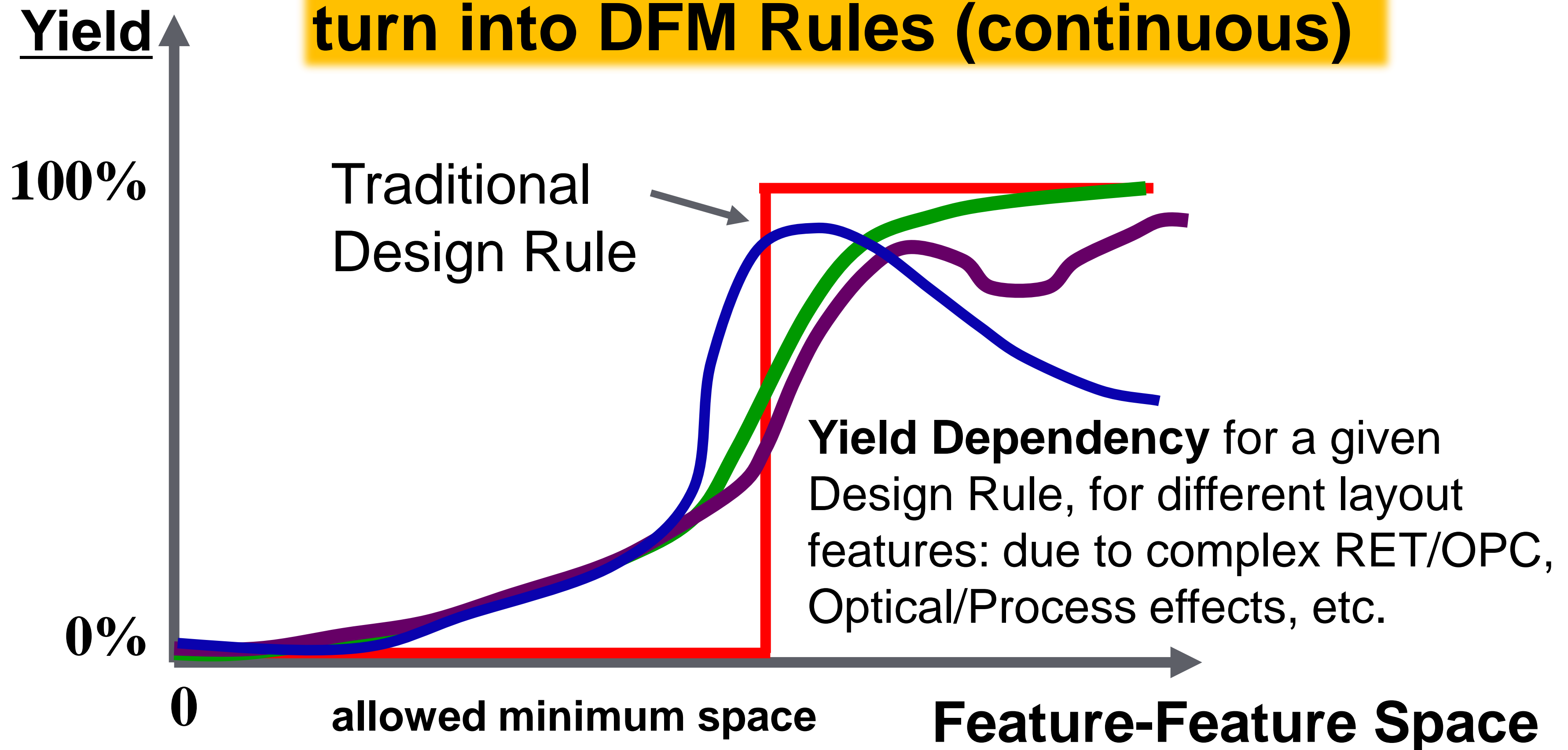
Complex Design Rules



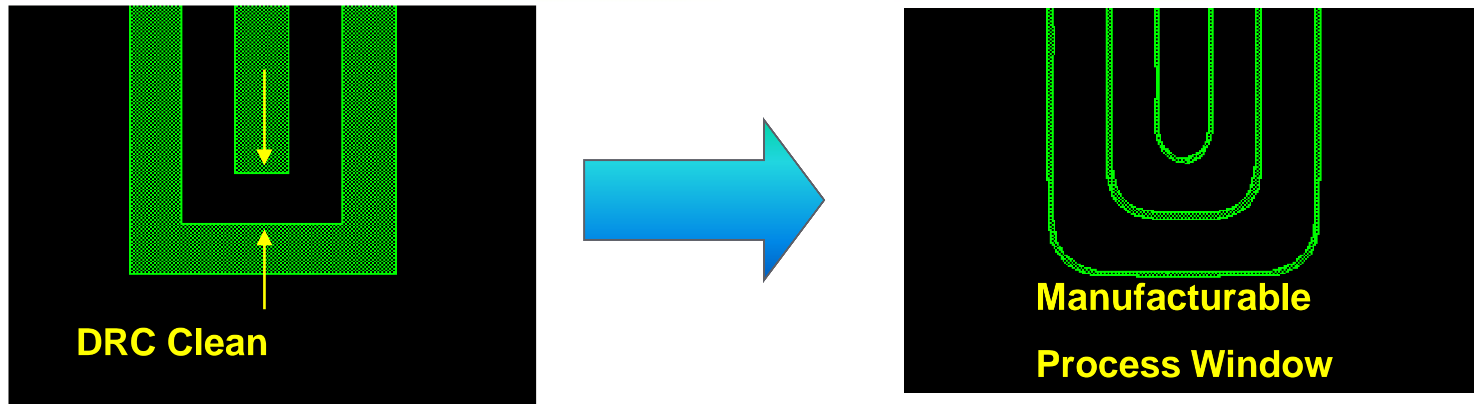
The Design Rule Manual mediates among:
•DESIGN
•TECHNOLOGY
•FAB

Two Types of DR:
1. Restrictive (95%)
2. Prescriptive (5%)

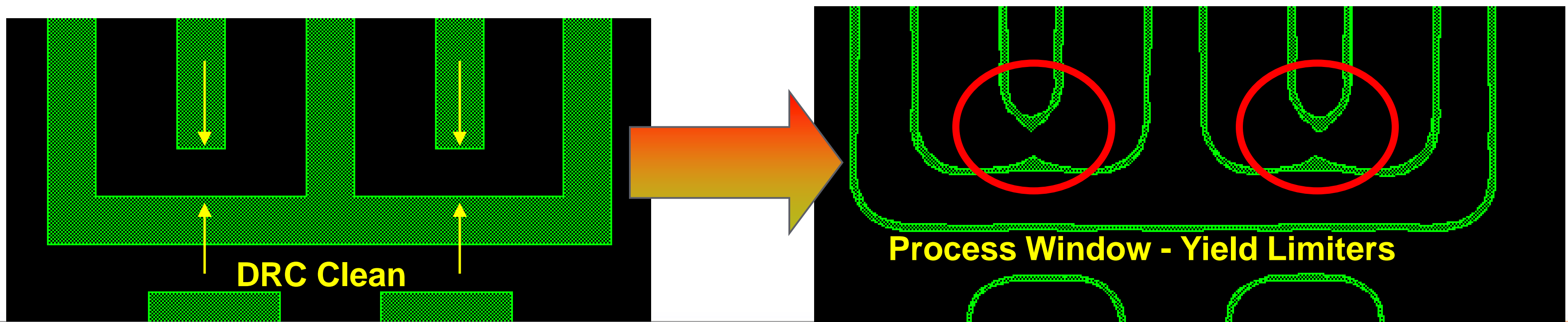
At 28nm and below: Physical Design dependent Yield



At 28nm, 20nm and below: Si-Accurate Model-Based Verification is needed



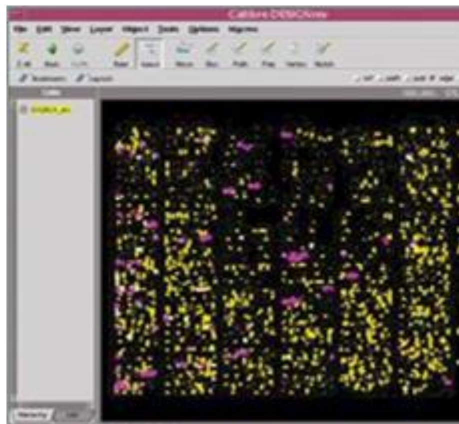
Model-Based Printability Verification for DRC clean physical design



Rule-Based DFM: Analysis/Scoring and Enhancement

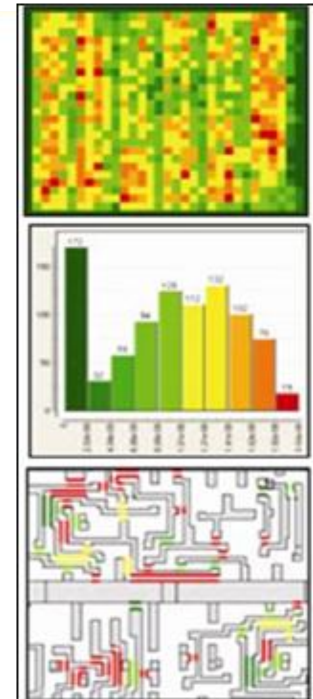
Typical Recommended Rule results in DRC difficult to analyze and fix

MAS/YES quickly identifies and fixes high impact DFM Rule violations



Type	Group	Rule Name	MAS_Total_Quality
mas28gf	Yield_Margin	611cR_V1	0.943832
mas28gf	Yield_CriticalArea	2x01aR_B1	0.942830
mas28gf	Yield_CriticalArea	52R	0.916912
mas28gf	Device_Variability	713R	0.847574
mas28gf	Yield_Redundancy	16X62R	0.804593
mas28gf	Yield_Redundancy	2x66R_W0	0.804593
mas28gf	Yield_Redundancy	8x60_YSaR	0.804593
mas28gf	Yield_Redundancy	8x60_ZVaR	0.804593
mas28gf	Yield_CriticalArea	601aR_M2	0.746212
mas28gf	Yield_CriticalArea	501aR	0.741389
mas28gf	Device_Variability	712R	0.648363

M(x+1) minimum overlap past Vx for two opposite sides >= 0.04um with the other two sides < 0.004 um, where x = 1-7.

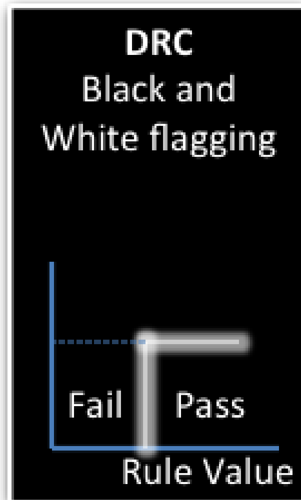


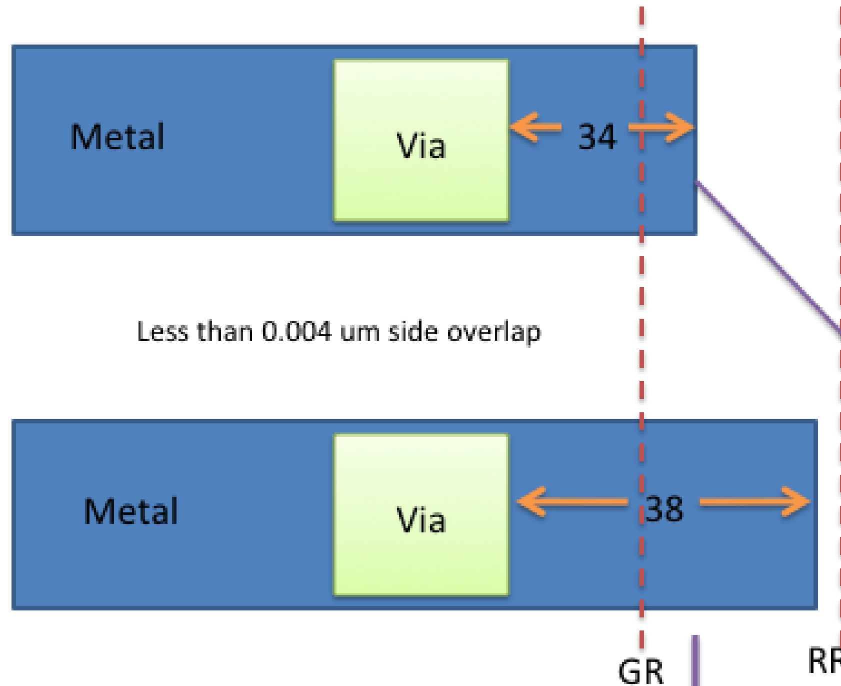
- MAS: An equation based tool to help designers to quickly **analyze** their design for usage of recommended rules, and prioritize fixes for the highest impact violations.
- YES : Seamless **auto-application** of recommendations without impacting current design within existing area

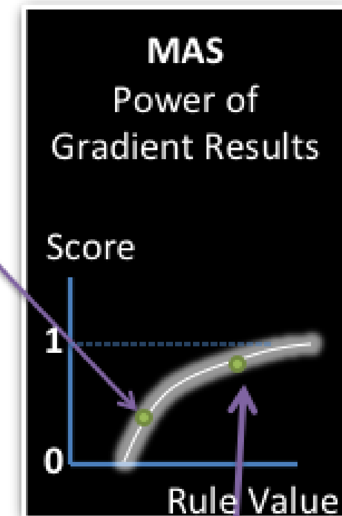
Equation-Based Scoring

EXAMPLE: Enclosure Rule

Enc.Rule.01	M(x+1) minimum overlap past Vx for two opposite sides with two other sides <0.004 um, where x=1-7	>=	0.04







Scoring Model for DFM Rules

Score

1.2
1
0.8
0.6
0.4
0.2
0

Low Priority rule

High Priority rule

Low
High
Density of Errors

Score correlation with Yield

100 %

Yield

Increasing MAS Score for DFM Rule i

MAS Score = 0.95

MAS Score = 0.9

MAS Score = 0.85

Increasing Process Maturity

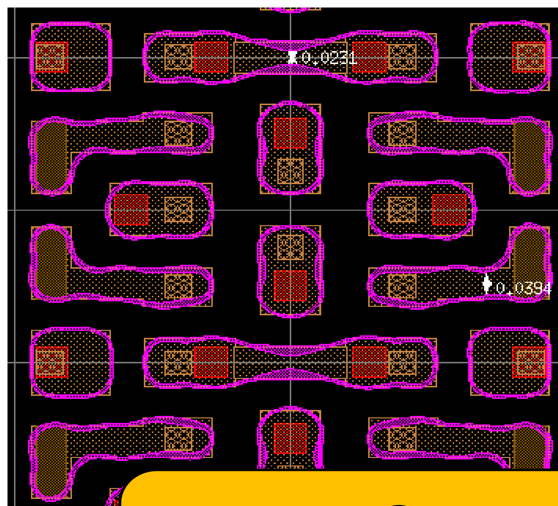
Failure Rate (for DFM Rule i)

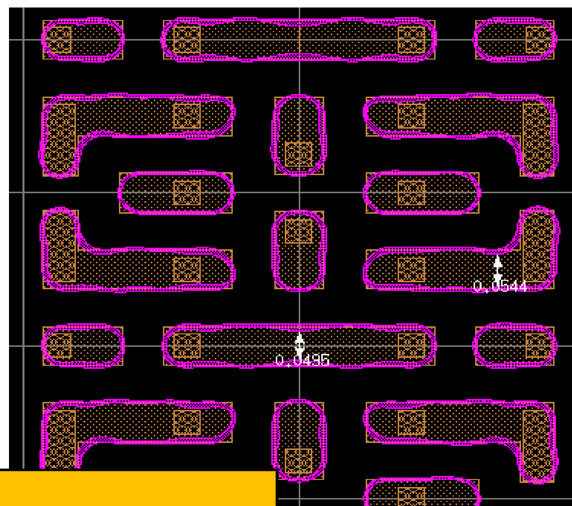
Full-Chip Solution: Automated Deployment of DFM Rules

After Improving Redundancy

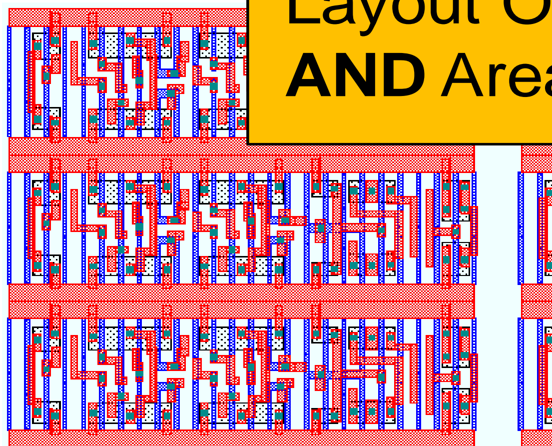
Before Improving Redundancy

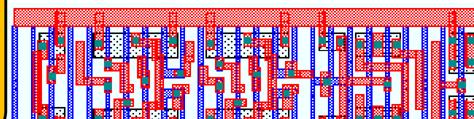
Model-Based DFM (Printability) drives Layout Optimization/Compaction

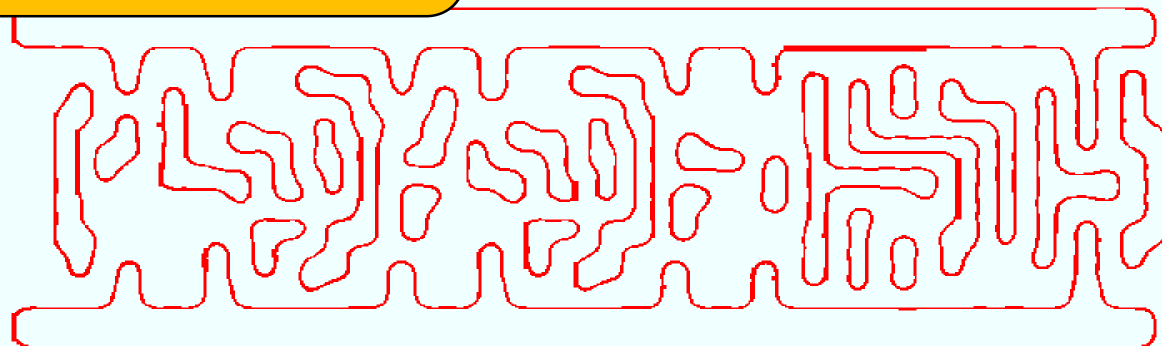




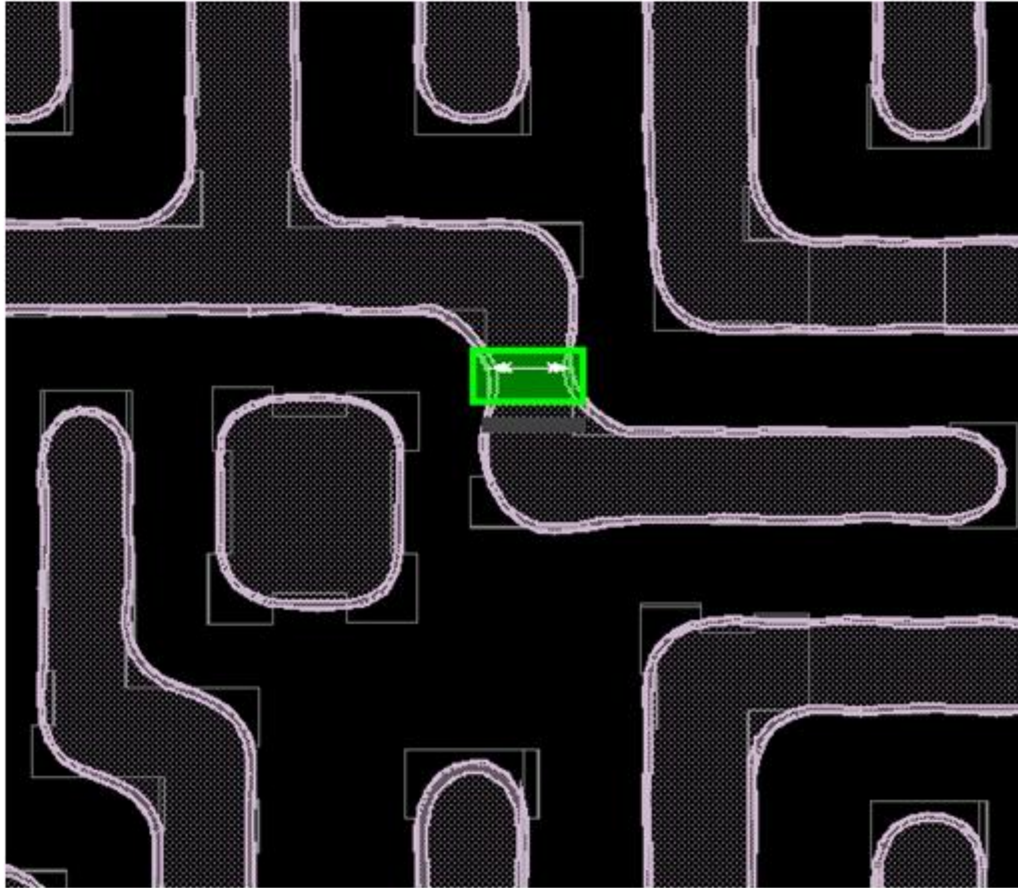
Layout Optimization
AND Area Compaction

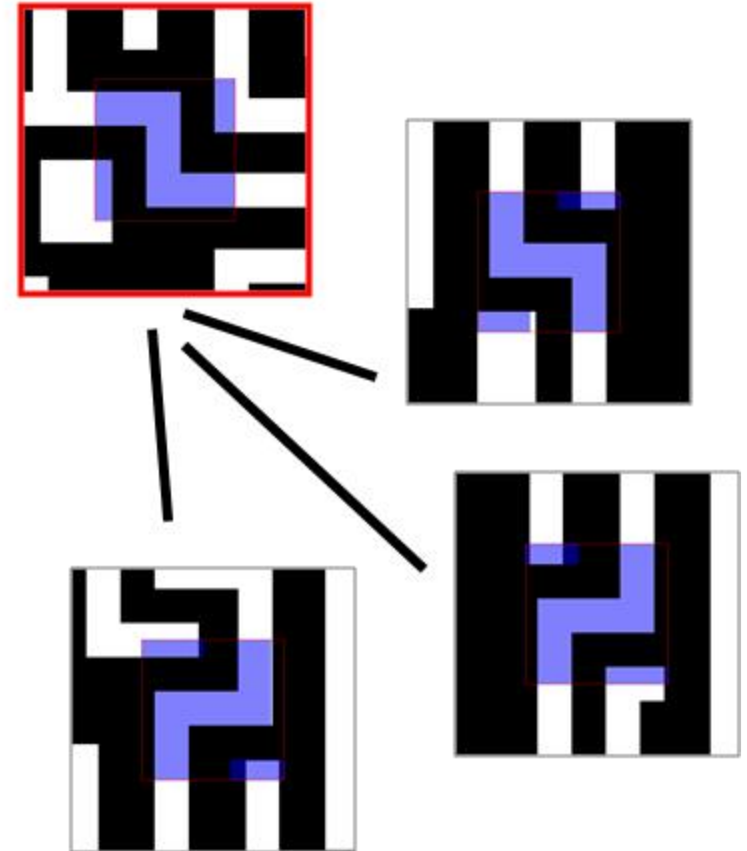






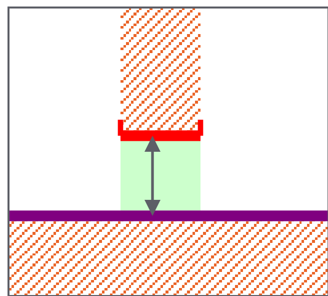
DRC+: Based on 2D Shapes Pattern-Matching: 10,000X Faster than Simulation

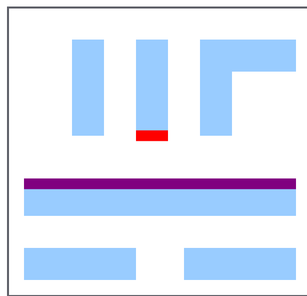
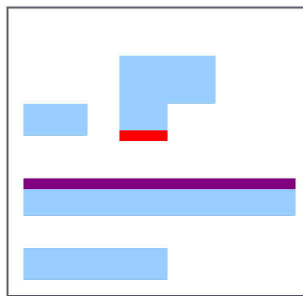
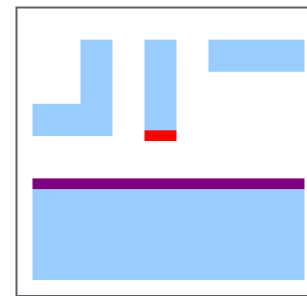
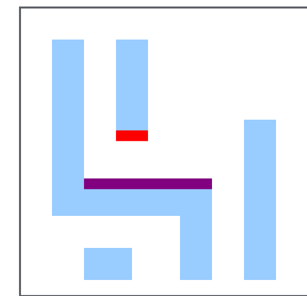




Configurations + Patterns = DRC+ Rules

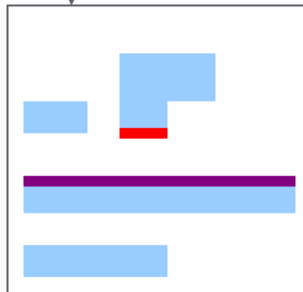
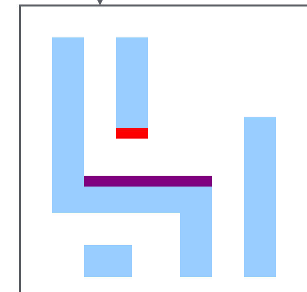
Configuration: tip-to-side



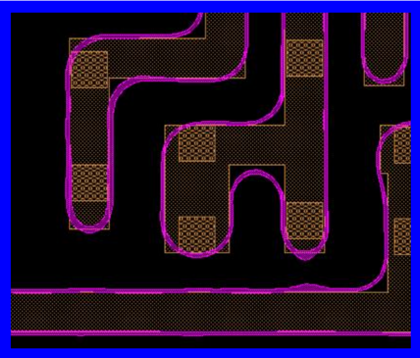
DRC constraint
≥ 60 nm

DRC+
DFM constraint
≥ 80 nm

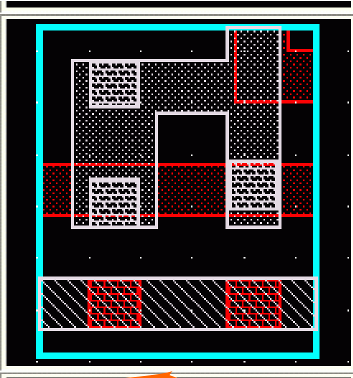



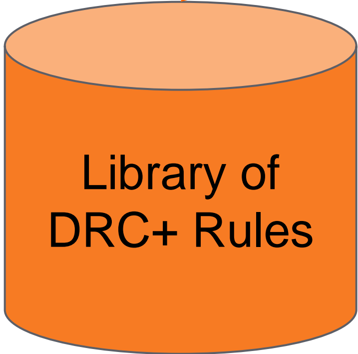
DRC Plus Rule Deck

Integration in P&R Implementation Flow

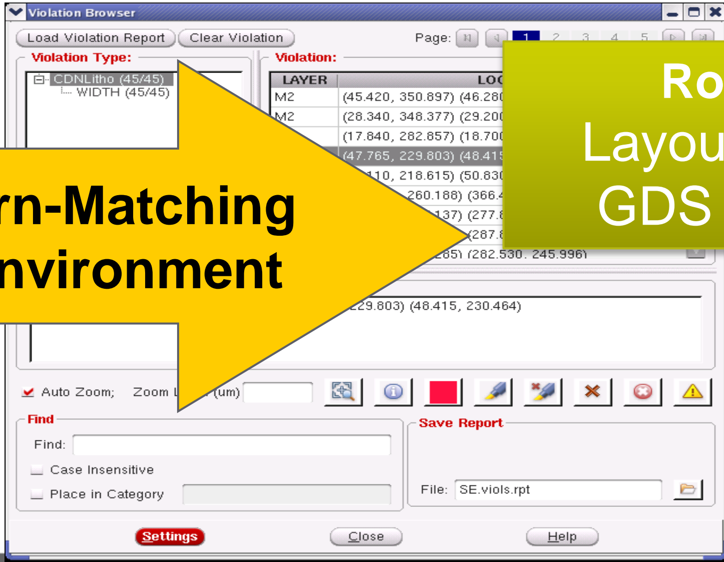


Automated Layout Analysis





Ultra-Fast Pattern-Matching in the Design Environment



Router, Layout Editor, GDS Signoff

Industry First from GLOBALFOUNDRIES

DFM Physical Verification in Timing Closure Loop

Traditional flow

Timing Closure

Placement

Routing ← ECO

STA

Physical Verification

DRC LVS ← ECO

Printability Simulation

Pattern Library

DRC+ enabled flow

Timing Closure

Placement

Routing ← ECO

DRC+

STA

Physical Verification

DRC LVS ← ECO

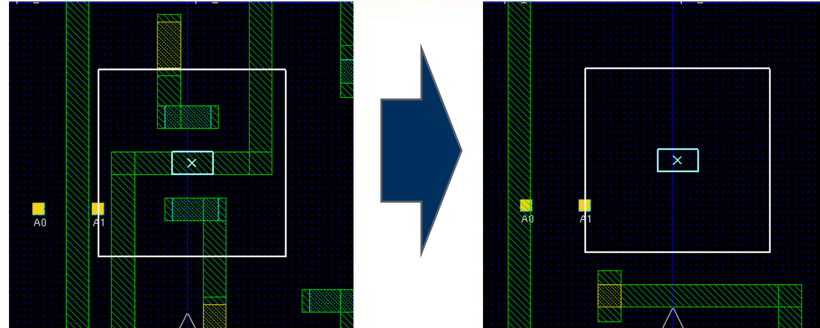
Printability Simulation (optional)

DRC+ Results on Sample Designs

Design	A	B	C	D	E	F	G	H
Chip Size (mm^2)	0.024	0.033	0.240	0.309	0.464	0.027	0.036	0.032
Core Size (mm^2)	0.023	0.031	0.115	0.294	0.440	0.026	0.035	0.030
Std Cell Density	85%	68%	56%	95%	64%	76%	60%	93%
Instance Count	17983	18581	83539	294572	303299	13577	14077	34234
Hotspots Detected	11	8	35	193	135	0	1	9
Hotspots Per mm^2 (Normalized)	475	259	306	658	307	0	29	297

- Consist of designs such as: CPU design and JPEG
- Different density, instance count and size
- Average of 291 hotspots per mm^2 detected

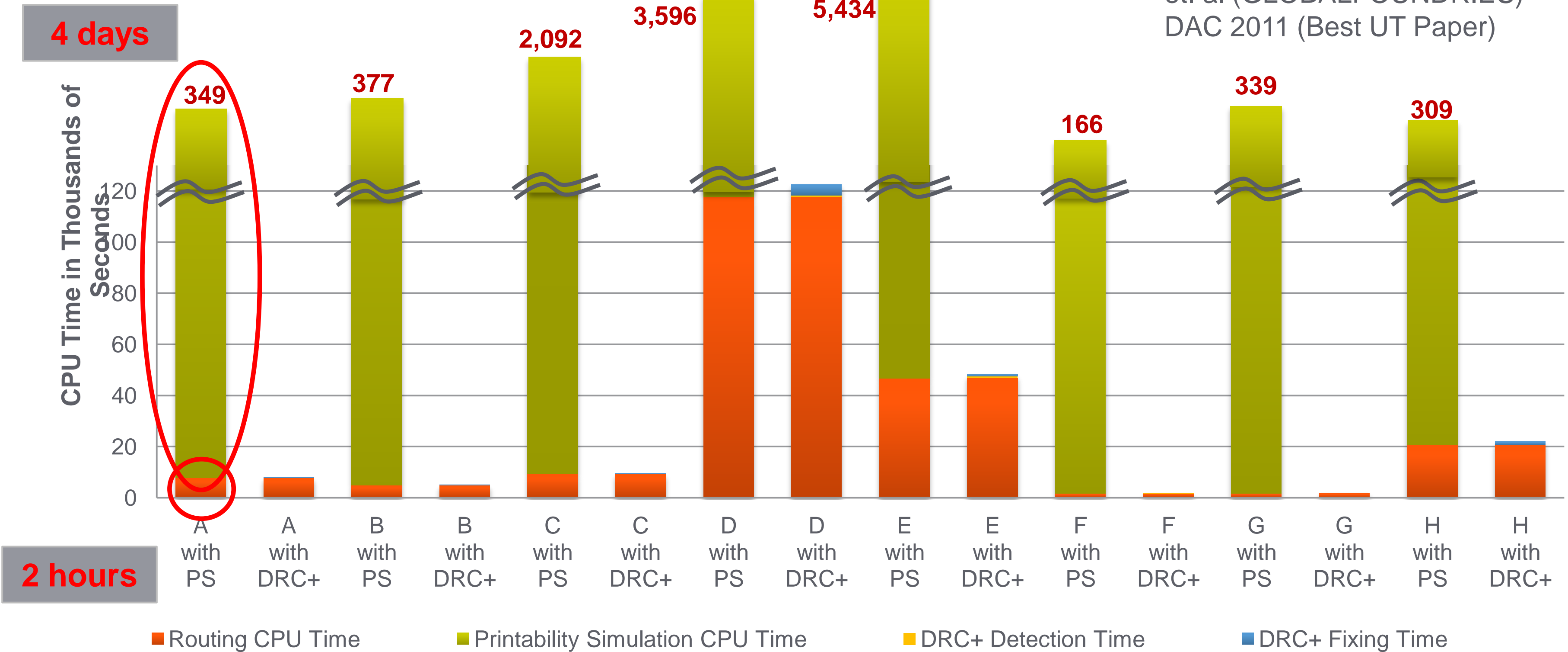
Automated Fixing and Timing Closure



		A	B	C	D	E	F	G	H
		Hotspots Found							
Auto-Fix Iterations	1	11	8	35	193	135	0	1	9
	2	0	0	0	1	0	-	0	0
	3	-	-	-	0	-	-	-	-
Max Timing Delta (ps)		43	19	5	**48**	23	N/A	3	45

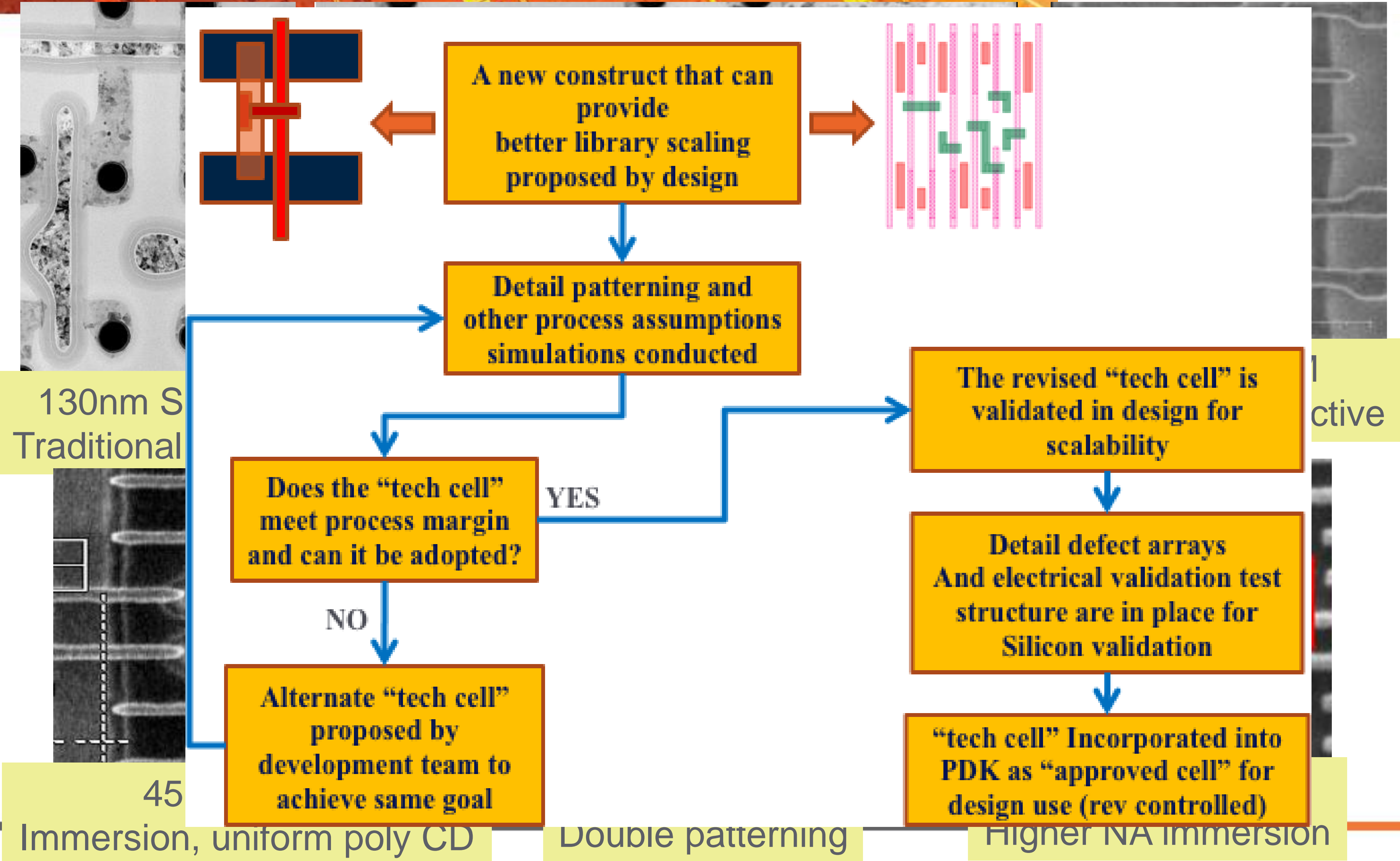
- 100% of DRC+ hotspots auto fixing with 2 iterations
- Timing delta after fix is significant enough to affect timing closure
- Essential to include DFM physical verification & fixing in timing closure

Variability Management Without Perfomance trade-offs



- DRC+ is over 10,000 times faster than printability simulation
- DRC+ detection and fixing adds very little to the overall routing runtime

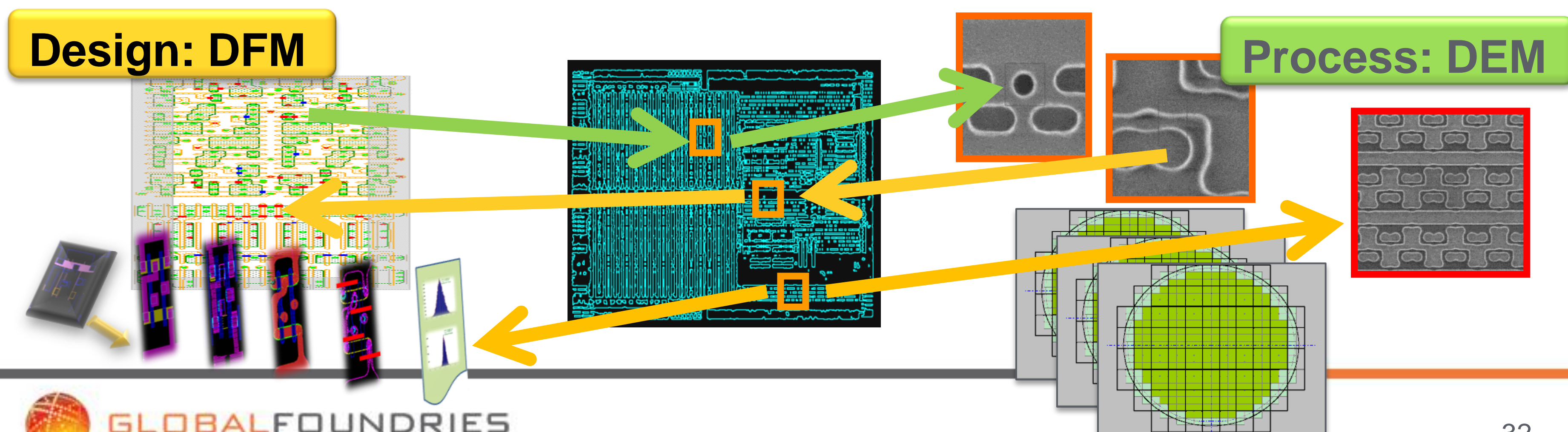
Fine-tuned Design-Technology Co-Optimization: Critical at 20nm!



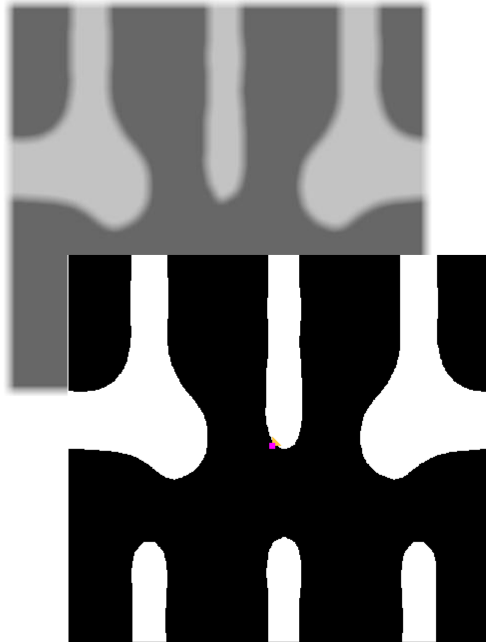
DFM: Design For Manufacturing
DEM: Design-Enabled Manufacturing

- DFM and DEM are 2 complementary set of methodologies, which mirror one another by tightly coupling flows in the design space with process metrology and yield data in the manufacturing space.

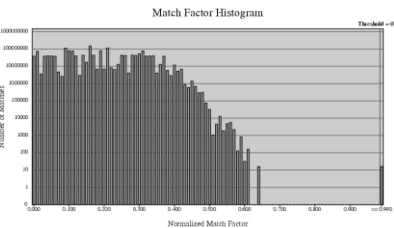
- **DFM** provides **process awareness into the design cycle** through accurately calibrated models and novel verification flows (DFM sign-off).
- **DEM** enables **manufacturing/design co-optimization**, using automated physical design analysis and characterization which in turn drive process optimization fine-tuned to specific customer product designs.



Pattern-Matching supports Design-Enabled-Manufacturing

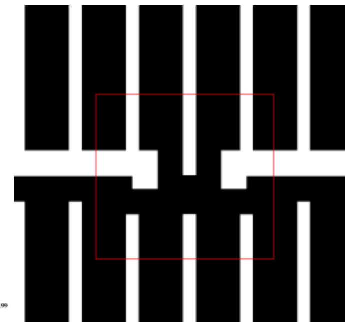


Binary Bitmap
from SEM Image

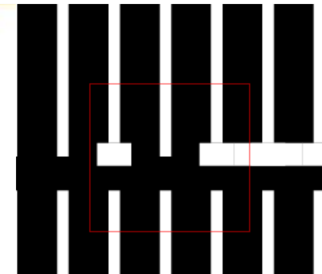


Full-Chip
Pattern-Match
(X,Y) Locations

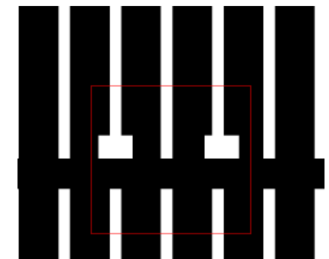
Match
Results:
Exact



I=84; M=94%

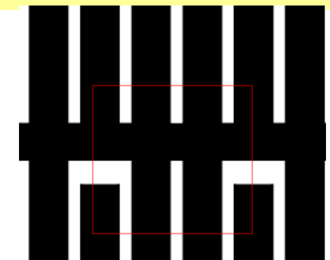


I=226; M=89%



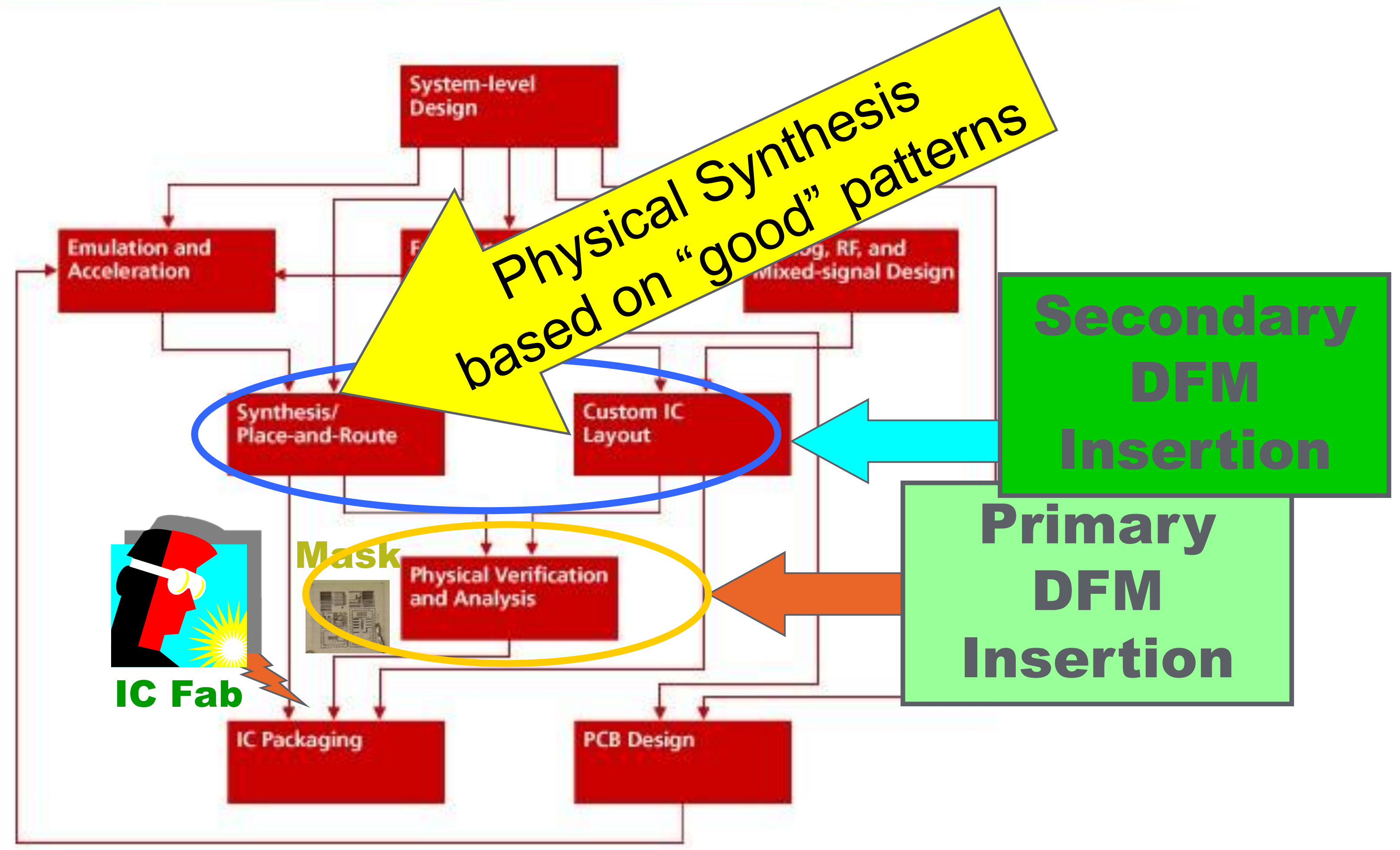
I=226; M=89%

and Fuzzy



I=52; M=83%

Evolution of DRC+ and Pattern Matching: Manufacturable-by-Construction Layouts



Patterns: from 20nm to 14nm

600
500
400
300
200
100
0

# of Patterns

-7 -6 -5 -4 -3 -2 -1 0

itivity to Manufacturing Process Variations (mean)

14nm

20nm
Critical for DPT

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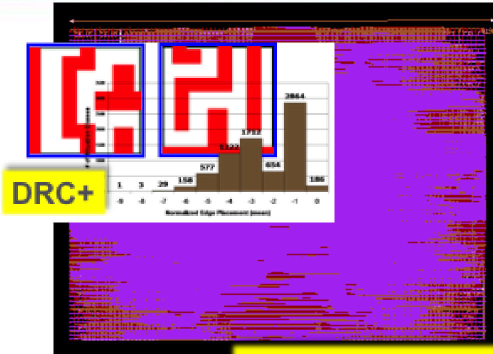
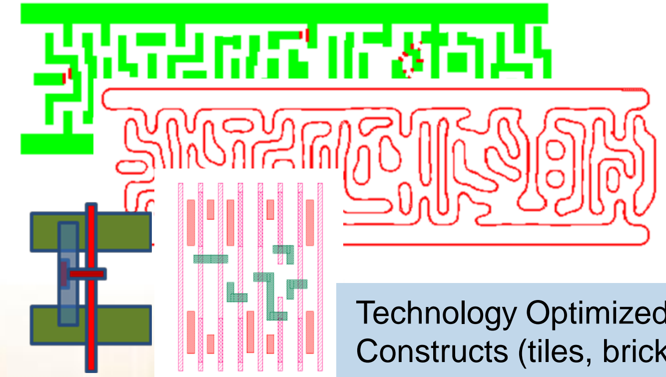
Conclusion: Variability Management fully deployed for 28 and 20nm design

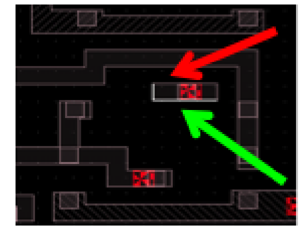


Process Aware Router Implementation

Design/Technology Co-Optimization

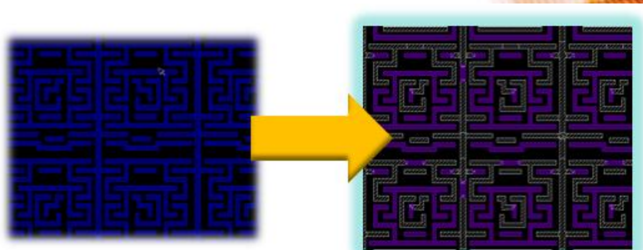


Technology Optimized Constructs (tiles, bricks)



MAS/YES Rule-Based DFM

Layout Decomposition Aware Physical Verification



Acknowledgments:

GLOBALFOUNDRIES Team (insert names)
Synopsys Team (insert names)