# Final Program

# ISQED

## 2018
## 19th International Symposium on

# QUALITY ELECTRONIC DESIGN

Security, IoT, Machine Learning/AI & Electronic Design

**March 13-14, 2018**
**Santa Clara Convention Center,**
**Santa Clara, CA USA**



IEEE | Electron Devices Society | CAS | Reliability Society | ISQED

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ISQED

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ISQED 2018 is produced and sponsored by the
**International Society for Quality Electronic Design**

# WELCOME TO ISQED 2018

On behalf of the ISQED 2018 conference and technical committees, we are pleased to welcome you to the 19th International Symposium on Quality Electronic Design.

ISQED 2018 is the premier interdisciplinary and multidisciplinary electronic design conference aimed at bridging the gap among electronic/semiconductor ecosystem members and providing electronic design tools, integrated circuit techniques, semiconductor manufacturing technologies, advanced packaging technologies, and assembly and test methodologies to achieve design quality.

ISQED is held with the technical sponsorship of the IEEE Electron Devices Society, the IEEE Circuits and Systems Society, and the IEEE Reliability Society. ISQED continues to provide and foster a unique opportunity to participants to interact and engage themselves in cutting edge tutorials, presentations, and panel and plenary sessions.

This conference is organized around the theme "Security, IoT, Machine Learning & Electronic Design". We have invited two distinguished keynote speakers who will focus on these topics. Additionally, four embedded tutorials by experts focus on this theme as well.

The two-day technical program with three parallel sessions packs nearly 80 papers highlighting the latest trends in electronic circuit and system design & automation, testing, verification, sensors, security, semiconductor technologies, cyber-physical systems, etc. ISQED 2018 also features a panel discussion, entitled "Deep Learning in System Design" on Tuesday, March 13th.

All of the technical presentations, plenary sessions, panel discussions, tutorials and related events will take place on March 13-14 at the Santa Clara Convention Center in Santa Clara, CA USA. Please refer to the conference booklet and/or ISQED website for program details.

We would like to thank the ISQED 2018 corporate sponsors: Synopsys, Innovotek, and the Silicon Valley Polytechnic Institute for their valuable support of this conference. Welcome to another exciting year of ISQED! It couldn't have happened without your support and participation.

***Steve Heinrich-Barna***
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Panel Co-Chair

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General Chair

***José Pineda de Gyvez***
Tutorial Co-Chair

***Paul Wesling***
Publication Chair

# ISQED 2018 Best Paper Candidates

**1B.1**

**Hybrid-Comp: A Criticality-Aware Compressed Last-Level Cache**

*Amin Jadidi[1], Mohammad Arjomand[2], Mahmut T. Kandemir[1], Chita R. Das[1]*

**[1]School of Electrical Engineering and Computer Science, Pennsylvania State University, USA**

**[2]School of Computer and Electrical Engineering, Georgia Institute of Technology, USA**

**1C.2**

**LUPIS : Latch-Up Based Ultra Efficient Processing-in-Memory System**

*Joonseop Sim[1], Mohsen Imani[1], Woojin Choi[1], Yeseong Kim[2], Tajana Rosing[1]*

**[1]UCSD, [2]University of California San Diego**

**1C.3**

**Energy efficient neuromorphic processing using spintronic memristive device with dedicated synaptic and neuron terminology**

*Zoha Pajouhi*

**Intel Corporation**

**2A.1**

**Recognition of Regular Layout Structures**

*Yu-Cheng Chiang, Shr-Cheng Tsai and Rung-Bin Lin*

**Yuan Ze University, Taoyuan, Taiwan**

**2A.2**

**A Simplified Methodology for Complex Analog Module Layout Generation**

*Pradeep Kumar Chawda*

**Texas Instruments Inc.**

**4A.2.1**

**A Deep Learning Based Approach for Analog Hardware Implementation of Delayed Feedback Reservoir Computing System**

*Jialing Li, Kangjun Bai, Lingjia Liu, Yang Yi*

**Bradley Department of Electrical and Computing Engineering, Virginia Tech, Blacksburg, Virginia**

**4A.2.2**

**An Area and Energy Ecient Design of Domain-Wall Memory-Based Deep Convolutional Neural Networks using Stochastic Computing**

*Xiaolong Ma[1], Yipeng Zhang1, Geng Yuan[1], Ao Ren1, Zhe Li[1], Jie Han[2], Jingtong Hu[3], Yanzhi Wang[1]*

**[1]Syracuse University, [2]university of alberta, [3]University of Pittsburgh**

**4B.2**

**Parallel implementation of finite state machines for reducing the latency of stochastic computing**

*Cong Ma and David J. Lilja*

**Department of Electrical and Computer Engineering, University of Minnesota, Twin Cities**

**5B.1**

**Securing FPGA-Based Obsolete Component Replacement for Legacy Systems**

*Zhiming Zhang[1], Laurent Njilla[2], Charles Kamhoua[3], Kevin Kwiat[2], and Qiaoyan Yu[1]*

**[1]University of New Hampshire, [2]Cyber Assurance Branch, Air Force Research Laboratory, [3]Army Research Laboratory**

# ISQED 2018 Best Papers

**4A.2.1**

**A Deep Learning Based Approach for Analog Hardware Implementation of Delayed Feedback Reservoir Computing System**

*Jialing Li, Kangjun Bai, Lingjia Liu, Yang Yi*

**Bradley Department of Electrical and Computing Engineering,**
**Virginia Tech, Blacksburg, Virginia**

**4B.2**

**Parallel implementation of finite state machines for reducing the latency of stochastic computing**

*Cong Ma and David J. Lilja*

**Department of Electrical and Computer Engineering, University of Minnesota, Twin Cities**

* Authors of best papers are honored during the Synopsys sponsored luncheon on Tuesday March 13

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**Arnaud Virazel - LIRMM**
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**Min Zhao - oracle**

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## Emerging Process&Device Tech. &Design Issues (EDT)

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**Rouwaida Kanj - American University of Beirut**
**Jin-Fu Li - National Central University**
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**Riaz Naseer - Rockwell Automation**
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## System-level Design and Methodologies (SDM)

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**Gabriela Nicolescu - Ecole Polytechnique de Montréal**
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## 3 Dimensional Integration &Adv. Packaging (TDIP)

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# GENERAL INFORMATION

## ISQED 2018
## GENERAL INFORMATION

*March 13-14, 2018*
*Santa Clara Convention Center*
*5001 Great America Pkwy, Santa Clara, CA 95054*

## KEYNOTE SPEECHES

*Tuesday, March 13, 9:00 AM - 10:45 AM*
**Meeting Rooms 209/210**

### Murphy Was an Optimist: Embracing Asymmetry in Electronics

**Kerry Bernstein**
Microsystems Technology Office
**Defense Advanced Research Projects Agency (DARPA)**

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*Tuesday, March 13, 11:50 AM - 12:25 PM*
**Meeting Rooms 209/210**

### AI Creating New Opportunities for Chip Designers

**Dr. Yankin Tanurhan**
Vice President of Engineering
**Synopsys**

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*Wednesday, March 14, 9:00 AM - 9:45 AM*
**Meeting Rooms 209/210**

### Innovation in an Exponential World

**Dr. Nate Brese**
Marketing Fellow, Electronics & Imaging
**DowDuPont**

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## Embedded Tutorials

*Chair:*
**Shiyan Hu** - *Michigan Technological University*

*Co-Chair:*
**José Pineda de Gyvez** - *Eindhoven University of Technology*

**Meeting Rooms 209/210**

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*Tuesday, March 13, 1:35 PM - 2:35 PM*

### Power-Aware Testing in the Era of IoT

**Dr. Patrick Girard**
*LIRMM / CNRS - University of Montpellier / France*

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*Tuesday, March 13, 2:35 PM - 3:35 PM*

### Ambient Energy Harvesting Sensor Platform for Internet of Things: From Circuit to System

**Prof. Yongpan Liu**
*Tsinghua University, P.R. China*

**Prof. Jingtong Hu**
*University of Pittsburgh*

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*Wednesday, March 14, 1:30 PM - 2:30 PM*

### Ultra-Low-Power Digital Architectures for the Internet of Things

**Prof. Davide Rossi**
*DEI, University of Bologna*

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*Wednesday, March 14, 2:30 PM - 3:30 PM*

### Managing the ever increasing complexity of Cyber-Physical Systems in High-Tech Industry

**Dr. Wouter Leibbrandt**
*Embedded Systems Innovation, TNO, The Netherlands*

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# GENERAL INFORMATION

## ISQED LUNCH & AWARDS CEREMONY

*Tuesday, March 13, 11:20 AM - 11:50 AM*
**Meeting Rooms 209/210**

### ISQED Best Paper Awards

Recipients of the ISQED 2018 Best Paper Award will be recognized during the ISQED luncheon on Tuesday. List of best papers is shown in Page 3 of this document.

## Luncheon Panel Discussion

*Tuesday, March 13, 12:25 PM - 1:25 PM*
**Meeting Rooms 209/210**

### Role of Machine Learning/AI in Quality Electronic Design

Machine learning is beginning to have an impact on system design and verification business, cutting the cost of designs by allowing tools to suggest solutions to common problems that would take design teams weeks or even months to work through. This reduces cost of designs, and potentially expands the market for such tools, opening the door to new designs and faster turnarounds. In this panel, we will have experts from industry and academia discussing the role of machine learning in designs of today and of a foreseeable future.

## TECHNICAL SESSIONS

There are a total of 15 paper sessions held on Tuesday and Wednesday. Technical sessions are held in the format of three parallel tracks in **Meeting Rooms 201, 206 & 207**.

## Poster Papers & Mixer

Poster display will take place on Tuesday afternoon 5:15 PM-6:45 PM in the Atrium area outside of the **Meeting Rooms.** Authors will be available to discuss their works and to answer questions. Refreshments will be served.

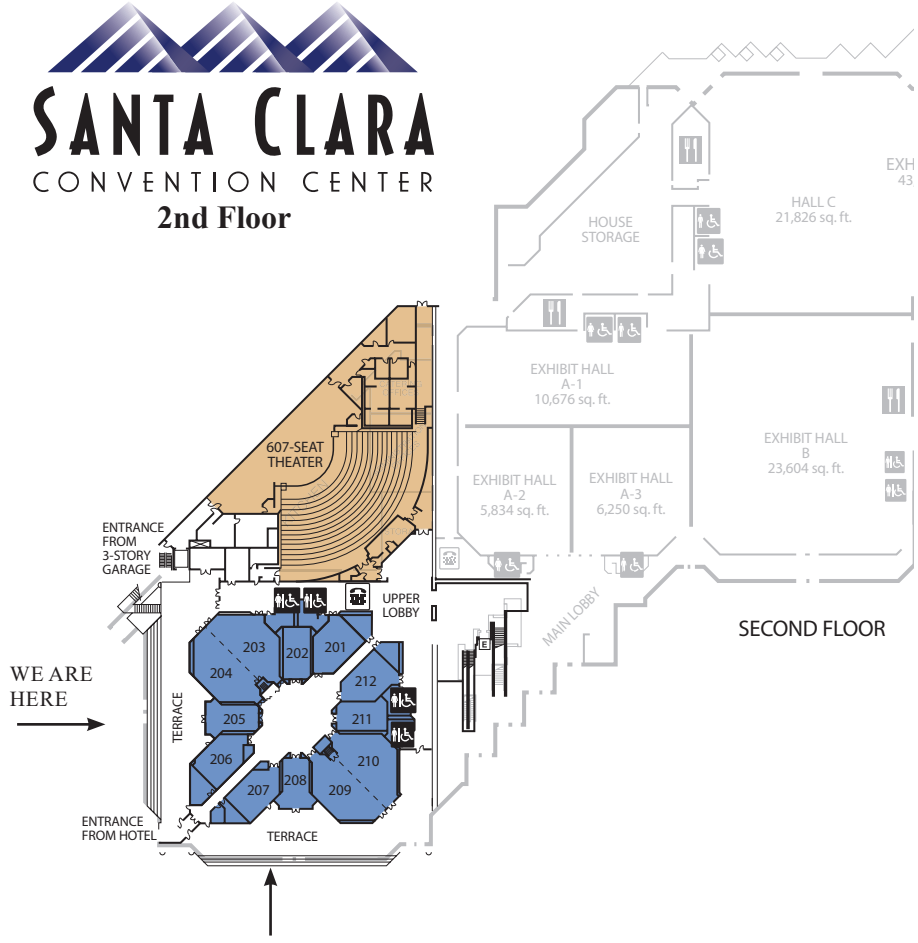
## ON-SITE REGISTRATION

Tentative time schedule of on-site registration is as follows:

| | |
|---|---|
| *Tuesday, March 13* | *8:00 AM - 3:00 PM* |
| *Wednesday, March 14* | *8:00 AM -1:00 PM* |

Registration desk location will be beside the Meeting rooms 209/210.

# FLOOR PLAN




**Santa Clara Convention Center**
***2nd Floor***
General Sessions & Tutorials:
Meeting Rooms 209/210

Breakout Rooms:
Meeting Rooms, 201, 206 and 207

# PROGRAM AT A GLANCE

ISQED 2018 PROGRAM AT A GLANCE

| DATE | TIME | | | |
|---|---|---|---|---|
| **TUESDAY 3/13/2018** | 9:00 AM -9:45AM | **KEYNOTE SPEECH**<br>(MEETING ROOMS 209/210)<br><br>**MURPHY WAS AN OPTIMIST: EMBRACING ASYMMETRY IN ELECTRONICS**<br>*KERRY BERNSTEIN - DEFENSE ADVANCED RESEARCH PROJECTS AGENCY (DARPA)* | | |
| | 9:45 AM - 10:00 AM | **MORNING BREAK** | | |
| | 10:00 AM -11:20 AM | **SESSION 1A**<br>DESIGN VERIFICATION AND TEST<br><br>MEETING ROOM 201 | **SESSION 1B**<br>SYSTEM-LEVEL DESIGN AND METHODOLOGIES (SDM)<br><br>MEETING ROOM 206 | **SESSION 1C**<br>EMERGING LOGIC AND MEMORY TECHNOLOGIES IN IOT AND NEUROMORPHIC ARCHITECTURES<br><br>MEETING ROOM 207 |
| | | | | |
| | 11:20 AM -11:50 AM | **ISQED LUNCHEON, KEYNOTE & PANEL**<br>MEETING ROOMS 209/210<br>BEST PAPER AWARDS , COMMITTEE RECOGNITION | | |
| | 11:50 AM -12:25 PM | **LUNCH KEYNOTE**<br><br>**AI CREATING NEW OPPORTUNITIES FOR CHIP DESIGNERS**<br>*DR. YANKIN TANURHAN - VICE PRESIDENT ENGINEERING, DESIGNWARE PROCESSOR CORES, IP SUBSYSTEMS, NON-VOLATILE MEMORY, SYNOPSYS*<br><br>SYNOPSYS® Silicon to Software | | |
| | 12:25 PM -1:25 PM | **PANEL DISCUSSION**<br><br>**DEEP LEARNING IN SYSTEM DESIGN** | | |
| | 1:25 PM -1:35 PM | **BREAK** | | |
| | 1:35 PM -2:35 PM | **EMBEDDED TUTORIAL 1**<br><br>**POWER-AWARE TESTING IN THE ERA OF IOT**<br><br>MEETING ROOMS 209/210 | | |
| | 2:35 PM -3:35 PM | **EMBEDDED TUTORIAL 2**<br><br>**AMBIENT ENERGY HARVESTING SENSOR PLATFORM FOR INTERNET OF THINGS: FROM CIRCUIT TO SYSTEM**<br><br>MEETING ROOMS 209/210 | | |
| | 3:35 PM -3:45 PM | **AFTERNOON BREAK** | | |
| | 3:45 PM -5:25 PM | **SESSION 2A**<br>AUTOMATED ANALOG AND DIGITAL CIRCUIT OPTIMIZATION<br><br>MEETING ROOM 201 | **SESSION 2B**<br>SYSTEM-LEVEL DESIGN AND METHODOLOGIES (SDM)<br><br>MEETING ROOM 206 | **SESSION 2C**<br>POSTER BRIEFS<br><br>MEETING ROOM 207 |
| | 5:25 PM -6:45 PM | **POSTER PAPERS & MIXER**<br>HALLWAY OUTSIDE MEETINGS ROOMS | | |
| | | | | |
| **WEDNESDAY 3/14/2018** | | | | |
| | 9:00 AM -9:45 AM | **KEYNOTE SPEECH**<br>(MEETING ROOMS 209/210)<br><br>**INNOVATION IN AN EXPONENTIAL WORLD**<br>*NATE BRESE - ELECTRONICS & IMAGING - DOWDUPONT* | | |
| | 9:45 AM -10:00 AM | **MORNING BREAK** | | |
| | 10:00 AM -11:20 AM | **SESSION 3A**<br>DESIGN VERIFICATION AND TEST<br><br>MEETING ROOM 201 | **SESSION 3B**<br>HIGH PERFORMANCE / LOW POWER LOGIC DESIGN<br><br>MEETING ROOM 206 | **SESSION 3C**<br>IOT & SMART SENSORS<br><br>MEETING ROOM 207 |
| | 11:20 AM -11:40 AM | **MORNING BREAK** | | |
| | 11:40 AM -1:00 PM | **SESSION 4A (4A.1 & 4A.2**<br>DESIGN TECHNOLOGY CO-OPTIMIZATION (DTCO)<br>MACHINE LEARNING ON CONVENTIONAL AND EMERGING PLATFORMS<br>MEETING ROOM 201 | **SESSION 4B**<br>HIGH PERFORMANCE / LOW POWER LOGIC DESIGN<br><br>MEETING ROOM 206 | **SESSION 4C**<br>IOT & SMART SENSORS<br><br>MEETING ROOM 207 |
| | 1:00 PM -1:30 PM | **LUNCH BREAK** | | |
| | 1:30 PM -2:30 PM | **EMBEDDED TUTORIAL 3**<br>**ULTRA-LOW-POWER DIGITAL ARCHITECTURES FOR THE INTERNET OF THINGS**<br>MEETING ROOMS 209/210 | | |
| | 2:30 PM -3:30 PM | **EMBEDDED TUTORIAL 4**<br>**MANAGING THE EVER INCREASING COMPLEXITY OF CYBER-PHYSICAL SYSTEMS IN HIGH-TECH INDUSTRY**<br>MEETING ROOMS 209/210 | | |
| | 3:30 PM -3:40 PM | **AFTERNOON BREAK** | | |
| | 3:40 PM -5:00 PM | **SESSION 5A**<br>ENERGY EFFICIENT LOGIC DESIGN USING SCALED TECHNOLOGIES<br><br>MEETING ROOM 201 | **SESSION 5B**<br>HARDWARE SECURITY: PUF, OBFUSCATION, AND TROJAN DETECTION<br><br>MEETING ROOM 206 | **SESSION 5C**<br>DEMYSTIFYING SELF-DRIVING CARS<br><br>MEETING ROOM 207 |

# ISQED Keynote 1P.1

Tuesday March 13

*9:00 AM - 9:45 AM*
Meeting Rooms 209/210

## Murphy Was an Optimist: Embracing Asymmetry in Electronics

**Kerry Bernstein**
***Defense Advanced Research Projects Agency (DARPA)***

The high performance digital microelectronic component is designed to do one thing – that is to faithfully execute its instruction set architecture. The resulting hardware embodiment, however, forces structure into materials that resist order. These structures immediately begin reverting to their lowest energy state and highest disorder. Semiconductor wear-out and aging are evidence of this entropy. Countering these effects is expensive, and contributes nothing to transaction throughput or energy efficiency. Against this backdrop, selected emerging concepts in device physics, process, design, architecture, reliability and hardware security may collectively embrace entropy, and use asymmetry in our favor. This talk will provide an overview of concepts that connect low level device physics to high level architecture in a way that leverages asymmetry in our favor. Given that current devices are confronting not just atomistic but now quantum-mechanical limitations to scaling, the need is greater than ever.

### About Kerry Bernstein

Kerry Bernstein is a program manager in the Microsystems Technology Office at the Defense Advanced Research Projects Agency (DARPA). His interests are in the area of hardware security and emerging high performance post-CMOS device technologies. Mr. Bernstein formerly spent 33 years at the IBM T.J. Watson Research Center and IBM Microelectronics, working in the areas of leading edge, high performance/low-power computing devices and circuits, and 3D Integration. He attributes any successes realized to be due in large part to being surrounded by wonderful people throughout his entire career. Mr. Bernstein received his B.S. (1978) in Electrical Engineering from Washington University in St. Louis, Missouri, and continued graduate work at the University of Vermont. He has co-authored four (4) textbooks, holds 155 patents, and is a Fellow of the Institute of Electrical and Electronics Engineers (IEEE).

## Luncheon Keynote

Tuesday March 13

*11:50 AM - 12:25 PM*
Meeting Rooms 209/210

# AI Creating New Opportunities for Chip Designers

**Dr. Yankin Tanurhan**
***Synopsys***

Rapid advances in artificial intelligence (AI) and machine learning are creating the next wave of opportunities for SoC designers. From facial recognition to surveillance monitoring to autonomous driving, AI is becoming must-have technology for an expanding number of tech applications. Neural networks, modeled after the human brain, have significantly improved developers' ability to implement machine learning hardware and software in edge devices, particularly for object detection and embedded vision applications. This keynote presentation provides an industry perspective on AI trends and emerging uses.

**About Yankin Tanurhan**

Dr. Yankin Tanurhan is Vice President Engineering, DesignWare Processor Cores, IP Subsystems, Non-Volatile Memory at Synopsys leading low power and high-performance ARC and EV Embedded Processor developments targeted from Mobile, IoT, Embedded Vision, AI/ML, Digital Home, Automotive/Industrial, Security to Storage markets. His portfolio additionally includes ASIP tool development with products like ASIP Designer and Programmer, IP Subsystems products like Sensor Fusion, Audio, Vision and Security Subsystems and CMOS based Non-Volatile Memory IP development. Dr. Tanurhan has authored 100+ papers in refereed publications. He holds a B.S. and M.S. in Electrical and Computer Engineering from Rheinisch Westfaellische Technische Hochschule (RWTH) in Aachen, Germany and a Dr. Ing. degree summa cum laude in Electrical Engineering from the University of Karlsruhe (TH) in Karlsruhe, Germany.

## Panel Discussion

Tuesday March 13

*12:25 PM –1:25 PM*
Meeting Rooms 209/210

# Role of Machine Learning/AI in Quality Electronic Design

**Summary**: Machine learning is beginning to have an impact on system design and verification business, cutting the cost of designs by allowing tools to suggest solutions to common problems that would take design teams weeks or even months to work through. This reduces cost of designs, and potentially expands the market for such tools, opening the door to new designs and faster turnarounds. In this panel, we will have experts from industry and academia discussing the role of machine learning in designs of today and of a foreseeable future.

**Moderator:**
**Vinod Viswanath** - Director of Research and Development, Real Intent

**Panelists:**
**Dr. Chris Rowen** - CEO, Cognite Ventures
**Dr. Drew Wingard** - CEO, Sonics Inc.
**Prof. Paul Franzon** - Cirrus Logic Distinguished Professor of ECE, NCSU
**Dr. Yankin Tanurhan** - VP Engineering, Synopsys

# ISQED Keynote 2P.1

Wednesday March 14

*9:00 AM - 9:45 AM*
Meeting Rooms 209/210

## Innovation in an Exponential World

**Nate Brese**
***DowDuPont***

The interplay of design objectives, regulatory disruptions, performance criteria and materials innovations have enabled electronic devices to evolve in accord with roadmaps, "laws" and correlations over the past half century. New opportunities to lower cost and improve performance have led designers into the third dimension where packaging offers miniaturization and efficiency gains. As we approach the tipping point for interconnected devices of all sorts, materials and design ingenuity are in high demand. This talk will focus on key market drivers and challenges facing our industry. We will discuss recent materials and design innovations required by emerging applications as well as the roadmaps guiding us into the future.

### About Nate Brese

Nate Brese is a Marketing Fellow in Strategic Marketing and Business Development within DowDuPont Electronics and Imaging. He currently leads acquisition and alliance strategy and has business development activities in a variety of high-growth market segments such as automotive, medical, and high-speed communication. Dr. Brese earned his B.A. in the Integrated Sciences Program at Northwestern Univ. and his Ph. D. in Solid State Chemistry from Arizona State Univ. He conducted postdoctoral research at the Max Planck Institut für Festkörperforschung in Stuttgart, Germany, and at Cornell Univ. He later completed the two-year Wharton Management Certification Program at Univ. Pennsylvania. As a research scientist and marketing professional at OSRAM Sylvania, Rohm and Haas, and Dow Electronic Materials, Nate has been instrumental in launching new products, creating business plans, assessing acquisition targets, and developing business opportunities in numerous areas, including phosphors, advanced packaging, industrial finishing, military optics, LEDs, and optical communication. He organized a Gordon Conference on Solid State Chemistry and a Materials Research Society Symposium on Solid State Chemistry. He is a member of the ACS, ECS, IEEE, MRS, and the Technical Committee of iNEMI. Nate is a co-inventor on over 20 US patents and co-author of 40 scientific papers.

# Embedded Tutorial 1

Tuesday March 13

*1:35 PM - 2:35 PM*
Meeting Rooms 209/210

## Power-Aware Testing in the Era of IoT

**Dr. Patrick Girard**
***LIRMM / CNRS - University of Montpellier / France***

Summary: Managing power consumption of circuits and systems is one of the most important challenges for the semiconductor industry in the era of IoT. Power management techniques are used today to control the power dissipation during functional operation. Since the application of these techniques has profound implications on manufacturing test, power-aware testing has become indispensable for low-power LSIs and IoT devices. This tutorial provides a comprehensive and practical coverage of power-aware testing. Its first part gives the background and discusses power issues during test. The second part provides comprehensive information on structural and algorithmic solutions for alleviating test-power-related problems. The third part outlines low- power design techniques and shows how low-power devices can be tested safely without affecting yield and reliability.

**About Patrick Girard**

Patrick GIRARD received a M.Sc. degree in Electrical Engineering and a Ph.D. degree in Microelectronics from the University of Montpellier, France, in 1988 and 1992 respectively. He is currently Research Director at CNRS (French National Center for Scientific Research) and works in the Microelectronics Department of the Laboratory of Informatics, Robotics and Microelectronics of Montpellier (LIRMM) - France. From 2010 to 2014, he was head of this Microelectronics Department. He is co-Director of the International Associated Laboratory « LAFISI » (French-Italian Research Laboratory on Hardware-Software Integrated Systems) created in 2013 by the CNRS and the University of Montpellier with the Politecnico di Torino, Italy. His research interests include all aspects of digital testing and memory testing, with emphasis on critical constraints such as timing and power. Reliability and fault tolerance are also part of his research activities. He has served on numerous conference committees and is the founder and Editor-in-Chief of the ASP Journal of Low Power Electronics (JOLPE). He is also an Associate Editor of the IEEE Transactions on Computers, IEEE Transactions on CAD and the Journal of Electronic Testing – Theory and Applications (JETTA - Springer). He has supervised 37 PhD dissertations and has published 7 books or book chapters, 65 journal papers, and more than 230 conference and symposium papers on these fields. Patrick Girard is a Fellow of IEEE.

# Embedded Tutorial 2

Tuesday March 13

*2:35 PM -3:35 PM*
Meeting Rooms 209/210

## Ambient Energy Harvesting Sensor Platform for Internet of Things: From Circuit to System

**Prof. Yongpan Liu**
***Tsinghua University, P.R. China***

Summary: Internet of things are regarded as a very promising market in the next decade. However, batteries have become as a critical obstacle due to their limited operating time and frequent maintenance. Energy harvesting techniques are proposed to relieve those problems and self-powered sensor nodes are attracting more and more attentions. A typical self-powered sensor node consists of power supply and computation system, and it collects energy from ambient power sources, such as solar, vibration, temperature difference and RF energy. Several major design challenges exist in the present self-powered sensor nodes: 1) Limited output power: The typical generated power ranges from several mW to hundreds of uW, leading to a gap of several orders of magnitude between the harvested energy and the consumption of mainstream low power chips. 2) Frequent power failures: Lots of power failures occur frequently in self-powered systems, requiring efficient operations in an energy intermittent mode. 3) Hard to predict: The power profiles are determined by the ambient factors and hard to be predicted. This tutorial will provide several state-of-the-art techniques from circuit levels to system levels to handle above challenges, including nonvolatile processor design, architecture exploration, software and system optimization techniques for energy harvesting sensor platform. Finally, we demonstrate a smart ultraviolet monitoring system using CNN-based pattern recognition on the platform.

**About Yongpan Liu**

Dr. Yongpan Liu received his B.S., M.S. and Ph.D. degrees from Electronic Engineering Department, Tsinghua University in 1999, 2002 and 2007. He was a visiting scholar at Pennsylvania State University in 2014. He is a key member of Tsinghua-Rohm Research Center and Research Center of Future ICs. He is now an associate professor in Dept. of Electronic Engineering Tsinghua University. His main research interests include nonvolatile computation, low power VLSI design, emerging circuits and systems and design automation. He has published over 100 peer-reviewed conference and journal papers and led over 6 chip design projects for sensing applications, including the first nonvolatile processor (THU1010N). His research is supported by NSFC, 863, 973 Program and Industry Companies such as Huawei, Rohm, Intel and so on. These projects lead to the first nonvolatile processor THU1010N and a series of advanced versions. The line of processors has been adopted for the research of self-powered sensing platforms in 7 universities His work has received Under 40 Young Innovators Award DAC 2017, Micro Top Pick 2016, Best Paper Award in ASPDAC2017, HPCA 2015, 2 Design Contest Awards in ISLPED 2012 and 2013, and 2 Best Paper Nominations in ASPDAC 2013 and 2016. He holds 7 authorized Chinese patents and 1 authorized U.S. patent.

# Embedded Tutorial 3

Wednesday March 14

*1:30 PM - 2:30 PM*
Meeting Rooms 209/210

## Ultra-Low-Power Digital Architectures for the Internet of Things

**Prof. Prof. Davide Rossi**
***DEI, University of Bologna***

Summary: A growing number of Internet of Things (IoT) applications require flexible processing of data streams generated by multiple sensors, such as accelerometers, low-resolution cameras, microphone arrays, and vital signs monitors. These applications share the need for high performance and extreme energy efficiency in a power envelope of a few milliWatts, while keeping the flexibility of software programmable architectures to deal to the vast variety of near-sensor data analytics algorithms. This tutorial presents an overview of the emerging architectures implementing the digital processing and control platforms for Internet of things applications. It will provide a review of the state of the art Ultra-Low-Power (ULP) micro-controllers architectures, highlighting main challenges and perspectives, and introducing the potential of exploiting parallel near-threshold computing in this field currently dominated by single-issue processors.

**About Davide Rossi**

David Rossi received the PhD from the University of Bologna, Italy, in 2012. He has been a post doc researcher in the Department of Electrical, Electronic and Information Engineering "Guglielmo Marconi" at the University of Bologna since 2015, where he currently holds an assistant professor position. His research interests focus on energy efficient digital architectures in the domain of heterogeneous and reconfigurable multi and many-core systems on a chip. This includes architectures, design implementation strategies, and runtime support to address performance, energy efficiency, and reliability issues of both high end embedded platforms and ultra-low-power computing platforms targeting the IoT domain. In this fields he has published more than 60 paper in international peer-reviewed conferences and journals.

# Embedded Tutorial 4

Wednesday March 14

*2:30 PM - 3:30 PM*
Meeting Rooms 209/210

## Managing the ever increasing complexity of Cyber-Physical Systems in High-Tech Industry

**Dr. Wouter Leibbrandt**
***Embedded Systems Innovation, TNO, The Netherlands***

Summary: The complexity of advanced cyber-physical systems is ever increasing, making it progressively more difficult to design in a proper and efficient way for system properties such as e.g. performance, reliability, upgradability, safety and security. High tech cyber-physical systems as diverse as industrial printers, cars, medical imaging and IC-manufacturing equipment often contain hundreds of processing elements, tens of millions of lines-of-code, with thousands of interfaces. The same holds for distributed systems like IoT. Architects and designers are rapidly losing grip and overview. A more fundamental basis of embedded systems engineering is being developed to address these issues and starting to be applied. This Model-Based Systems Engineering (MBSE) approach aims at reasoning about non-functional, system, properties such as performance from the highest system architecture level down to the engineering level for individual components. Objective is to assure that in the end system requirements and stakeholder needs are fulfilled, and that components and systems can be tested and validated in a meaningful way. In this tutorial we introduce some of the key principles, such as executable models and domain specific languages, and concerns of MBSE, and present examples from the car entertainment and industrial printing domains. Furthermore, we discuss the current developments which will further increase complexity of cyber-physical systems in the near future, such as autonomous systems and adaptive and learning systems.

**About Wouter Leibbrandt**

Wouter Leibbrandt is general manager of the Embedded Systems Innovation department in TNO (TNO-ESI). TNO-ESI focusses on the development of new methods and techniques for design and engineering of increasingly complex high-tech (embedded) systems. It does so in strong partnership and close collaboration with leading high-tech companies such as ASML, Philips, Thales, NXP, Océ, Thermo-Fisher and DAF as well as with leading academic groups in the Netherlands and across Europe. Until early 2016 Wouter was with NXP Semiconductors for 10 years, where he managed the Advanced Applications Lab, investigating new application concepts around future advanced silicon products, driving secure connections for a smarter world. The recurring theme here is that everything is getting connected with everything (IoT). Before joining NXP, he was with Philips Research labs for 14 years, managing a variety of projects and departments. From 2004 to 2006 he lived and worked in China, founding and managing part of the Philips Research labs in Shanghai. Wouter holds a PhD in physics from Utrecht University.

# SESSION 1A

**Tuesday March 13**

## Design Verification and Test

Chair: **Vinod Viswanath**, Real Intent
Co-Chair: **Sreejit Chakravarty**, Intel

*10:00AM*
**1A.1**
**Concolic Testing of SystemC Designs**
*Bin Lin[1], Kai Cong[2], Zhenkun Yang[2], Zhigang Liao[3], Tao Zhan[4], Christopher Havlicek[1], Fei Xie[1]*
[1]Portland State University, [2]Intel Corporation, [3]Virtual Device Technologies LLC, [4]Northwestern Polytechnical University

*10:20AM*
**1A.2**
**A Droop Measurement Built-in Self-Test Circuit for Digital Low-Dropout Regulators**
*Aydin Dirican, Cagatay Ozmen, Martin Margala*
University of Massachusetts Lowell

*10:40AM*
**1A.3**
**Test Set Identification for Improved Delay Defect Coverage in the Presence of Statistical Delays**
*Pavan Kumar Javvaji[1], Basim Shanyour[2], Spyros Tragoudas[1]*
[1]Southern Illinois University Carbondale, [2]Southern Illinois University- Carbondale

*11:00AM*
**1A.4**
**Augmenting ESD and EOS Physical Analysis with Per Pin ESD and Leakage DFT**
*Horaira Abu, Salem Abdennadher, Benoit Provost, Harry Muljono*
Intel Corporation

# SESSION 1B

**Tuesday March 13**

## System-level Design and Methodologies (SDM)

Chair: **Rajesh Berigei**, Consultant
Co-Chair: **Jingtong Hu**, University of Pittsburgh

*10:00AM*
**1B.1**
**Hybrid-Comp: A Criticality-Aware Compressed Last-Level Cache**
*Amin Jadidi[1], Mohammad Arjomand[2], Mahmut Kandemir[1], Chita Das[1]*
[1]Pennsylvania State University, [2]Georgia Institute of technology

*10:20AM*
**1B.2**
**Energy-Optimal Dynamic Voltage Scaling in Multicore Platforms with Reconfigurable Power Distribution Network**
*Juyeon Kim[1] and Taewhan Kim[2]*
[1]Samsung Electronics, [2]Seoul National University

*10:40AM*
**1B.3**
**Optimizing Energy in a DRAM based Hybrid Cache**
*Jiacong He[1] and Joseph Callenes-Sloan[2]*
[1]University of Texas at Dallas, [2]California Polytechnic State University

*11:00AM*
**1B.4**
**Program Acceleration Using Nearest Distance Associative Search**
*Mohsen Imani[1], Daniel Peroni[2], Tajana Rosing[3]*
[1]University of California San Diego, [2]University of California at San Diego, [3]UCSD

# SESSION 1C

**Tuesday March 13**

## Emerging Logic and Memory Technologies in IoT and Neuromorphic Architectures

Chair: **Shih-Hung Chen**, IMEC
Co-Chair: **Jayita Das**, Intel Corporation

*10:00AM*
**1C.1**
**Synthesis of Normally-Off Boolean Circuits: An Evolutionary Optimization Approach Utilizing Spintronic Devices**
*Arman Roohi, Ramtin Zand, Ronald F DeMara*
Computer Systems and Architecture Laboratory, Department of EECS, University of Central Florida

*10:20AM*
**1C.2**
**LUPIS : Latch-Up Based Ultra Efficient Processing-in-Memory System**
*Joonseop Sim[1], Mohsen Imani[1], Woojin Choi[1], Yeseong Kim[2], Tajana Rosing[1]*
[1]UCSD, [2]University of California San Diego

*10:40AM*
**1C.3**
**Energy efficient neuromorphic processing using spintronic memristive device with dedicated synaptic and neuron terminology**
*Zoha Pajouhi*
Intel Corporation

*11:00AM*
**1C.4**
**A Bi-Memristor Synapse with Spike-Timing-Dependent Plasticity for On-Chip Learning in Memristive Neuromorphic Systems**
*Sagarvarma Sayyaparaju, Sherif Amer, Garrett S. Rose*
The University of Tennessee, Knoxville

# SESSION 2A

**Tuesday March 13**

## Automated Analog and Digital Circuit Optimization

Chair: **Srini Krishnamoorthy**, AMD
Co-Chair: **Srinivas Katkoori**, University of South Florida

*3:45PM*
**2A.1**
**Recognition of Regular Layout Structures**
*Yu-Cheng Chiang, Shr-Cheng Tsai, Rung-Bin Lin*
Yuan Ze University

*4:05PM*
**2A.2**
**A Simplified Methodology for Complex Analog Module Layout Generation**
*Pradeep Chawda*
Texas Instruments

*4:25PM*
**2A.3**
**Process Variation Aware D-Flip-Flop Design using Regression Analysis**
*Shinichi Nishizawa[1] and Hidetoshi Onodera[2]*
[1]Saitama University, [2]Kyoto University

*4:45PM*
**2A.4**
**Clock Buffer and Flip-flop Co-optimization for Reducing Peak Current Noise**
*Joohan Kim[1] and Taewhan Kim[2]*
[1]Samsung Electronics, [2]Seoul National University

*5:05PM*
**2A.5**
**Parasitic-Aware gm/ID-Based Many-Objective Analog/RF Circuit Sizing**
*Tuotian Liao[1] and Lihong Zhang[2]*
[1]Memorial University of Newfoundland, [2]Memorial University of Newfoundlan

# SESSION 2B

**Tuesday March 13**

## System-level Design and Methodologies (SDM)

Chair: **Rajesh Berigei**, Consultant
Co-Chair: **Jingtong Hu**, University of Pittsburgh

*3:45PM*
**2B.1**
**A Loop Structure Optimization targeting High-level Synthesis of Fast Number Theoretic Transform**
*Kazushi Kawamura, Masao Yanagisawa, Nozomu Togawa*
Waseda University

*4:05PM*
**2B.2**
**A 4-PAM Interconnect in Network-on-Chip for High-Throughput and Latency-Sensitive Applications**
*Ahmad Mansour[1], Ahmed Elnaggar[1], Bassma Alabassy[2], Mostafa Khamis[2], Ahmed Shalaby[3]*
[1]EE Department, Alexandria University, Egypt., [2]Mentor Graphics, [3]Faculty of Computers and Informatics, Benha University, Egypt

*4:25PM*
**2B.3**
**Comparative Study and Prediction Modeling of Photonic Ring Network on Chip Architectures**
*Sara Karimi[1] and Jelena Trajkovic[2]*
[1]M.Sc Concordia University, [2]Assistant Professor in Concordia University

*4:45PM*
**2B.4**
**Power and Performance Aware Memory-Controller Voting Mechanism**
*Milena Vratonjic[1], Harmander Singh[2], Gautam Kumar[3], Roumi Mohamed[3], Ashish Bajaj[3], Ken Gainey[1]*
[1]Qualcomm Atheros, Inc., [2]Qualcomm Technologies Inc., [3]Qualcomm India Private Limited

*5:05PM*

**2B.5**

**PDA-HyPAR: Path-Diversity-Aware Hybrid Planar Adaptive Routing Algorithm for 3D NoCs**

*Jindun Dai[1], Renjie Li[2], Xin Jiang[3], Takahiro Watanabe[4]*

[1]Shanghai Jiao Tong University, [2]The Graduate School of Information Production and Systems, Waseda University, [3]Graduate School of Information Production and Systems, Waseda University, Japan, [4]The Graduate School of Information, Production and Systems Of Waseda University, Japan

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# SESSION P/Session 2C

**Tuesday March 13**

## Posters

Chair: **Swaroop Ghosh**, Pennsylvania State University

*5:55PM*
**P1**
**Network on Interconnect Fabric**
*Boris Vaisband, Adeel Bajwa, Subramanian Iyer*
University of California, Los Angeles

*5:55PM*
**P2**
**Efficient K Nearest Neighbor Algorithm Implementations for Throughput-Oriented Architectures**
*Jihyun Ryoo[1], Meena Arunachalam[2], Rahul Khanna[2], Mahmut Kandemir[1]*
[1]Pennsylvania State University, [2]Intel

*5:55PM*
**P3**
**Body-Biasing Assisted Vmin Optimization for 5nm-Node Multi-Vt FD-SOI 6T-SRAM**
*Jheng-Yi Chen, Ming-Yu Chang, Shi-Hao Chen, Jia-Wei Lee, Meng-Hsueh Chiang*
National Cheng Kung University

*5:55PM*
**P4**
**Measuring the effectiveness of ISO26262 compliant Self Test Library**
*Frederico Pratas, Thomas Dedes, Andrew Webber, Majid Bemanian, Itai Yarom*
MIPS

*5:55PM*
**P5**
**An Online Framework for Diagnosis of Multiple Defects in Scan Chains**
*Sarmad Tanwir[1], Michael Hsiao[1], Loganathan Lingappan[2]*
[1]Virginia Tech, [2]Intel Corporation

*5:55PM*
**P6**
**Routing at Compile Time**
*Chun-Xun Lin, Tsung-Wei Huang, Martin Wong*
University of Illinois at Urbana-Champaign

*5:55PM*
**P7**
**Uncertainty Aware Mapping of Embedded Systems for Reliability, Performance, and Energy**
*Wenkai Guan, Milad Ghorbani Moghaddam, Cristinel Ababei*
Marquette University

*5:55PM*
**P8**
**On the Write Energy of Non-Volatile Resistive Crossbar Arrays With Selectors**
*Albert Ciprut and Eby G. Friedman*
University of Rochester

*5:55PM*
**P9**
**A Modified Method of Logical Effort for FinFET Circuits Considering Impact of Fin-Extension Effects**
*Archana Pandey[1], Pitul Garg[2], Shobhit Tyagi[2], Rajeev Ranjan[3], Anand Bulusu[2]*
[1]Indian Institute of Technology Roorkee, [2]IIT Roorkee, [3]Samsung Electronics, Republic of Korea

*5:55PM*
**P10**
**Generic System-Level Modeling and Optimization for Beyond CMOS Device Applications**
*Victor Huang, Chenyun Pan, Azad Naeemi*
Georgia Institute of Technology

*5:55PM*
**P11**
**Terahertz Travelling Wave Amplifier Design using Ballistic Deflection Transistor**
*Huan Wang[1], Jean-François Millithaler[1], Ronald Knepper[2], Martin Margala[1]*
[1]University of Massachusetts, [2]Boston University

*5:55PM*
**P12**
**Reliable Memory PUF Design for Low-Power Applications**
*Mohammad Saber Golanbari, Saman Kiamehr, Rajendra Bishnoi, Mehdi Tahoori*
Karlsruhe Institute of Technology

*5:55PM*
**P13**
**An ESD Transient Clamp with 494 pA Leakage Current in GP 65 nm CMOS Technology**
*Mahdi Elghazali, Manoj Sachdev, Ajoy Opal*
University of Waterloo

*5:55PM*
**P14**
**Enhancing Circuit Operation using Analog Floating Gates**
*Ujas Patel[1], Sai Govinda Rao Nimmalapudi[1], Harvey Stiegler[1], Andrew Marshall[1], Keith Jarreau[2]*
[1]University of Texas at Dallas, [2]Texas Instruments Incorporated

*5:55PM*
**P15**
**An Automated Flow for Design Validation of Switched Mode Power Supply**
*Pradeep Chawda[1] and Srikrishna Srinivasan[2]*
[1]Texas Instruments, [2]Texas Instruments Inc

*5:55PM*
**P16**
**Dynamic NoC Platform for Varied Application Needs**
*Sidhartha Sankar Rout[1], Hemanta Kumar Mondal[2], Rohan Juneja[1], Sri Harsha Gade[1], Sujay Deb[1]*
[1]IIIT Delhi, [2]University of Southern Brittany, Lab STICC, Lorient, france

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# SESSION 3A.1

**Wednesday March 14**

## Design Verification and Test

Chair: **Vinod Viswanath**, Real Intent
Co-Chair: **Sreejit Chakravarty**, Intel

*10:00AM*
**3A.1.1**
**A Technique to Aggregate Classes of Analog Fault Diagnostic Data Based on Association Rule Mining**
*Ruslan Dautov[1] and Sergey Mosin[2]*
[1]Shenzhen University, [2]Kazan Federal University

*10:20AM*
**3A.1.2**
**Extracting Hardware Assertions Including Word-Level Relations over Multiple Clock Cycles**
*Mami Miyamoto and Kiyoharu Hamaguchi*
Shimane University

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# SESSION 3A.2

**Wednesday March 14**

## Automated Analog and Digital Circuit Optimization

Chair: **Srini Krishnamoorthy**, AMD
Co-Chair: **Srinivas Katkoori**, University of South Florida

*10:40AM*
**3A.2.1**
**A Study on NBTI-induced Delay Degradation Considering Stress Frequency Dependence**
*Zuitoku Shin[1], Shumpei Morita[1], Song Bian[1], Michihiro Shintani[2], Masayuki Hiromoto[1], Takashi Sato[1]*
[1]Kyoto University, [2]Nara Institute of Science and Technology

*11:00AM*
**3A.2.2**
**Verification Methodology to Guarantee Low Routing Resistance to Well Taps**
*MOHAMMED FAKHRUDDIN, Kuok-Khian Lo, James Karp, Michael Hart, Min-Hsing Chen*
Xilinx, Inc.

# SESSION 3B

**Wednesday March 14**

## High Performance / Low Power Logic Design

Chair: **Kurt Schwartz**, Texas Instruments, Inc
Co-Chair: **Jose Pineda de Gyvez**, Eindhoven Univ of Technology

*10:00AM*
**3B.1**
**Ultra-Low Swing CMOS Transceiver for 2.5-D Integrated Systems**
*Przemyslaw Mroszczyk and Vasilis Pavlidis*
The University of Manchester

*10:20AM*
**3B.2**
**Back-Bias Generator for Post-Fabrication Threshold Voltage Tuning Applications in 22nm FD-SOI Process**
*Arif Siddiqi, Navneet Jain, Mahbub Rashed*
Global Foundries

*10:40AM*
**3B.3**
**Logic-based Row Redundancy Technique Designed in 7nm FinFET Technology for Embedded SRAMs**
*Vivek Nautiyal, Nishant Nukala, Fakhruddinali Bohra, Sagar Dwivedi, Jitendra Dasani, Satinderjit Singh, Gaurav Singla, Martin Kinkade Kinkade*
ARM

*11:00AM*
**3B.4**
**A 125mV 2ns-Access-Time 16Kb SRAM Design based on a 6T Hybrid TFET-FinFET Cell**
*Hassan Afzali-Kusha[1], Alireza Shafaei Bejestan[2], Massoud Pedram[1]*
[1]USC, [2]University of Southern California

# SESSION 3C

**Wednesday March 14**

## IoT & Smart Sensors

Chair: **Pradeep Chawda**, Texas Instruments, Inc
Co-Chair: **Ali A. Shahi**, Globalfoundaries

*10:00AM*
**3C.1**
**New AC Resistance Calculation of Printed Spiral Coils for Wireless Power Transfer**
*Gaorong Qian, Yuhua Cheng, Guoxiong Chen, Gaofeng Wang*
Hangzhou Dianzi University

*10:20AM*
**3C.2**
**An Automated Design Flow for Synthesis of Optimal Multi-layer Multi-shape PCB Coils for Inductive Sensing Applications**
*Pradeep Chawda*
Texas Instruments

*10:40AM*
**3C.3**
**When "things" get older - Exploring Circuit Aging in IoT Applications**
*Xinfei Guo, Vaibhav Verma, Patricia Gonzalez-Guerrero, Mircea Stan*
University of Virginia

# SESSION 4A.1

**Wednesday March 14**

## Design Technology Co-Optimization

Chair: **Aswin Mehta**, Texas Instruments, Inc
Co-Chair: **Rajan Beera**, Pall Corporation

*11:40AM*
**4A.1.1**
**A systematic study of hotspot detection in physical designs using machine learning**
*Piyush Verma[1], Robert Pack[2], Sriram Madhavan[2]*
[1]Globalfoundries Inc., [2]Globalfoundaries

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# SESSION 4A.2

**Wednesday March 14**

## Machine Learning on Conventional and Emerging Platforms

Chair: **Yang (Cindy) Yi**, Virginia Tech
Co-Chair: **Aswin Mehta**, Texas Instruments, Inc.

*12:00PM*
**4A.2.1**
**A Deep Learning Based Approach for Analog Hardware Implementation of Delayed Feedback Reservoir Computing System**
*Jialing Li, Kangjun Bai, Lingjia Liu, Yang Yi*
Virginia Tech

*12:20PM*
**4A.2.2**
**An Area and Energy Efficient Design of Domain-Wall Memory-Based Deep Convolutional Neural Networks using Stochastic Computing**
*Xiaolong Ma[1], Yipeng Zhang[1], Geng Yuan[1], Ao Ren[1], Zhe Li[1], Jie Han[2], Jingtong Hu[3], Yanzhi Wang[1]*
[1]Syracuse University, [2]university of alberta, [3]University of Pittsburgh

*12:40PM*
**4A.2.3**
**A Path to Energy-efficient Spiking Delayed Feedback Reservoir Computing System for Brain-inspired Neuromorphic Processors**
*Kangjun Bai[1] and Yang Yi[2]*
[1]Virginia Tech, [2]Department of Electrical and Computer Engineering, Virginia Tech

# SESSION 4B

**Wednesday March 14**

## High Performance / Low Power Logic Design

Chair: **Jose Pineda de Gyvez**, Eindhoven Univ of Technology
Co-Chair: **Raviprakash Rao**, Texas Instruments, Inc

*11:40AM*
**4B.1**
**Low Power Latch Based Design with Smart Retiming**
*Kamlesh Singh[1], Hailong Jiao[2], Jos Huisken[3], Hamed Fatemi[4], Josè Pineda de Gyvez[4]*
[1]Eindhoven University of Technology (TU/e), [2]Peking University Shenzhen Graduate School Shenzhen, China, [3]Eindhoven University of Technology, The Netherlands, [4]NXP Semiconductors, The Netherlands

*12:00PM*
**4B.2**
**Parallel implementation of finite state machines for reducing the latency of stochastic computing**
*Cong Ma and David Lilja*
University of Minnesota

*12:20PM*
**4B.3**
**A Post-Silicon Hold Time Closure Technique using Data-Path Tunable-Buffers for Variation-Tolerance in Sub-threshold Designs**
*Divya Akella Kamakshi[1], Xinfei Guo[1], Harsh Patel[1], Mircea Stan[2], Benton Calhoun[1]*
[1]University of Virginia, [2]

*12:40PM*
**4B.4**
**A Low-Power Configurable Adder for Approximate Applications**
*Tongxin Yang, Tomoaki Ukezono, Toshinori Sato*
Fukuoka University

# SESSION 4C

**Wednesday March 14**

## IoT & Smart Sensors

Chair: **Pradeep Chawda**, Texas Instruments, Inc
Co-Chair: **Ali A. Shahi**, Globalfoundaries

*11:40AM*
**4C.1**
**Mathematical Derivation, Circuits Design and Clinical Experiments of Measuring Blood Flow Volume (BFV) at Arteriovenous Fistula (AVF) of Hemodialysis (HD) Patients Using a Newly-Developed Photoplethysmography (PPG) Sensor**
*Paul (C.P.) Paul*
National Chiao Tsung University

*12:00PM*
**4C.2**
**A Wireless Multifunctional Monitoring System of Tower Body Running State Based on MEMS Acceleration Sensor**
*Linxi Dong, Haonan Wang, Gaofeng Wang, Weimin Qiu*
Hangzhou Dianzi University

*12:20PM*
**4C.3**
**Power Management Factors and Techniques for IoT Design Devices**
*Anupriya Prasad and Pradeep Chawda*
Texas instruments

*12:40PM*
**4C.4**
**Hierarchical Dynamic Goal Management for IoT Systems**
*Axel Jantsch[1], Arman Anzanpour[2], Hedyeh Kolerdi[1], Iman Azimi[2], Lydia Chaido Siafara[1], Amir M. Rahmani[3], Nima TaheriNejad[1], Pasi Liljeberg[2], Nikil Dutt[4]*
[1]TU Wien, [2]University of Turku, [3]University of California Irvine & TU Wien, [4]UC Irvine

# SESSION 5A

**Wednesday March 14**

## Machine Learning on Conventional and Emerging Platforms

Chair: **Yang (Cindy) Yi**, Virginia Tech
Co-Chair: **Aswin Mehta**, Texas Instruments, Inc.

*3:40PM*
**5A.1**
**Quantized Neural Networks with New Stochastic Multipliers**
*Bingzhe Li[1], MohammadHassan Najafi[1], Bo Yuan[2], David Lilja[1]*
[1]University of Minnesota-twin cities, [2]City University of New York

*4:00PM*
**5A.2**
**High Performance Training of Deep Neural Networks Using Pipelined Hardware Acceleration and Distributed Memory**
*Raghav Mehta[1], Yuyang Huang[2], Mingxi Cheng[3], Shrey Bagga[4], Nishant Mathur[4], Ji Li[4], Jeffrey Draper[5], Shahin Nazarian[4]*
[1]Mentor, A Siemens Business, [2]NVIDIA, [3]Duke University, [4]University Of Southern California, [5]Information Sciences Institute

*4:20PM*
**5A.3**
**Deep Neural Network Acceleration Framework Under Hardware Uncertainty**
*Mohsen Imani[1], Pushen Wang[1], Tajana Rosing[2]*
[1]University of California San Diego, [2]UCSD

*4:40PM*
**5A.4**
**A Hardware-Friendly Algorithm for Scalable Training and Deployment of Dimensionality Reduction Models on FPGA**
*Mahdi Nazemi[1], Amir Erfan Eshratifar[2], Massoud Pedram[1]*
[1]USC, [2]University of Southern California

# SESSION 5B

## Wednesday March 14

## Hardware Security: PUF, Obfuscation, and Trojan Detection

Chair: **Jon Nafziger**, Texas Instruments, Inc
Co-Chair: **Swaroop Ghosh**, Pennsylvania State University

*3:40PM*
**5B.1**
**Securing FPGA-based Obsolete Component Replacement for Legacy Systems**
*Zhiming Zhang[1], Laurent Njilla[2], Charles Kamhoua[3], Kevin Kwiat[2], Qiaoyan Yu[1]*
[1]University of New Hampshire, [2]Cyber Assurance Branch, Air Force Research Laboratory, [3]Army Research Laboratory

*4:00PM*
**5B.2**
**High-Level Synthesis of Key Based Obfuscated RTL Datapaths**
*Sheikh Ariful Islam and Srinivas Katkoori*
University of South Florida

*4:20PM*
**5B.3**
**Double Error Cellular Automata-Based Error Correction with Skip-mode Compact Syndrome Coding for Resilient PUF Design**
*Anthony Mattar El Raachini[1], Hussein Alawieh[1], Adam Issa[2], Zainab Swaidan[1], Rouwaida Kanj[1], Ali Chehab[1], Mazen Saghir[1]*
[1]American University of Beirut, [2]University of Toronto

*4:40PM*
**5B.4**
**Design and Evaluation of Physical Unclonable Function for Inorganic Printed Electronics**
*Ahmet Turan Erozan[1], Mohammad Saber Golanbari[1], Rajendra Bishnoi[1], Jasmin Aghassi-Hagmann[2], Mehdi Tahoori[1]*
[1]Karlsruhe Institute of Technology, [2]Karlsruhe Institute of Technology, Offenburg University of Applied Sciences

# SESSION 5C

## Wednesday March 14

## Demystifying self-driving cars

Chair: **Jayita Das**, Intel Corporation

*3:40PM*
**5C.1**
**Near-Future Traffic Evaluation based Navigation for Automated Driving Vehicles Considering Traffic Uncertainties**
*Kuen-Wey Lin[1], Masanori Hashimoto[2], Yih-Lang Li[1]*
[1]National Chiao Tung University, [2]Osaka University

*4:05PM*
**5C.2**
**Low cost & power CNN/Deep learning solution for Automated Driving**
*Mihir Mody, Kumar Desappan, Pramod Swami, Manu Mathew, Soyeb Nagori*
Texas Instruments, Inc

*4:30PM*
**5C.3**
**Resource Constrained Cellular Neural Networks for Real-time Obstacle Detection using FPGAs.**
*Yiyu Shi[1], Xiaowei Xu[2], Tianchen Wang[1], Qing Lu[1]*
[1]University of Notre Dame, [2]Huazhong university of science and techonology

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