Ramping New Products Yields in the Deep Submicron Age

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PDF Solutions, Inc.

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Major Points

- Increasing design and process complexity becoming critical factor leading to yield loss
- Systematic yield loss component is significant, growing, and recoverable
- Fundamental new approach, focused on integration between design, process and manufacturing, is required to recover yield loss

Outline

- Product Yield Ramps: the market pressures
- The Design-Manufacturing Integration Problem
- Solution
- Examples
- Concluding remarks

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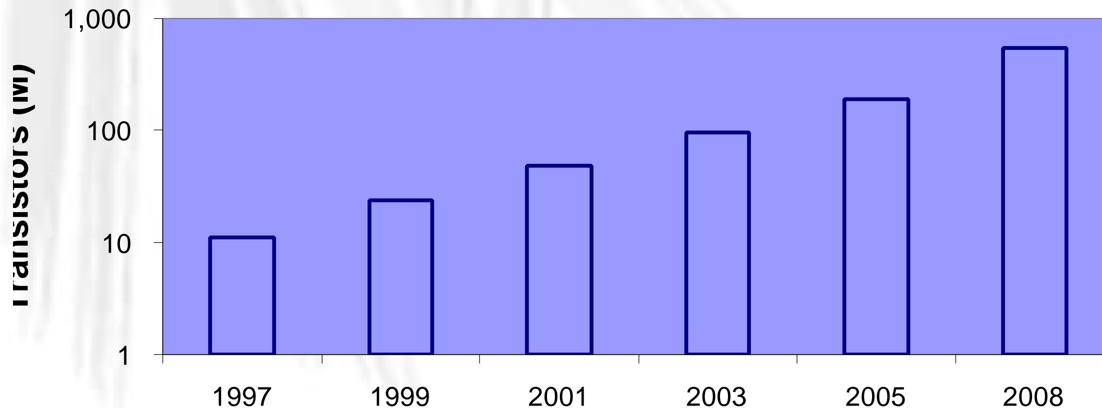
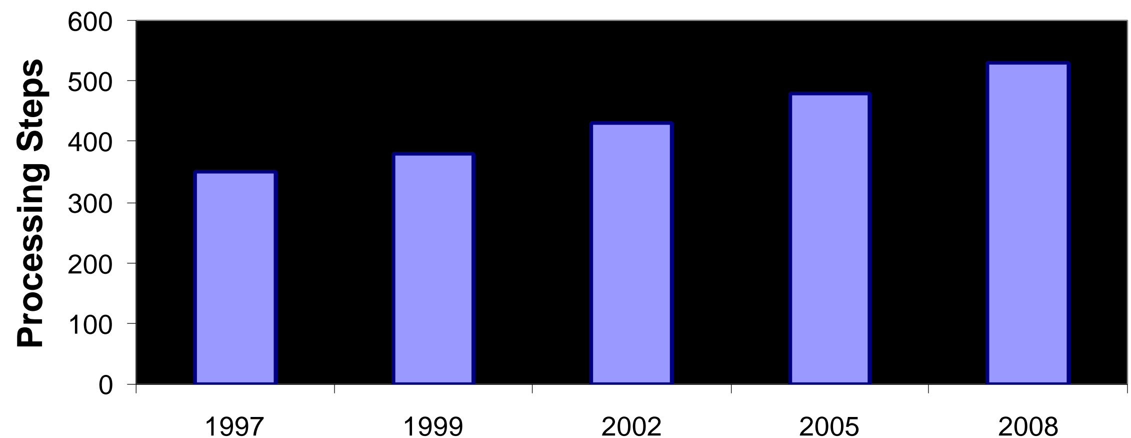
Complexity is Increasing Across the Board



IP Reuse is Critical to Get Designs to Market Faster

Unless Corrected, Increased Processing Complexity Reduces Yield up to 5% per Year



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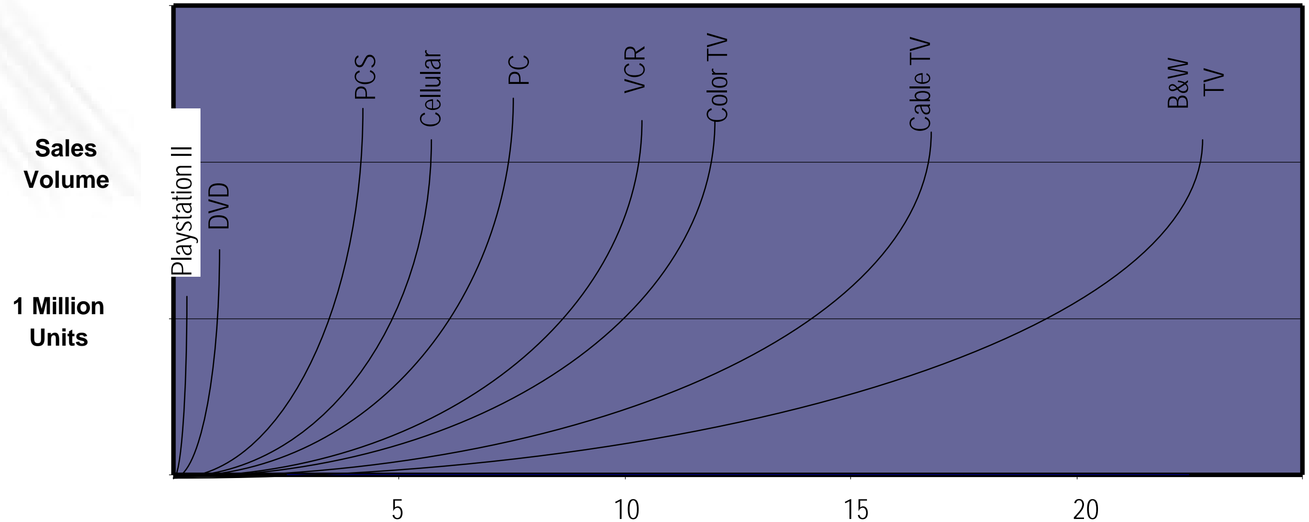
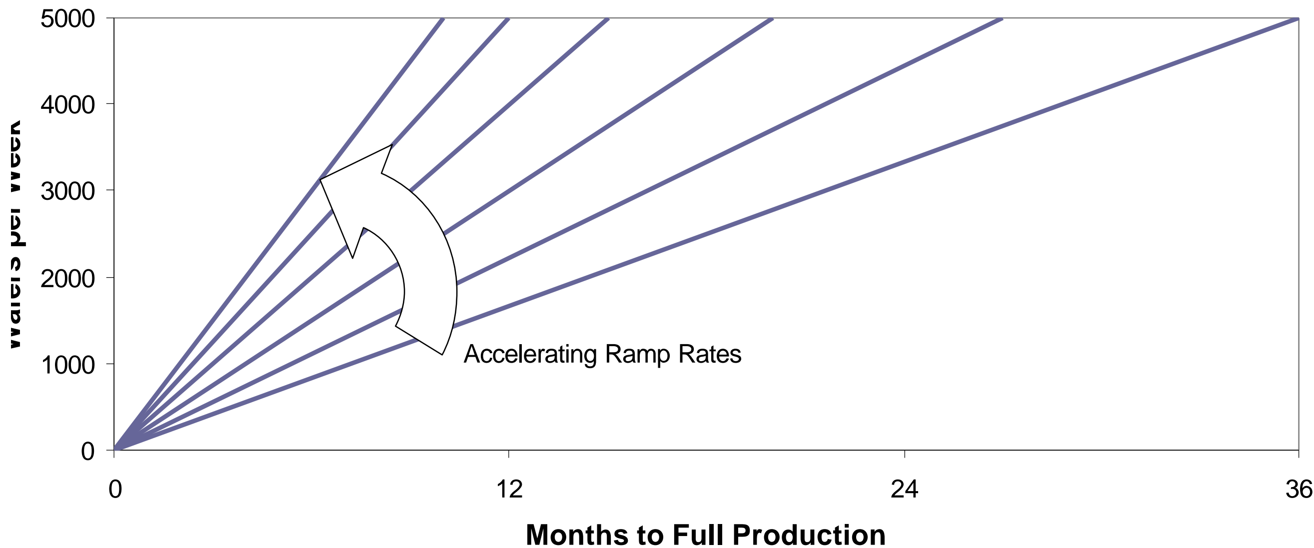
The Window is Tightening

The demand is accelerating





There is less time to bring up the volume

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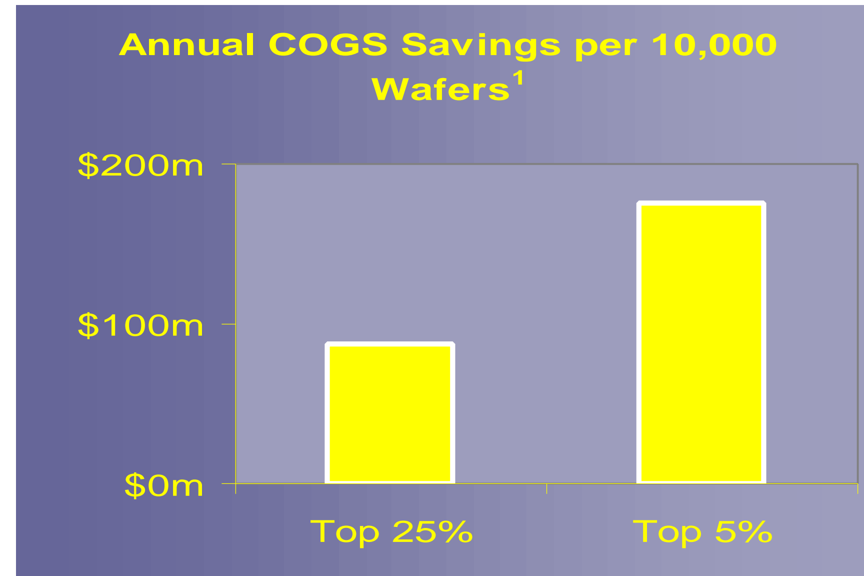
Missing the Window is Expensive

Three costs:

- Lost market share
- Increased NRE
- Increased Costs of Goods Sold (COGS)



Integration effects market entry point, performance, and cost basis

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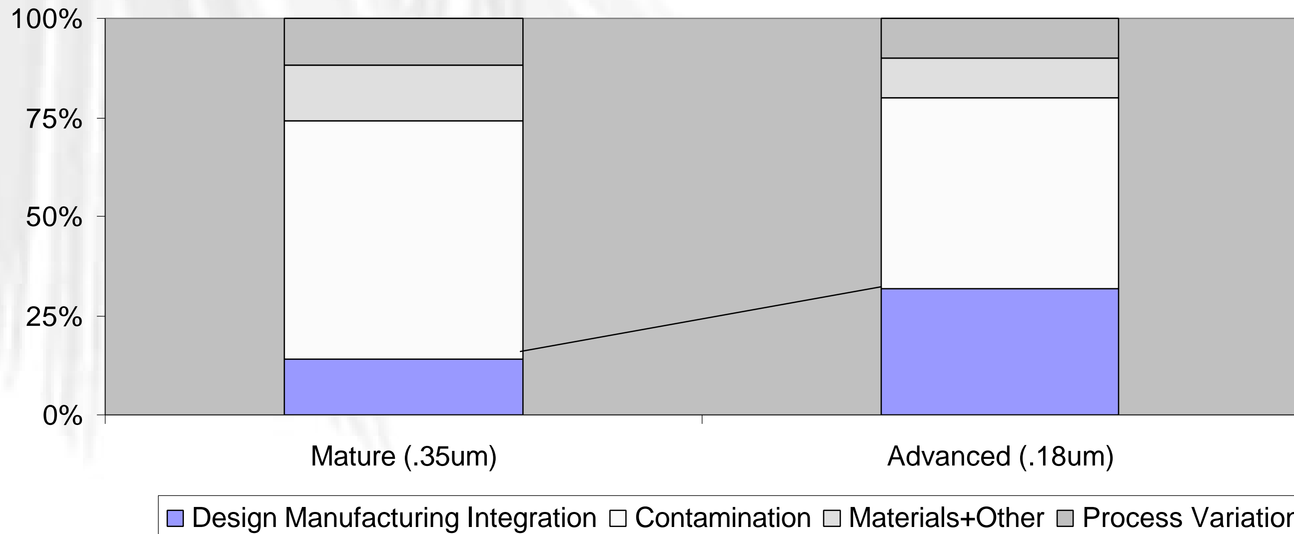
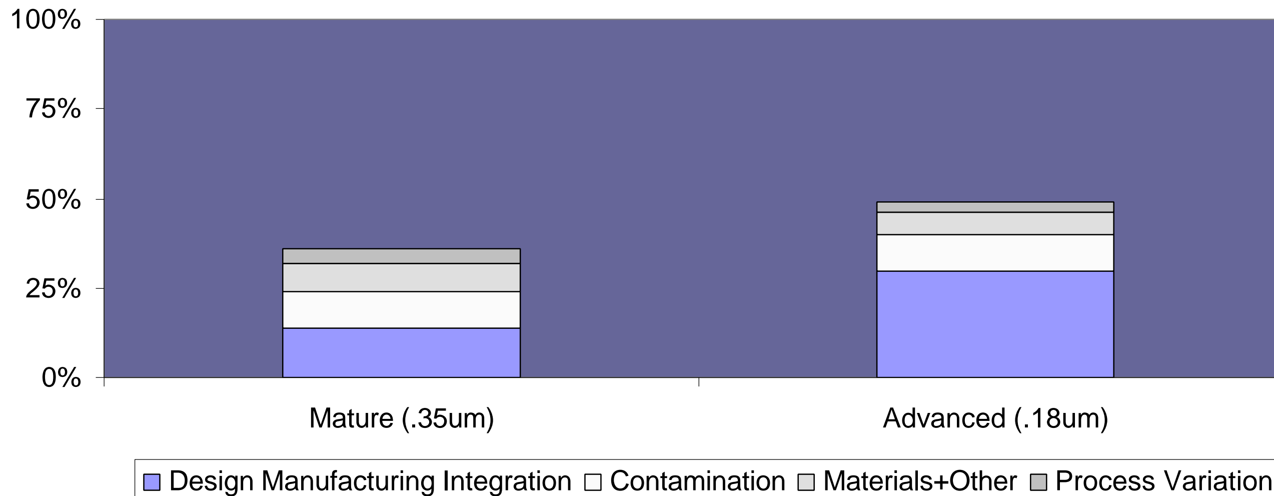
And Those Yield Loss $$$ are Recoverable ...



Bad News:
Integration Issues Now Account for 30% of Yield Loss During Ramp



Good News:
Nearly All Integration Related Loss is Recoverable

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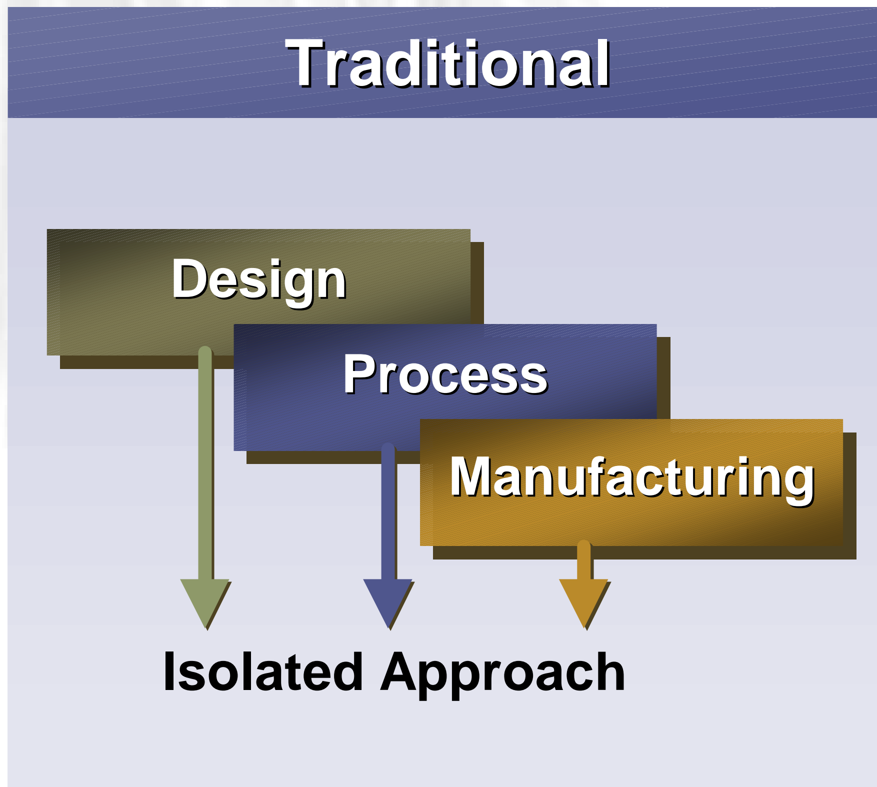
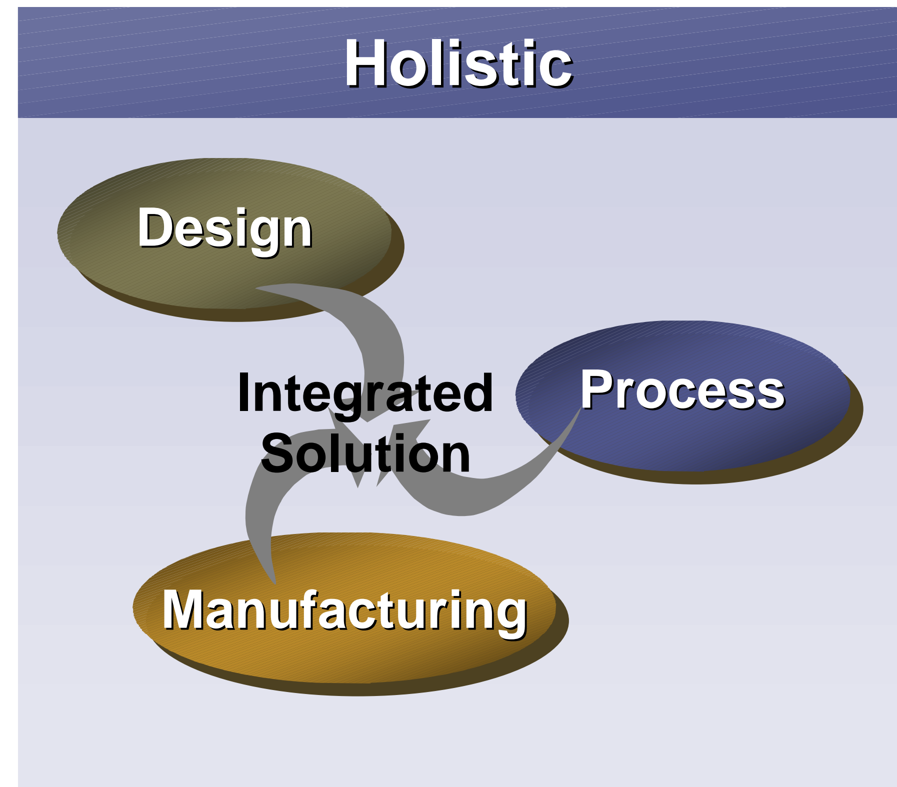
… but, an Integrated Approach is Required





"Ask yourself this: Why does a MIPS core cost 25 cents, and you go to QED and there's a 100-fold increase in value? … the QED part is worth $25 because it is implemented in silicon."

— Rob Chaplinsky, general partner of Mohr Davidow Ventures

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Technical Issues Have Both Design and Manufacturing Implications

New Technology	Impact on Design / Manufacturing Interface	Compensation	Design – Manufacturing Issue
Chemical Mechanical Polishing (CMP)	• ILD Variability • Depth of focus • Capacitance variability	• Dummy fill • Increased design margin	• What is the circuit performance impact? • What is the optimal dummy fill strategy?
I-Line @ 0.35µm DuV @ 0.25µm and below	• Large w/in chip line width variation	• Optical Proximity Correction	• Printability verification after OPC? • Gap fill issues?
Channel & Source Drain Engineering RTA, Tox, Poly CD	• Increased relative variability of transistor performance	• Statistical design • Increase margins	• Traditional worst case corners not valid
Re-use of large design cores	• Debugging product yield issues	• Black box yield models	• Fault localization difficult

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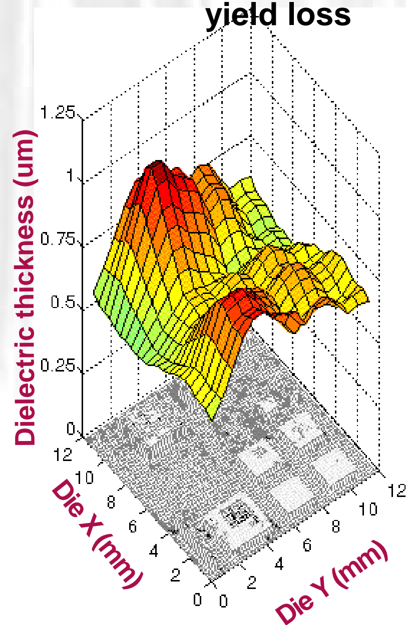
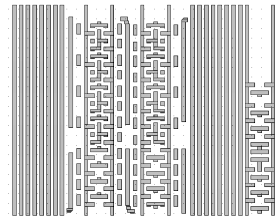
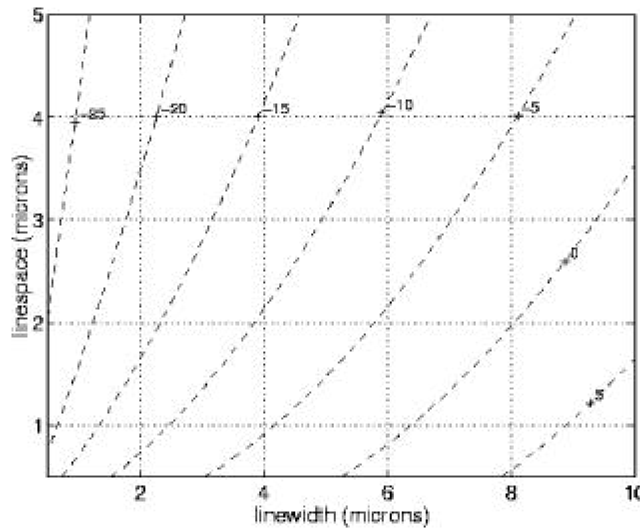
Design or Manufacturing Problem? Both!

CMP causes layout dependent dielectric variation which causes yield loss

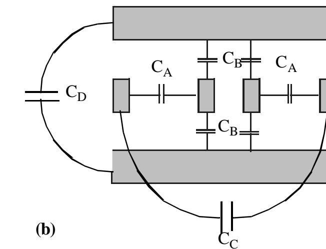


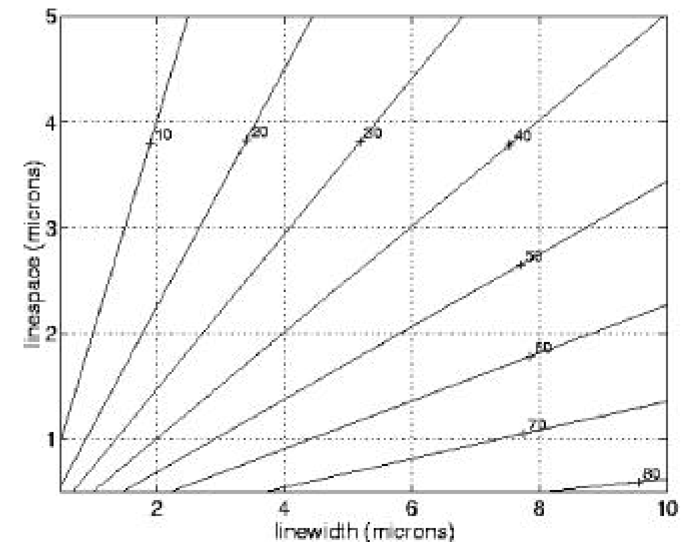
Dummy fill improves uniformity



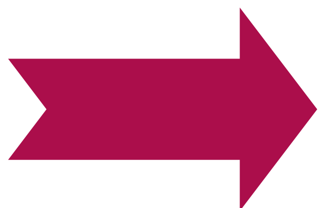


But capacitance can go up!



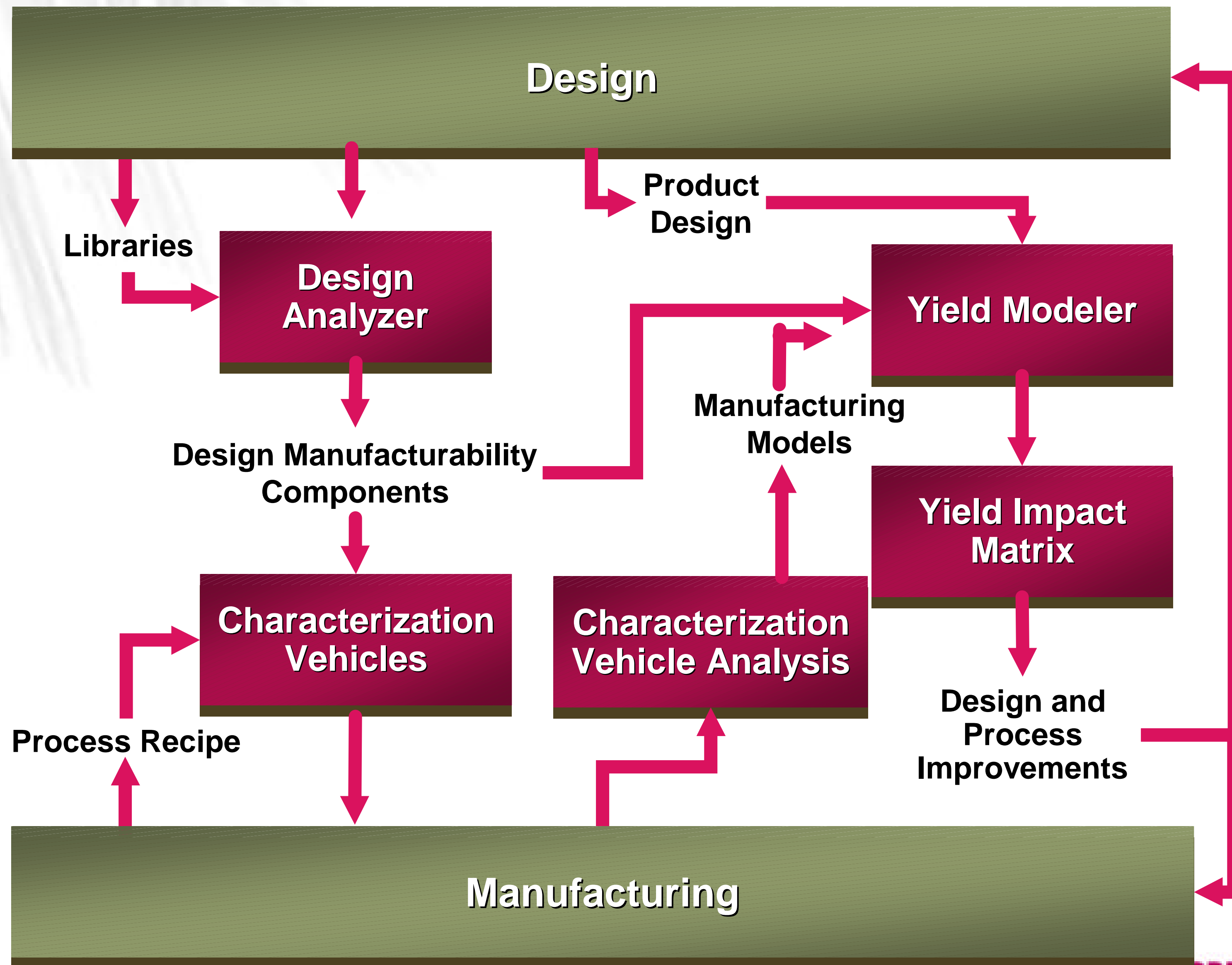


B. Stine et al, Transactions on Electron Devices, Vol 45 No. 3



Optimal solution depends on both design and process considerations

Simulating Design - Manufacturing Integration



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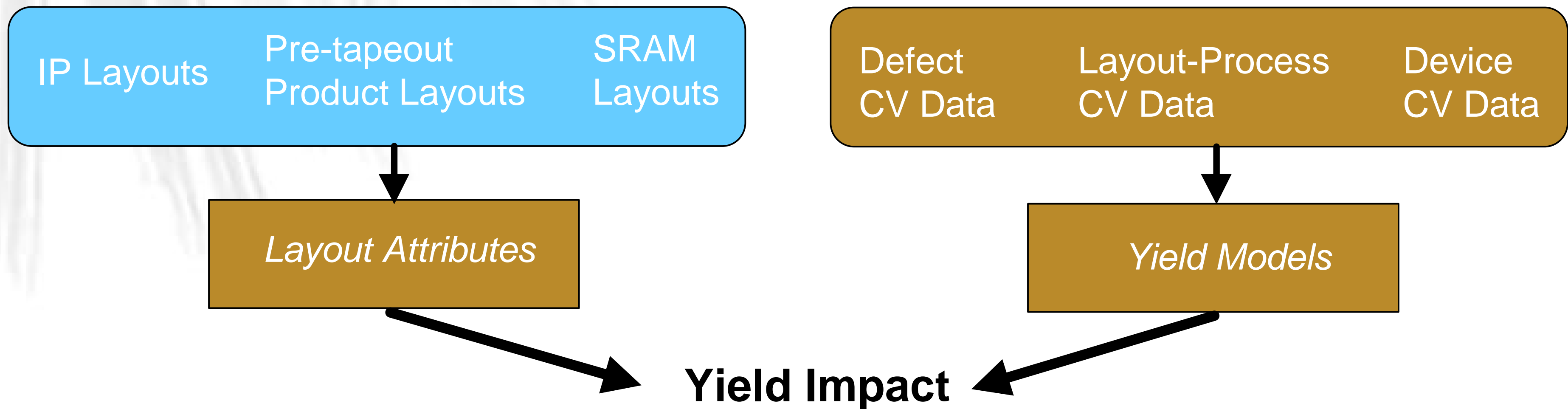
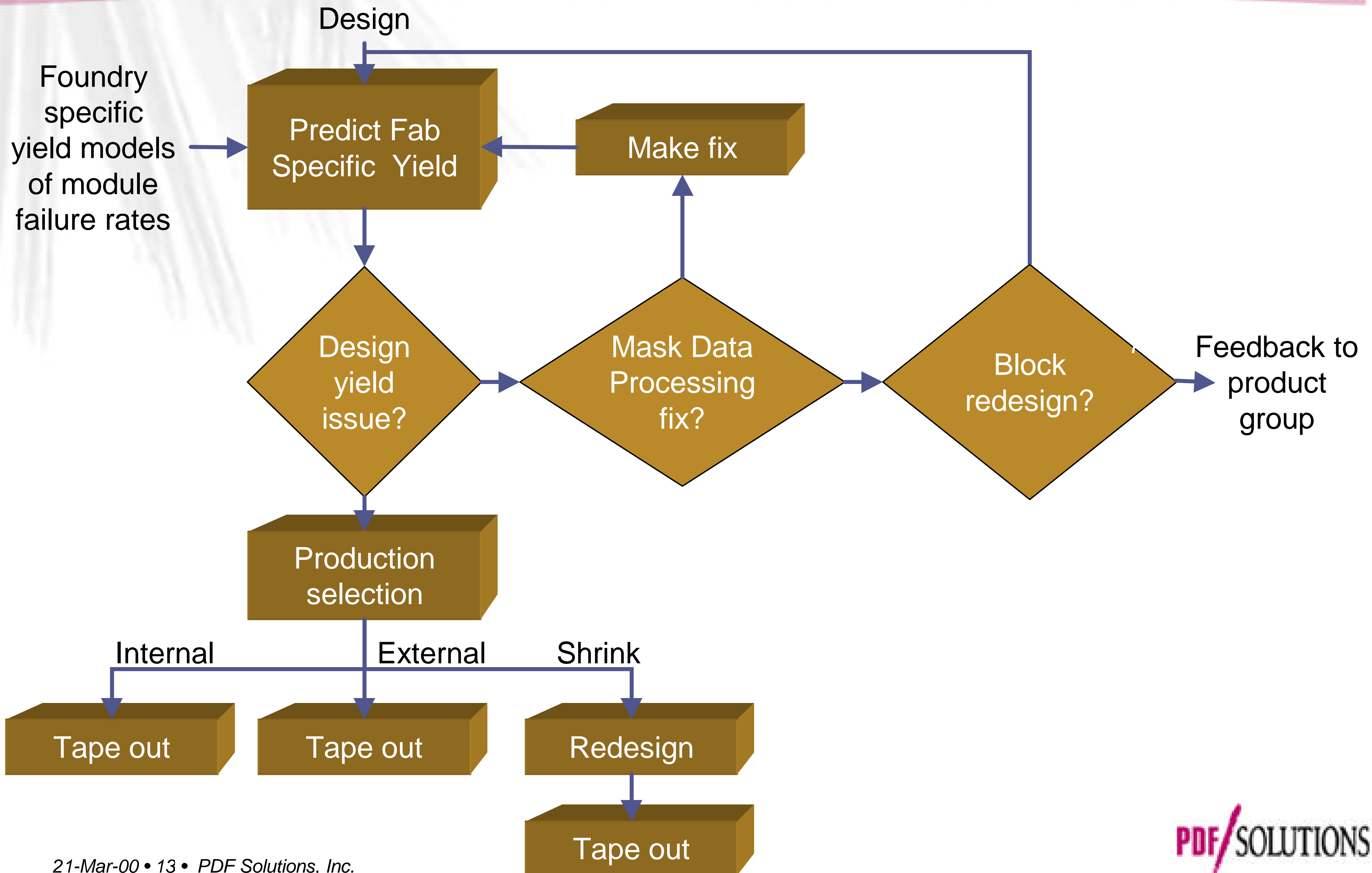
The Yield Impact Matrix



Yield Impact Matrix		Defectivity	Design Dependent	Overall
Product A	Chip	85.7%	58.0%	**49.8%**
	Block A	95.0%	93.0%	88.4%
	Block B	95.0%	**65.0%**	61.8%
	Virgin Cache	80.0%	80.0%	64.0%
	Cache w/ Repair	95.0%	96.0%	91.2%

Using Simulated Integration Results to Make Production Decisions



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Example 1: Via Short Flow CV Example

Floorplan

<table>
<tr><td rowspan="5">Long Runners</td><td colspan="6">Long Runners</td><td rowspan="5">Long Runners</td></tr>
<tr><td colspan="6">Via1 Loading</td></tr>
<tr><td colspan="2">Via2 Loading</td><td colspan="2">Contact Loading</td><td colspan="2">Isolated Vias</td></tr>
<tr><td colspan="3">Via2 Misalignment</td><td colspan="3">Contact Misalignment</td></tr>
<tr><td colspan="4">Redundancy</td><td colspan="2">Size</td></tr>
</table>

- Via1/Via2/Contact Loading:
  Compute yield impact of density.
- Via2/Contact Misalignment:
  Compute yield impact of misalignment of via to underlying layers.
- Redundancy:
  Compare fault rates of single via chains to redundant via chains.
- Size:
  Compute yield impact of via size.
  Check process margin.
- Long Runners:
  Compute yield impact of long metal runs in via chain.

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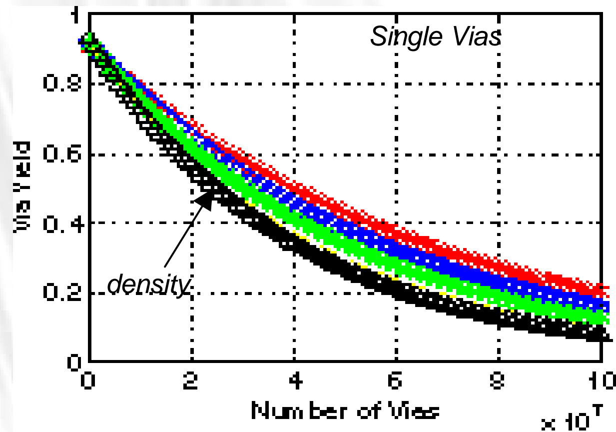
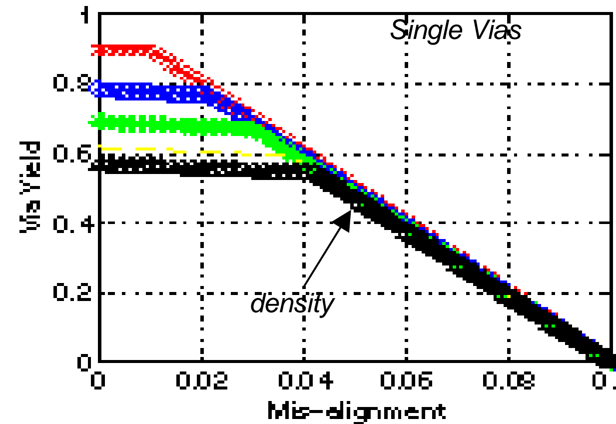
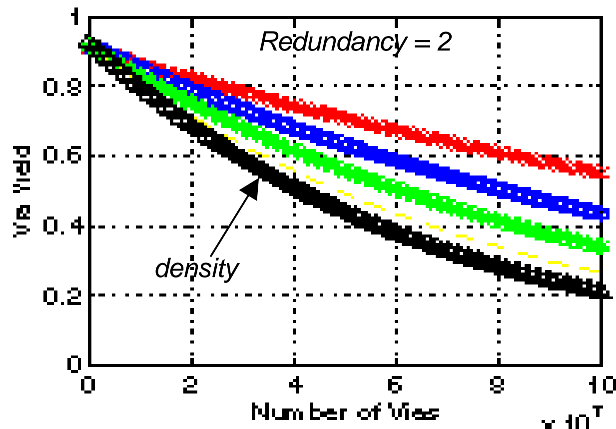
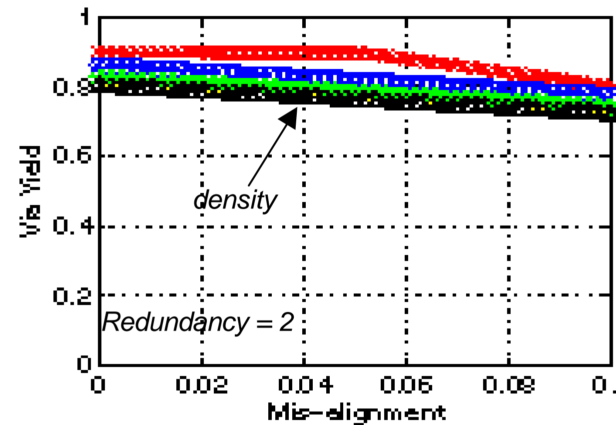
Example 1: Yield Modeling

Process Specific Via Yield Model









Via Yield Model:

$Y_{via(non\text{-}redundant)}$ = f_1(misalignment, density, N)

$Y_{via\text{-}redundant)}$ = f_2(misalignment, density, N)

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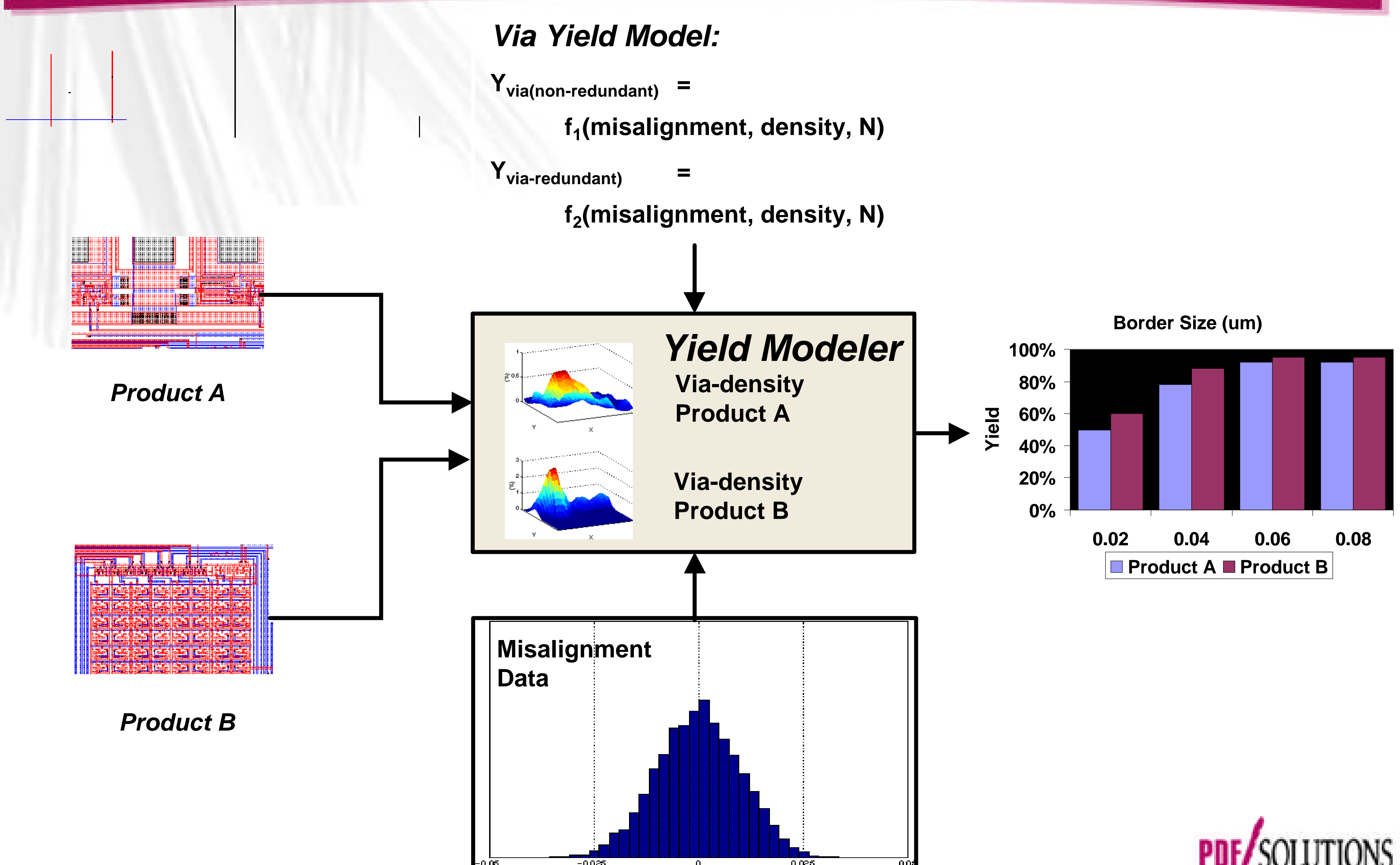
Example 1: Design Yield Entitlement
Product Specific Via Yield Prediction



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Example 2: Optimizing Fill For Performance and Yield

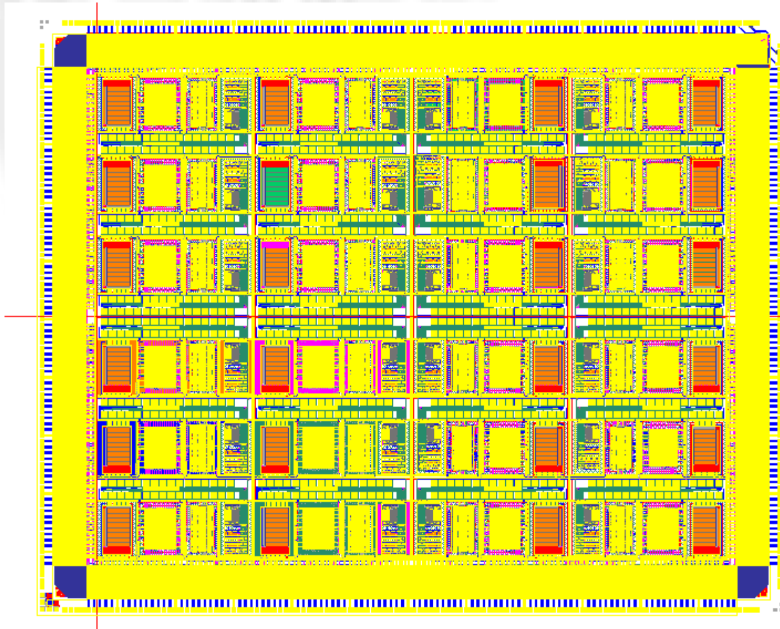
Questions about dummy fill algorithm:

- Which layers?
- What pattern?
- Should you exclude sections of the design layout?

Approach

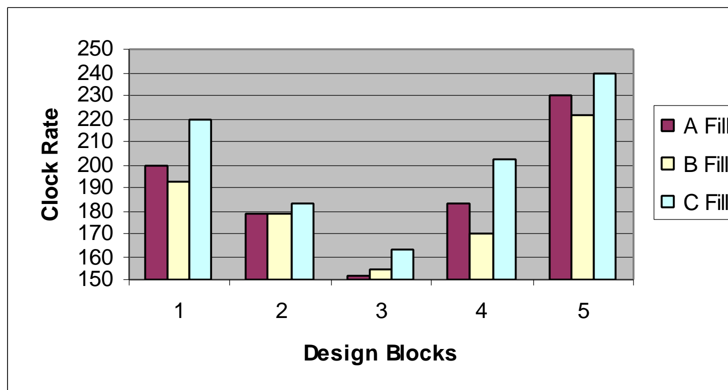
- Build vehicle to characterize performance/yield dependencies on layout choice
- Build yield models
- Optimize dummy fill for product chips

Example 2: Optimizing Fill for Yield and Performance



30 Identical circuits

- **Each contains: SRAM, gate dependent and interconnect dominated logic circuits, and analog blocks**
- **Each variant is a DOE element exploring dummy fill, meta/poly OPC, via sizing options**



Some fill patterns have positive impact on yield and performance for some design blocks

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Concluding Remarks

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- Systematic yield loss component is significant, growing, and recoverable
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