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# Design Success: Foundry Perspective


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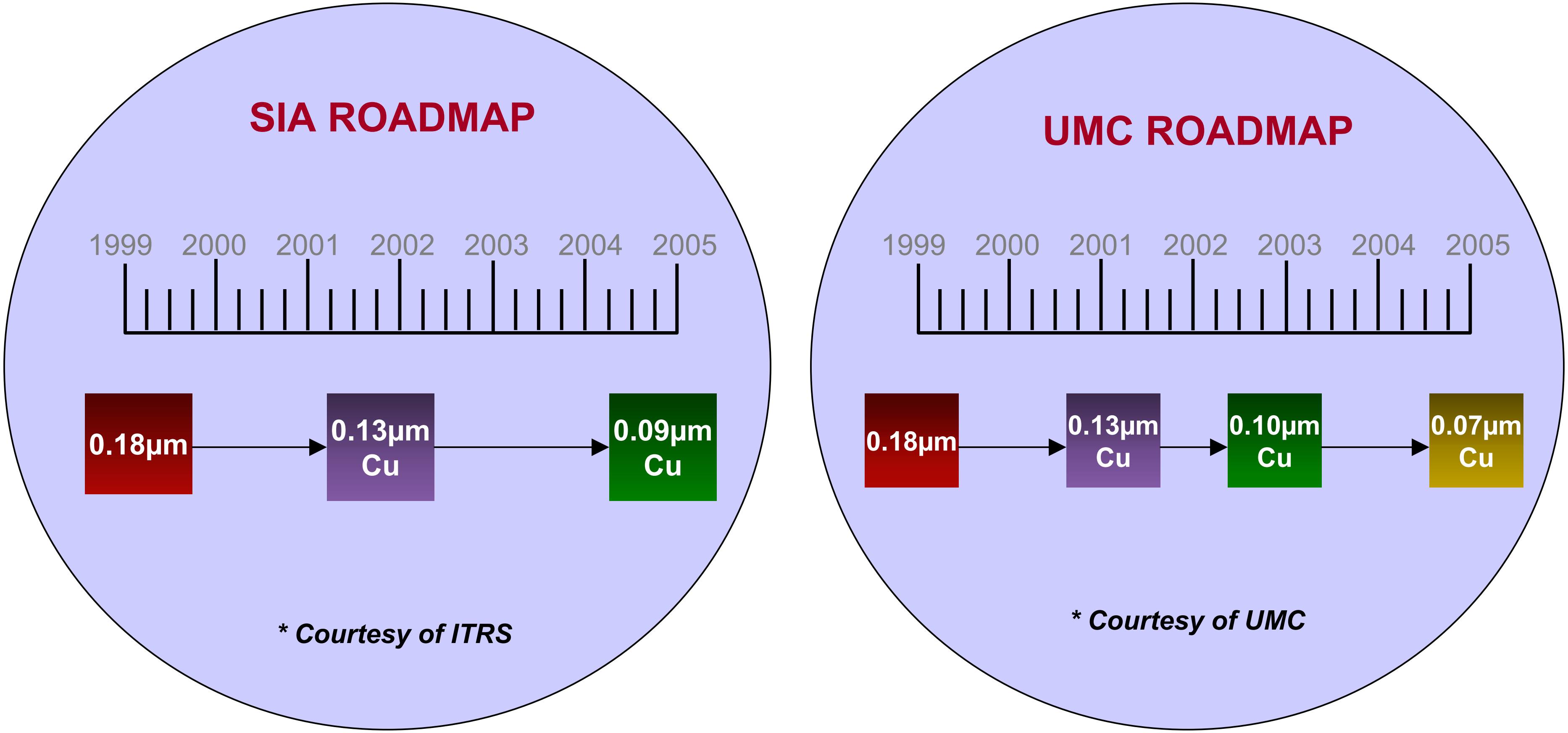
*Previous President of UMC-USA*

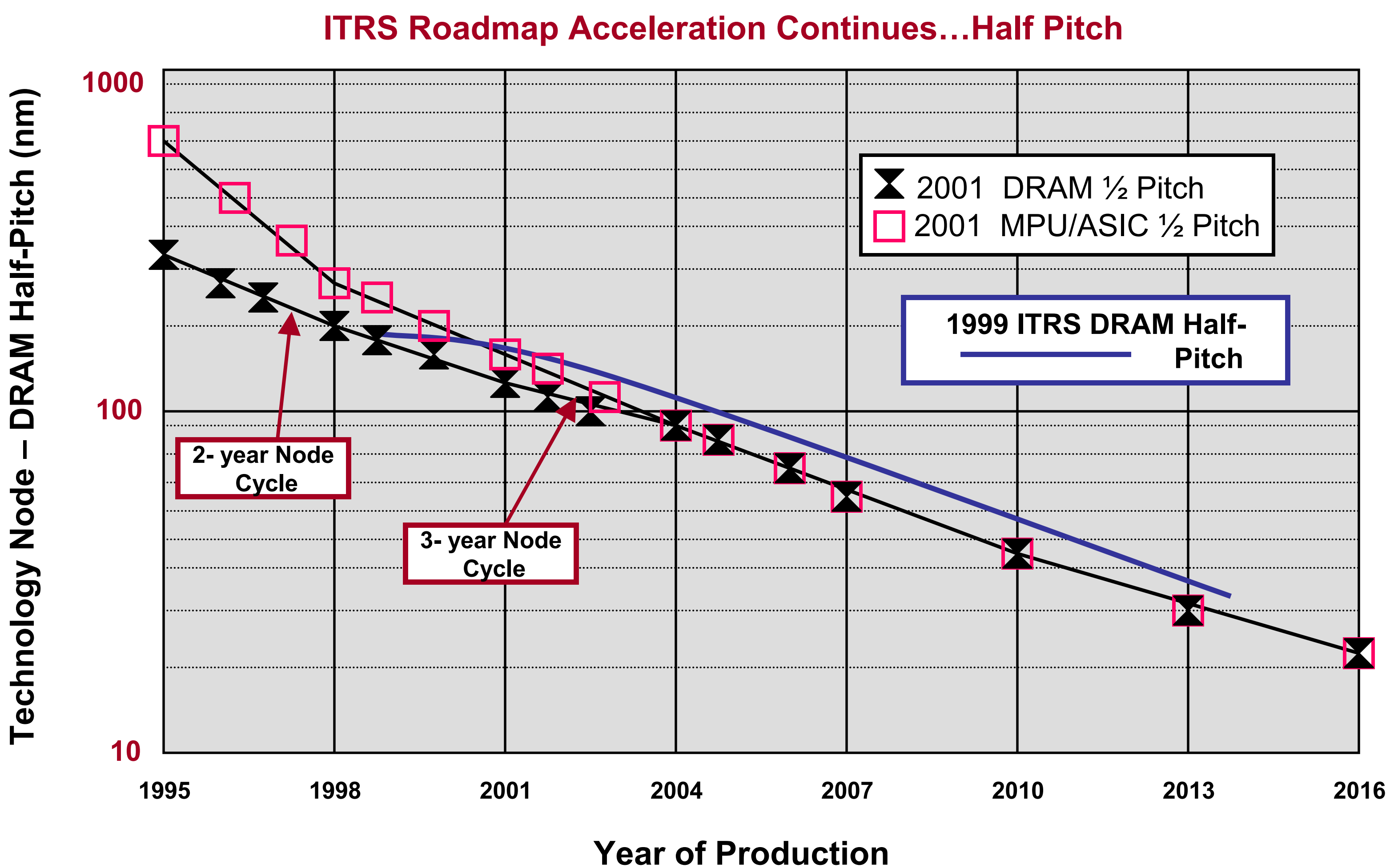
***"It is not the strongest of the species to survive,***
***nor the most intelligent,***
***but rather the one most responsive to change."***

*Charles Darwin, "On the Origin of the Species by Natural Selection", 1859*

# Technology is Rapidly Advancing



# Technology is Rapidly Accelerating




* Courtesy of ITRS

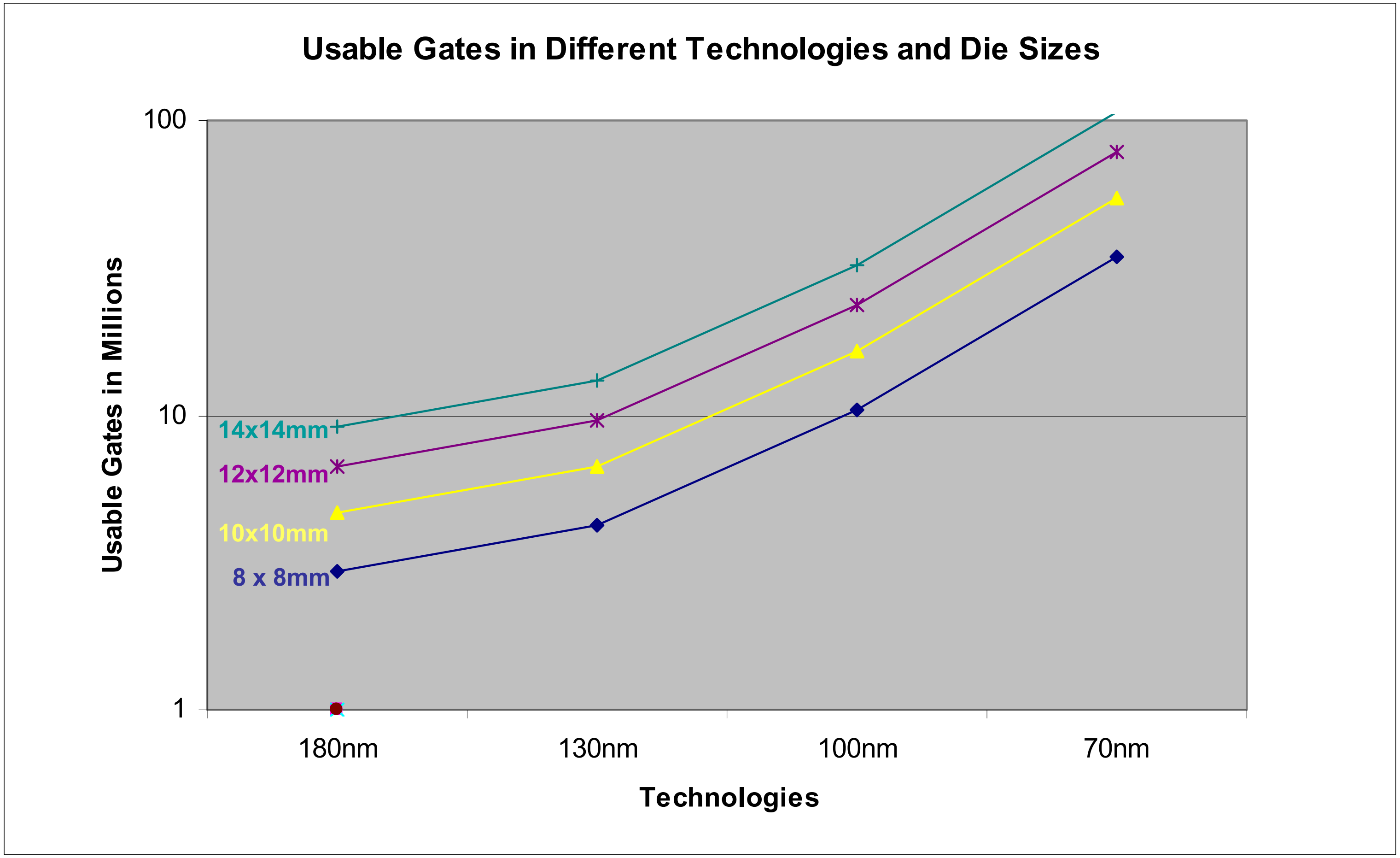
## Disintegration Allows More Advanced Resources But…

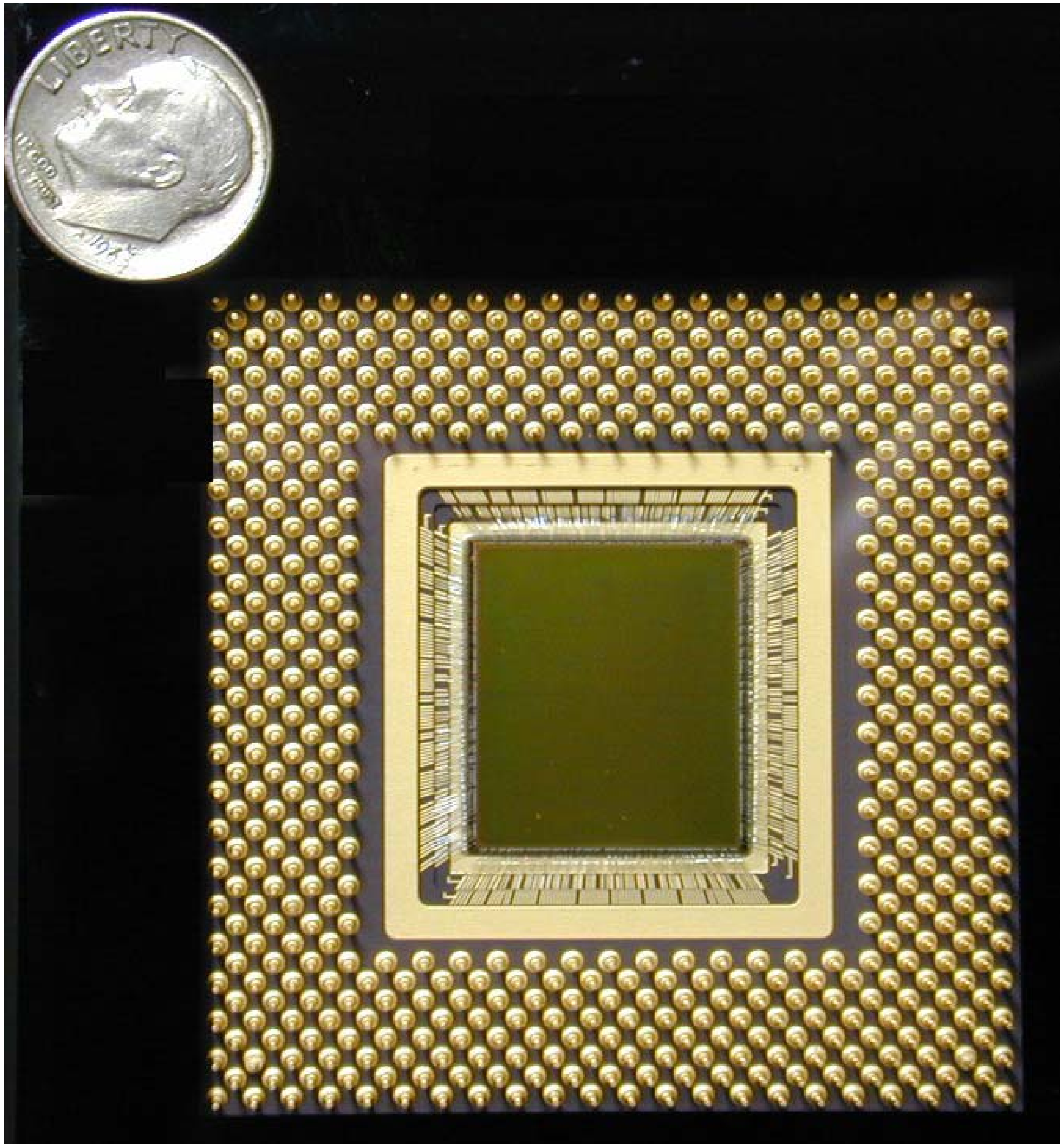
① System Specification → ② IC Design → ③ IP Sourcing → ④ Wafer Fabrication → ⑤ Assembly and Test

## …Coordination is Critical

**Example**

# The Big Hard Chips



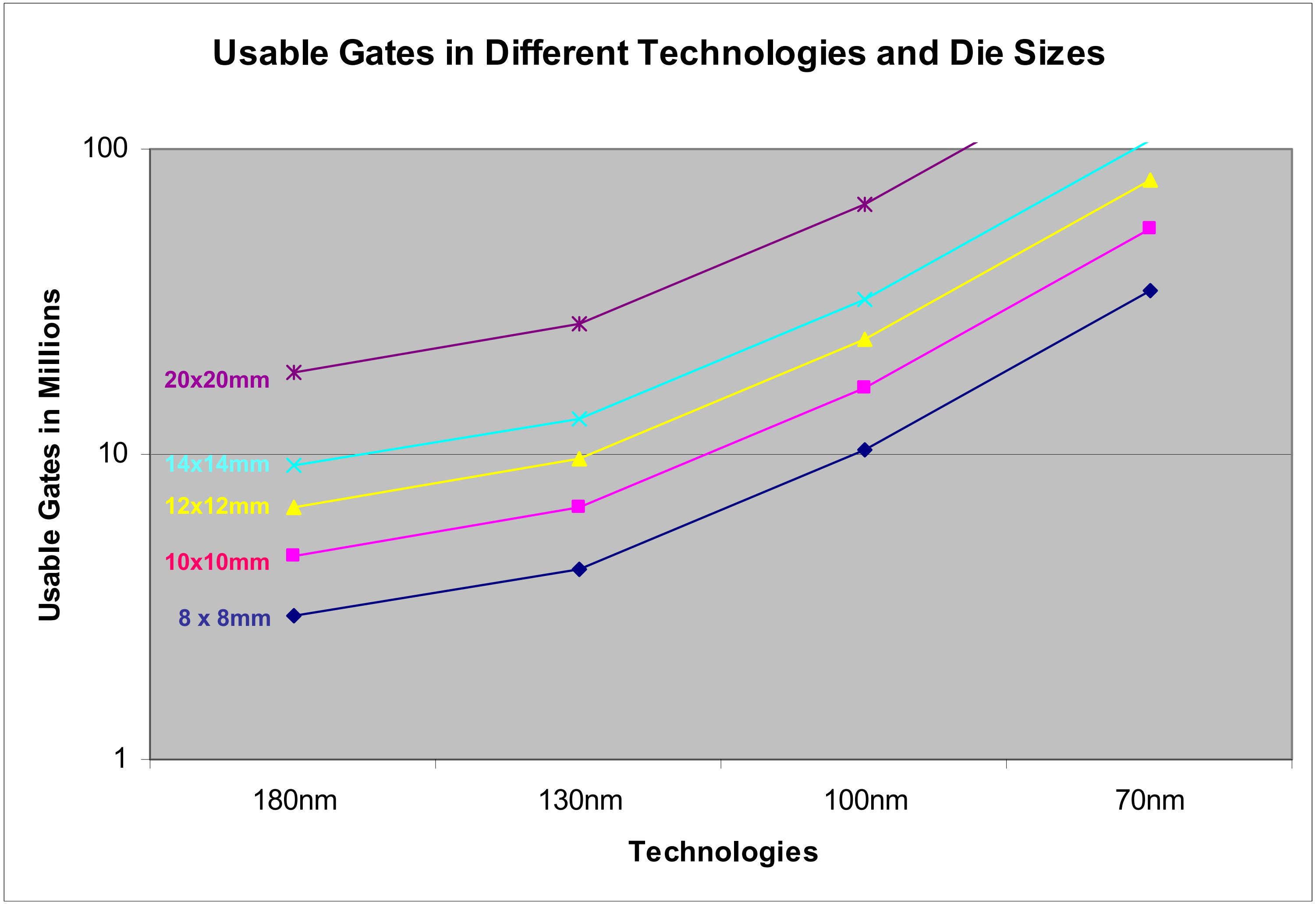



## Big Chips are Real

**20 x 20 mm**

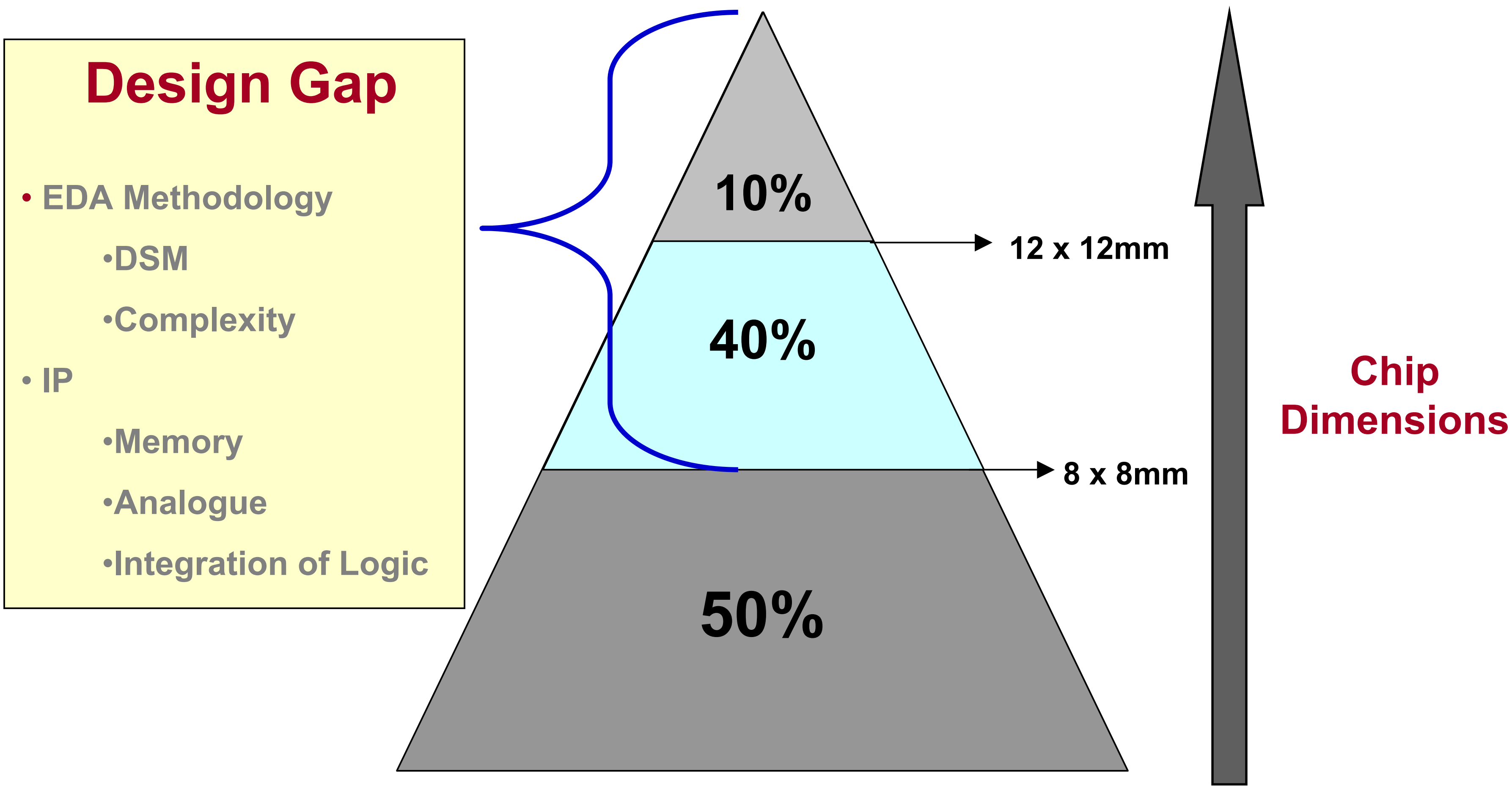
***** Chip courtesy of Xilinx***

# The Big Hard Chip



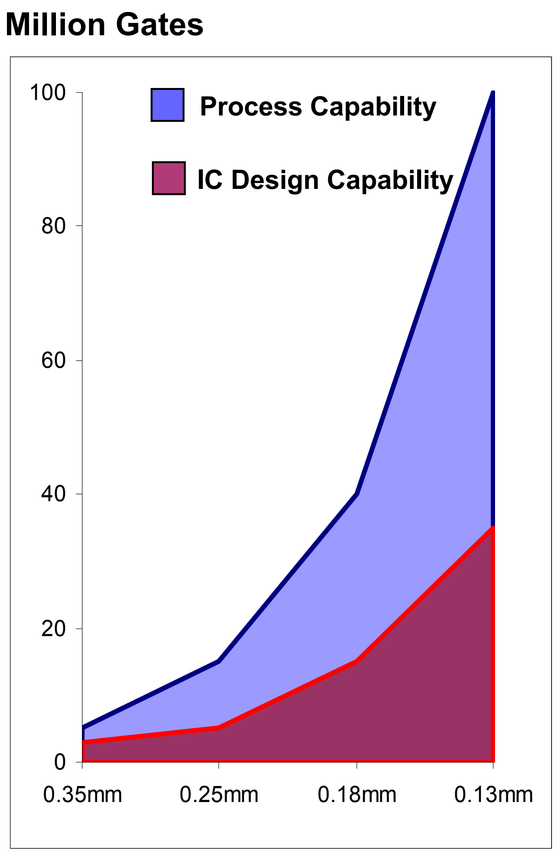

* From ITRS/ AmmoCore Estimates

# Chip Size Estimates




% = Silicon consumed by various chip sizes

# Rapidly Expanding Design Gap



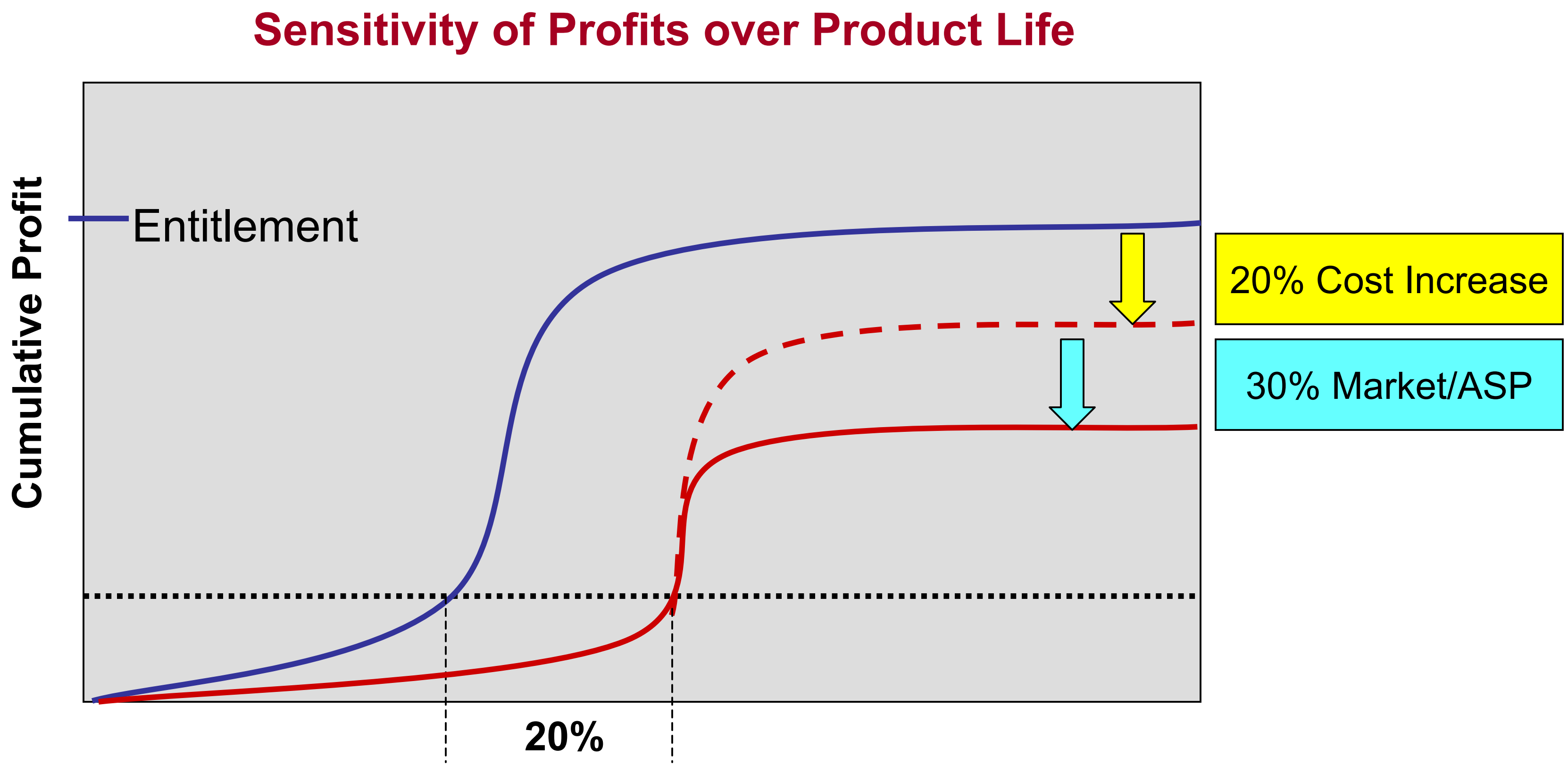

| | 1997 | 1999 | 2001 | 2003 |
|---|---|---|---|---|
| IC Physical Size ($cm^2$) | 4.8 | 8.0 | 8.5 | 9.0 |
| Area after Mem ($cm^2$) | 2.9 | 4.8 | 5.1 | 5.4 |
| Auto-layout Tx (M) | 23.0 | 67.2 | 81.6 | 129.6 |
| Equivalent Gates (M) | 5.8 | 16.8 | 20.4 | 32.4 |

Sources: SIA, Dataquest

- New systems will need to take advantage of advances in IC manufacturing technology
- Finer process geometries provide ability to manufacture >30M gates on a single die
- Ability to implement large Systems in silicon will decline due to physical design limitations

***Physical design methodologies will not scale***

# Design Gap Creates Opportunity…
# If Early Adoption is Successful

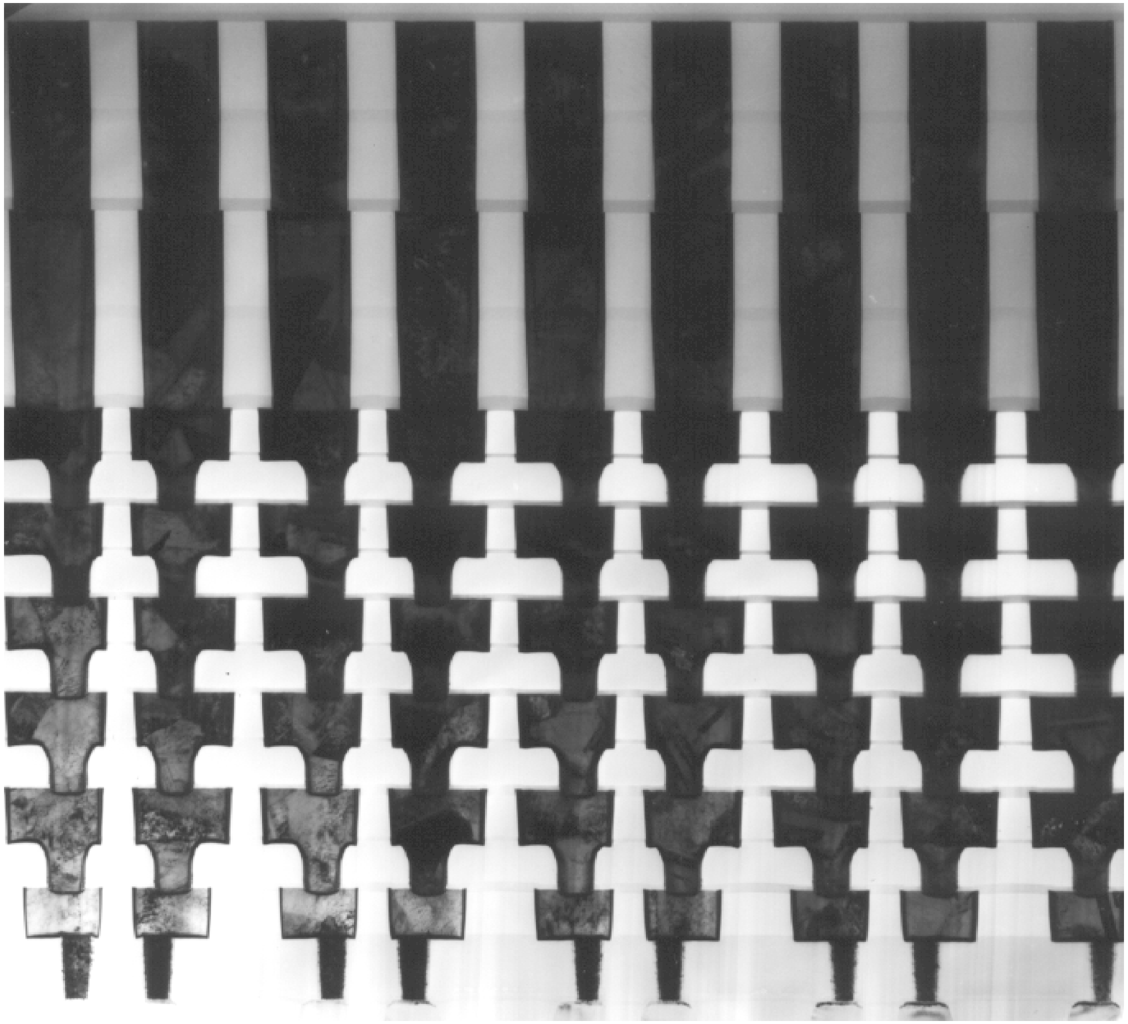



* From Accelerating Innovation

## Challenges of Big Multi-Million Gate Chips

- Deep Submicron Effects Are Critical
- Physical Methodologies Do Not Scale
- Engineering Team Coordination Raises Overhead Factors
- IP Integration

# DSM Challenges



**Metal Modeling**

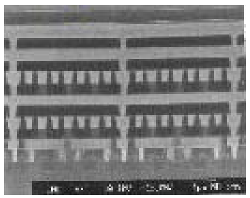
- Coupling
- Antenna
- Electro Migration

* Courtesy of UMC

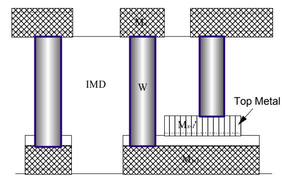
# Modularized Technology

**Passivation, Fuse, RDL**

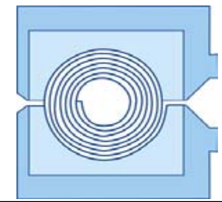
**Multi-layer Interconnect**



**MIM Capacitor**

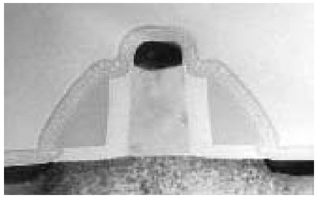



**RF Inductor**

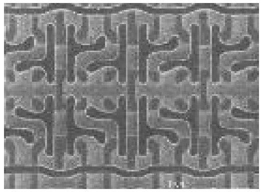


**Devices**
**Core**
**I/O**
**Analog**
**Low Vt**
**Zero Vt**
**Resistor**
**Varactor**

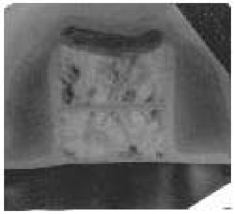
**HS, LL, MPU, LP**



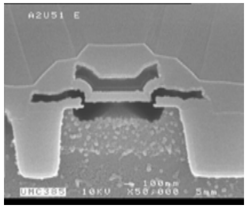
**e-SRAM**



**e-FLASH**

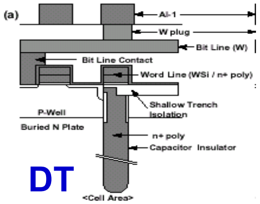


**SiGe-BiCMOS**



**Twin-well / Triple-well / well isolation**

**e-DRAM Trench cell**




**DT**

**Starting Material**

**Bulk, EPI, SOI, etc.**

* Courtesy of UMC

# Platform Technology

**Logic Transistors**

- MPU
- High Speed (HS)
- Low Leakage (LL)
- Very Low Leakage (VLL)

**Mixed Signal/RF CMOS**

- -Zero Vt, Low Vt, 2.5V I/O, 3.3V I/O transistors
- -Spiral Cu Inductors, Metal-I-Metal Caps, Poly Resistor

**e-Memories**

- e-SRAM: $2.28um^2$ bit cell
- e-DRAM: $0.31um^2$ cell

**0.13um SOC Platform**

- Low-k Dielectrics (k =2.7)
- 8 Layers Cu Interconnect

**Libraries**

- Memory Compilers
- RF Design Kits

**Gold IP Catalog**

- ARM, DAC's, ADC's, Advanced I/O's

**Silicon Shuttle**

- 0.13um Prototyping

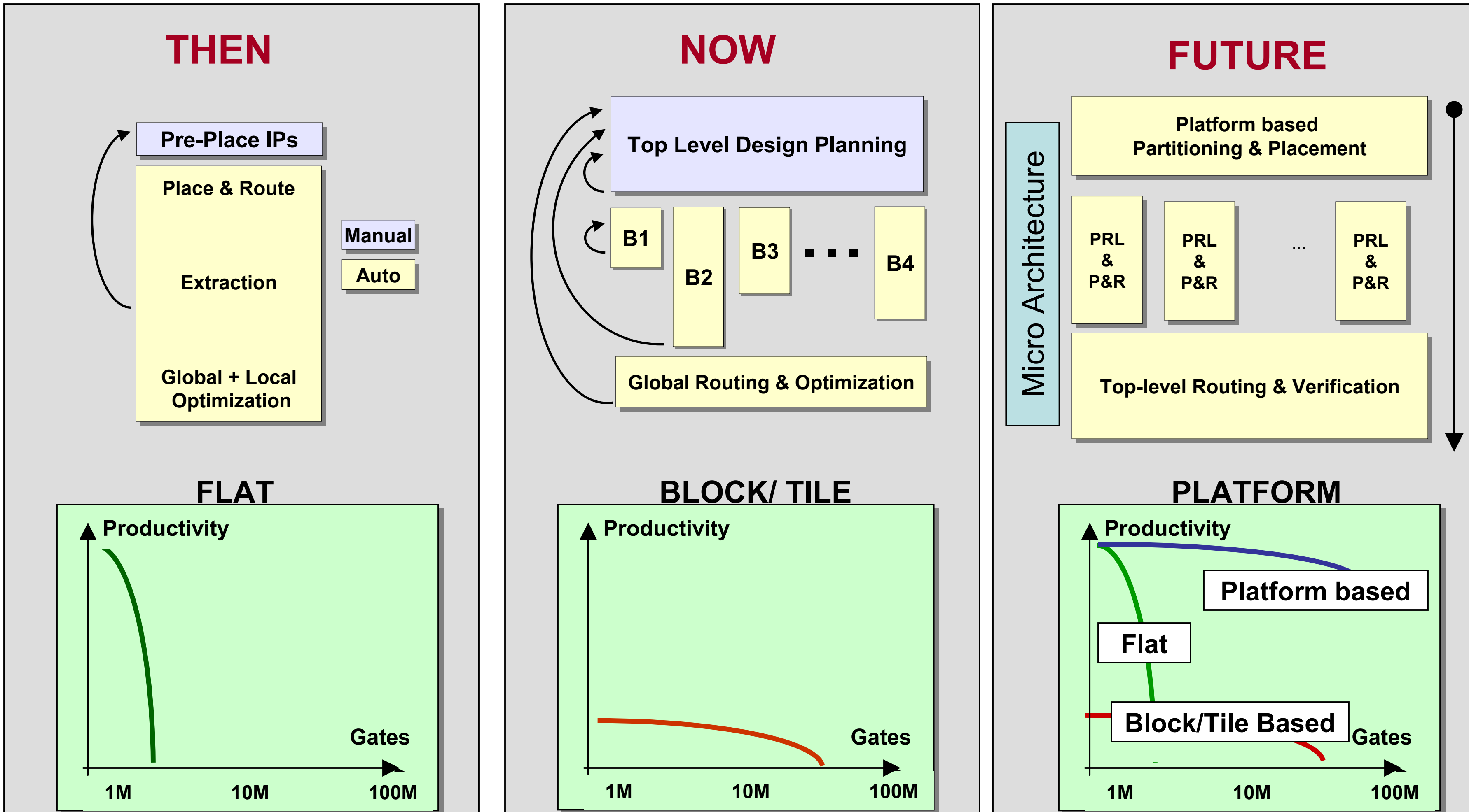
**EDA Partners**

- Technology Files: DRC, LVS, RC Extraction

=Technology Features

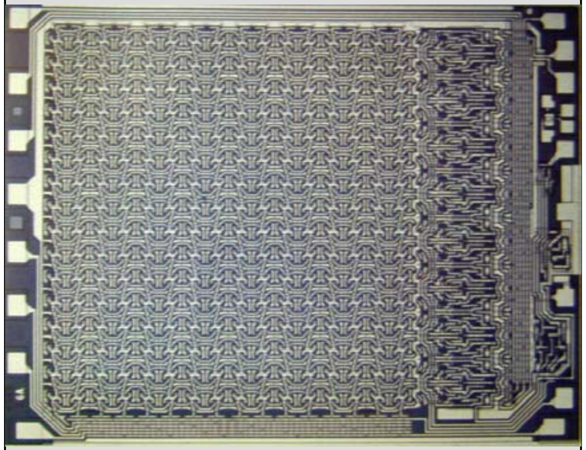
= Design Support Features

# EDA: Challenges of Big Chips
## (multi-million gates > 10M)



# SRAM: Challenges

## THEN

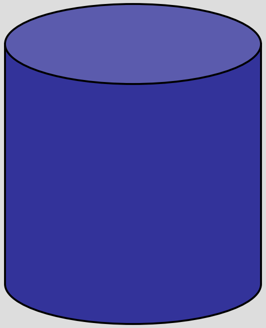


**First 256 Bit SRAM**

- Handcrafted
- Fixed Size
- Technology Bound
- Extremely Optimized

* Courtesy of Fairchild, circa 1970

## NOW



**Compilation**

- Auto-Compilation
- Various Sizes (smaller)
- Technology Sets
- Non-Optimized

(limited range, cells, footprint)

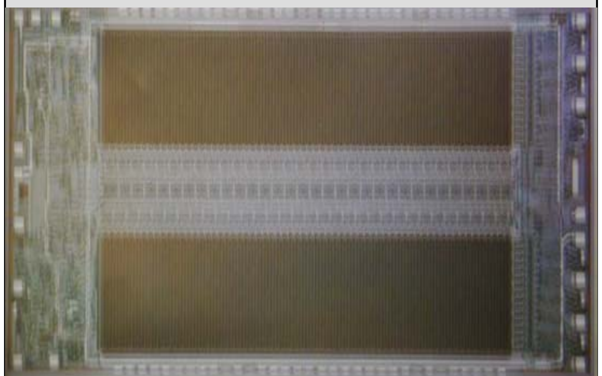
## FUTURE

**SRAM Future**

- Large Sizes
  - Redundancy
  - 1T, 2T Cells
  - MRAM Cells
- Bit Density Approach 50% DRAM
- ASIC Process Compatible
- Tolerable Process Cost

# DRAM: Challenges

## THEN

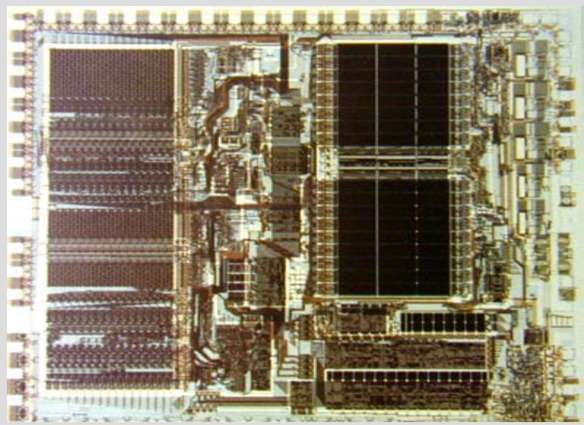


**Most Successful 16K DRAM**

- Handcrafted
- Fixed Size
- Technology Bound
- Extremely Optimized

* Courtesy of Mostek, circa 1976

## NOW



**EDRAM**

- Place Macro
- Limited Implementation
- 8M – 256 Mbit
- Process Complexity Adder
- Non-evolved IP

## FUTURE

**EDRAM Future**

- Technology lags ASICS
- Process Cost Adder
- Package Solution Competition

# Summary

- Design must be able to coordinate multiple IP sets
  - “ Trust but Verify ”
- New EDA tools/ methodologies required to cope w/ large densities and DSM
  - “ Target Needs ”
- Adaption opportunities are accelerating
  - “ Proverbial Inflection Point ”