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WaferNEWS

THE SEMICONDUCTOR EQUIPMENT AND MATERIALS WEEKLY BRIEFING

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In the spotlight

Percentage change in AMD stock price, which was $6.38 on April 1, 2003, compared to $14.75 a year ago. See related story, page 3.

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Inside:

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SEMICON Europa opens with shared booths, hopeful signs of a turnaround

A more compact SEMICON Europa opened in Munich on April 1 as smaller booths, shared booths, and lighter traffic were the results of a third year of a deep downturn in the industry.

"Wait until next year," summed up the message from SEMI CEO Stan Myers, who forecasts double-digit growth for 2004 and 2005, but modest growth for the first half of 2003, at least. Rising capacity utilization, especially for advanced devices, and low inventory levels indicate that the market is poised for growth, Myers pointed out, but geo-political uncertainty is delaying spending.

"Don't expect a large surge in bookings in the short run," he said. "We're still bouncing on the bottom."

The global equipment market has dropped almost 60% since 2000, to the lowest level since 1994, he added.

In 2000, chipmakers overbooked $6 billion in equipment, and it's not clear if all of this is off the books yet. Analysts disagree about whether we are still working down this overhang, Myers said, or if the industry is now under-spending, which would suggest a strong turnaround when capacity utilization rises.

At Europa, the exhibit area fell about 20% for the second year in a row at the Munich Trade Fair Center, but there were 956 primary- plus co-exhibitors, up from 785 last year, as many more companies share booth space, according to Walter Roessger, president, SEMI Europe. New this year was a MEMS platform, for companies specializing

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ISQED explores nanometer design challenges

More on Moore — Part 1

The semiconductor industry has been concerned about growing gaps between design and wafer process engineers, and between designers and maskmakers. This concern was demonstrated by microlithographers attending recent SPIE and BACUS conferences; the topic also was explored at IEEE's 4th International Symposium on Quality Electronic Design (ISQED), held in San Jose on March 24 – 26.

Speaking at the first plenary session, Robert Payne, senior VP/GM, advanced systems technology at Philips Semiconductors, posed this question: What happens to the industry if Moore's Law continues to be followed but design creativity does not keep up? "Can the semiconductor industry become a victim of its own silicon efficiency?" asked Payne. His concern is that it could be possible for factories and revenues to keep getting smaller and smaller, even as die get smaller and smaller and prices go lower and lower.

And what if Moore's Law died? Payne says that the compound annual growth of the industry would continue but the productivity slope would change, doubling every two to three years instead of every 18 months. He doesn't believe that physical limits, economic limits or EDA tools would be to blame. He also doesn't see application demand as the issue — there's plenty of unfulfilled demand in areas of home and office needs as well as demand for wireless and other mobile applications.

Payne believes the real problems are a failure to invent simplifying methods and architecture. He suggests that the industry could benefit by returning to the roots of another scientific challenge: the Apollo space pro-

See **ISQED** *continued on page 10*

Briefs...

Catalyst names board member—*Catalyst Semiconductor, Sunnyvale, CA, a developer of programmable products, said that Garrett Garrettson has been appointed to the company's board of directors and will serve on the board's audit and compensation committees. He succeeds Cynthia Butitta who has resigned from the board.*

Electroglas appoints Saliba to board—*Electroglas Inc., San Jose, CA, a supplier of process management tools, said that Edward Saliba has joined the company's board of directors. Saliba, a former executive at Sun Microsystems, has replaced Roger Emerick, who is set to retire.*

Entegris wins 300mm orders—*Entegris Inc., Chaska, MN, has secured orders for its horizontal wafer shipper and single film frame shipper from nine 300mm customers in Asia, Europe, and the US within the first six months of FY03.*

Sony closes plant—*Sony Corp., Tokyo, Japan, plans to close its analog chip factory in San Antonio, TX, by the end of September. The factory has a wafer preprocessing line and manufactures bipolar chips for assembly into audio and telecommunications equipment. Sony has decided to close the factory because demand for analog chips for audio equipment remains sluggish, reported the* Nihon Keizai Shimbun. *All 600 workers will be let go. Some of the equipment will be transferred to a Sony factory in Kagoshima Prefecture.*

ISQED *continued from page 1*

gram. In those days, engineers in the space program performed most calculations using slide rules, raising approximation to the level of a science by heavy use of simplifying assumptions with boundary conditions — something the post-Apollo generation of engineers hasn't needed because of the tremendous computing power available to solve problems. "We need to learn the lesson," states Payne. "We can't solve the problem by whipping the computer harder." He goes on to note that more than 30 years of cycle-after-cycle refinements — faster computers, better CAD, more complex ICs — may be coming to an end.

Payne promulgates a design for low power philosophy as a way to gain performance for free, as well as dramatically change system level design methods and architecture to close the design productivity gap and streamline the design process.

To illustrate the difference between a performance-focused approach and a low-power approach to design, Payne notes that a 3GHz Pentium 4 runs at >75W with only ~10% of the chip running at 3GHz. If the entire chip were run at 3GHz, the chip would consume >500W/cm^2. Extrapolating the trend to future technology would result in power density approaching that of a nuclear reactor (~1kW/cm^2). Conversely, the practical limits on consumer electronics and mobile electronics, he says, are 2-4W and 0.2-0.4W, respectively.

Payne described various design techniques with respect to computational unit optimization of configurable DSPs (called AXUs [application xceleration units] or power plugs) and control processor efficiency that result in more efficient power consumption and/or better performance. As an example, power plugs can provide >100x leverage that can be spent in one of three ways: 1) as a 100x power advantage, 2) as a 10x power advantage and a 10x throughput advantage, or as 3) a 100x throughput advantage.

It is no surprise that Intel Fellow and director of the circuit research lab at the company Shekhar Borkar does not see Moore's Law dying anytime soon. By continuing to double transistor density, improve transistor performance, and lower power dissipation with each generation, Borkar says that the industry can continue Moore's Law for at least 20 more years. Admitting that these things get harder to do with each generation and as the cost of fabs go up, he emphasizes that the cost of a transistor declines. "This is the reason why we can now afford a 3GHz Pentium 4 at home, which costs less than $2,000, and is more powerful than the computers of the 1960s that cost hundreds of thousands of dollars," said Borkar.

The challenges that often are faced first by microprocessor designers sooner or later come home to roost for SoC and ASIC designers. Borkar discussed some of the techniques being used by Intel, such as low-power design techniques, improved design and power efficiency (e.g., multi-threading, chip level multi-processing, embedded special-function hardware) and valued performance by increasing the integration of slower transistors that can perform such functions as sleep transistors, adaptive body biasing, and other methods to control leakage.

Borkar further pointed to the critical role that adaptive body biasing plays as a tactical solution to account for the variations in circuit performance that arise from variations within the die. Strategically, however, variation tolerance using statistical design methods is the way to go. "Within-die variations in supply voltage, threshold voltage and temperature result in a probability distribution function for path delays," said Borkar. "The result is a much broader probability distribution function for device frequency as a function of leakage power. When this distribution function is taken into account, the fabricated chip does not have targeted performance or power; rather, it has a certain probability of hitting the targets ... some chips will be better, and some worse." According to Borkar, this is as major a paradigm shift in design, similar to the shift from Newtonian mechanics to quantum mechanics.

Next week's issue of *WaferNews* will include Part 2 of this series, which describes a contrarian viewpoint and proposed solutions that address the problem of the industry being a victim of pricing pressure on commodity products.—*D.V.*