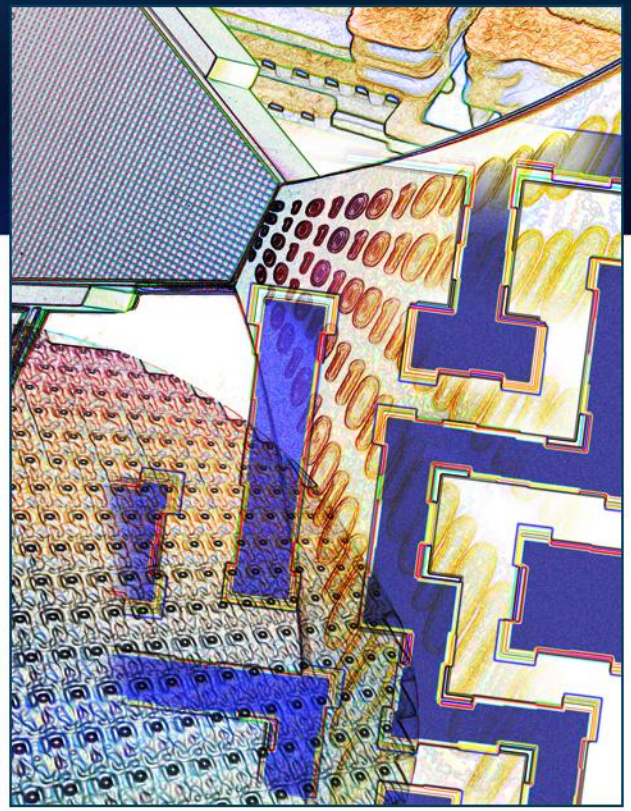
Trends In Analog Mixed Signal Design Tools



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March, 2013
ISQED2013

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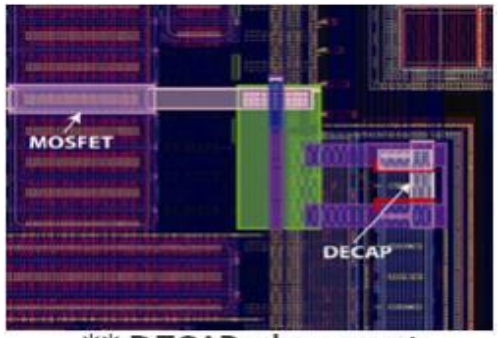
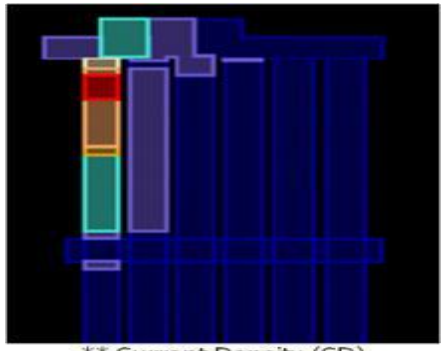
Analog Mixed Signal Designs Difficult and Becoming More Difficult

- There is increased analog content in today's SoCs and it is becoming more tightly integrated to the digital portion of the design



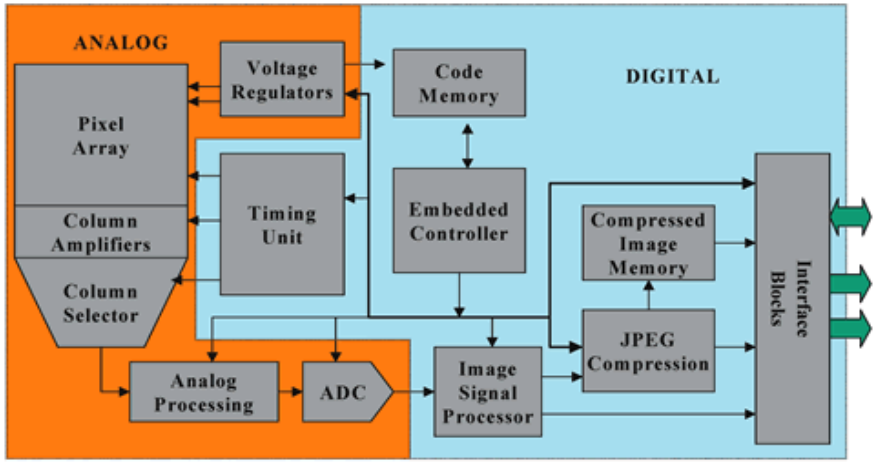
** DECAP placement


** Current Density (CD)

- Analog circuits are sensitive to layout, matching and proximity with demanding interface requirements – advanced process nodes amplify these difficulties

Analog and Digital No Longer Separate Worlds

- Traditionally, analog and digital design were separate, highly specialized disciplines with success determined by a clean handoff between the analog and digital teams

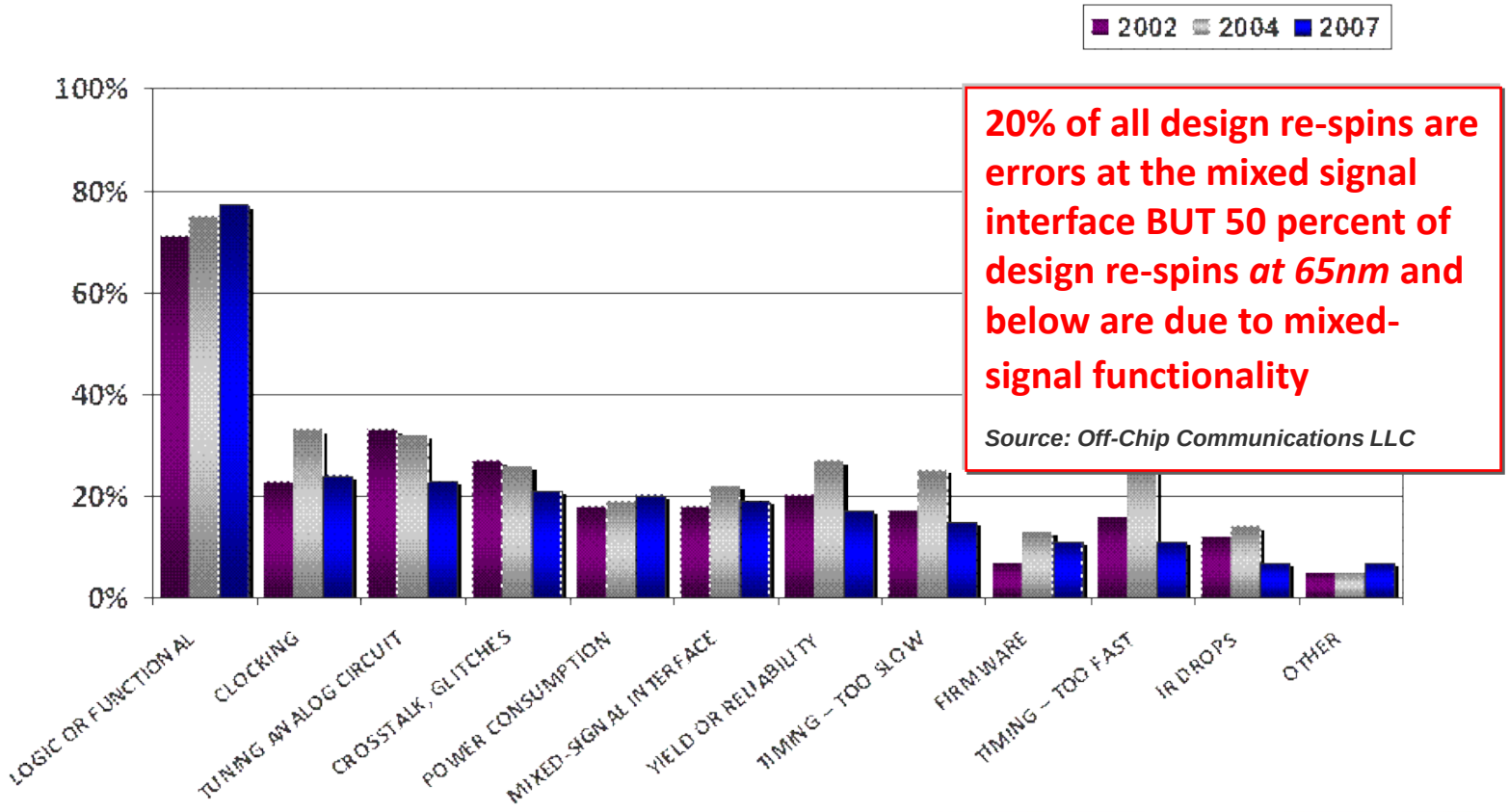


Camera chip CMOS imager architecture

- Today, a mixed-signal SoC integrates many mixed-signal blocks each containing a hierarchy of tightly integrated analog and digital circuits

Verification is Key

- Functionally verifying mixed-signal designs remains a tough challenge – simple simulation is no longer adequate

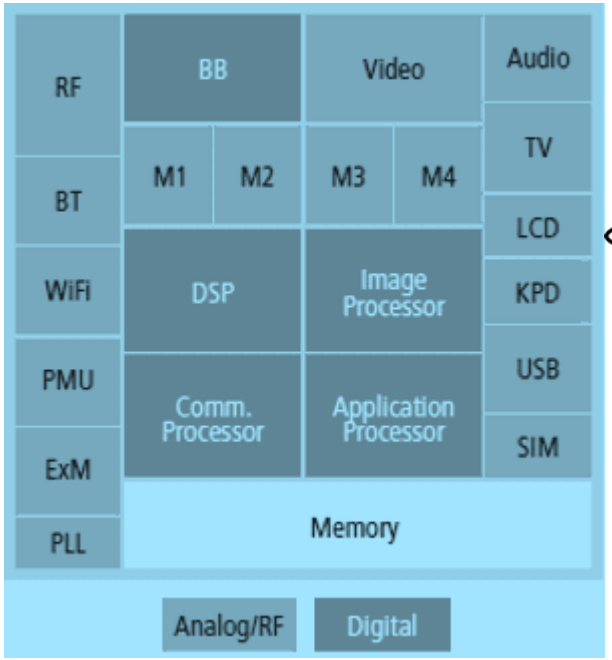


20% of all design re-spins are errors at the mixed signal interface BUT 50 percent of design re-spins *at 65nm* and below are due to mixed-signal functionality

Source: Off-Chip Communications LLC

Mixed-Signal Verification

- A new discipline called ”mixed-signal verification” is emerging that requires skills in mixed-mode simulation, behavioral model generation, and characterization and test bench development



What This Means For Methods and Tools

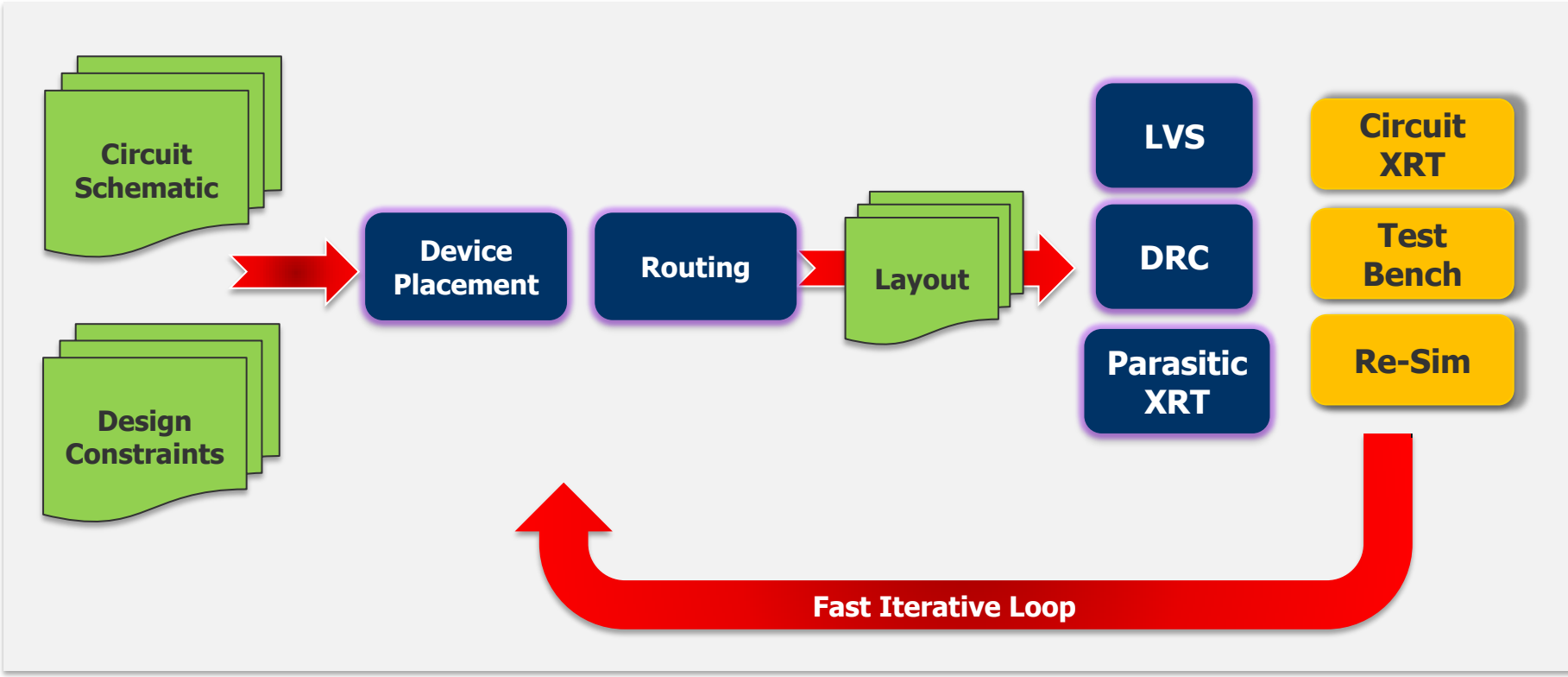
- Designers and verification engineers need high performance automation that gives them ***insight***:
- The following five areas are critical:
  - Achieving better verification of ***Analog and Digital Interfaces***
  - Creating a ***higher level of abstraction*** for analog and mixed-signal blocks
  - Verifying the increasing amount of ***digital logic in analog designs*** (e.g. low-power and digitally assisted)
  - ***Automating the manual custom design steps -*** especially placement and routing
  - Adopting ***circuit analytics*** that tell the designer something about ***why*** and ***where*** the circuit is failing to perform

Electrical and Physical No Longer Separate Worlds

- At 28nm, layout dependent effects such as stress and well proximity are significant
- A favorite quote from the CTO of a customer:
  - "The layout ***is*** the schematic"
- Need for robust Electrical and Physical Reconciliation (EPR) flow that fosters transparency between electrical intent and physical effects
- To do this, the EDA tool suppliers need to bring together technologies from many tools to serve in a new EPR cockpit

The EPR Cockpit

- Fast loop to enable iterative design and verification of all aspects of the design



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