WELCOME TO ISQED 2016

On behalf of the ISQED 2016 conference and technical committees, we are pleased to welcome you to the 17th International Symposium on Quality Electronic Design, ISQED 2016. The 17th International Symposium on Quality Electronic Design (ISQED 2016) is the premier interdisciplinary and multidisciplinary Electronic Design conference—bridges the gap among Electronic/Semiconductor ecosystem members providing electronic design tools, integrated circuit technologies, semiconductor technology, packaging, assembly & test to achieve design quality. ISQED is held with the technical sponsorship of IEEE CASS, IEEE EDS, and IEEE Reliability Society.

ISQED continues to provide and foster a unique opportunity to participants to interact and engage themselves in cutting edge tutorials, presentations, and panel and plenary sessions. We are happy to report a number of initiatives this year. The conference is organized around the theme 'IoT, Smart Sensors and Security'. And we have invited 2 distinguished keynote speakers from industry to focus on these topics.

Additionally four tutorials provide a holistic approach, from devices to circuits to systems, while covering in-depth studies and state-of-the-art in each of the topics impacting the quality of electronic design. The two-day technical program with three parallel sessions pack over 100 papers highlighting the latest trends in electronic circuit and system design & automation, test, verifications, and semiconductor technologies. ISQED 2016 also features a panel discussion titled "Hardware and System Security in IoT Era" on Tuesday March 15th.

All the technical presentations, plenary sessions, panel discussions, tutorials and related events will take place on March 15-16 at the Santa Clara Convention Center in Santa Clara, CA. Please refer to the conference booklet and/or ISQED website for program details. Welcome to another stellar year of ISQED! It couldn't have happened without your support and participation.

Brian Cline
TPC Co-Chair

Saibal Mukhopadhyay
TPC Co-Chair

Peter J. Wright
General Chair

Hai (Helen) Li
Tutorial Chair

Vinod Viswanath
Tutorial Co-Chair

Paul Wesling
Publication Chair

Gang Qu
Plenary Chair

Ali A. Iranmanesh
Founder & President

ISQED 2016 Best Paper Candidates

1A.1

Sizing-Priority Based Low-Power Embedded Memory for Mobile Video Applications

Seyed Alireza Pourbakhsh, Xiaowei Chen, Dongliang Chen, Xin Wang, Na Gong, Jinhui Wang

North Dakota State University

2A.2

Process Variation Aware Crosstalk Mitigation for DWDM based Photonic NoC Architectures

Sai Vineel Reddy Chittamuru, Ishan Thakkar, Sudeep Pasricha

Colorado State University

2C.1

Exploring the Use of Volatile STT-RAM for Energy Efficient Video Processing

Hengyu Zhao[1], Hongbin Sun[1], Qiang Yang[2], Tai Min[1], Nanning Zheng[1]

[1]Xi'an Jiaotong University, [2]Changhong Electric Co., Ltd

5A.1

Reliability and Energy-aware Cache Reconfiguration for Embedded Systems

Yuanwen Huang and Prabhat Mishra

University of Florida

5B.1

Digital IP Protection Using Threshold Voltage Control

Joseph Davis, Niranjan Kulkarni, Jinghua Yang, Aykut Dengi, Sarma Vrudhula

Arizona State University

5B.5

On Testing Physically Unclonable Functions for Uniqueness

Arunkumar Vijayakumar, Vinay Patil, Sandip Kundu

University of Massachusetts Amherst

6A.1

Impact of Interconnect Variability on Circuit Performance in Advanced Technology Nodes

Divya Madapusi Srinivas Prasad, Chenyun Pan, Azad Naeemi

Georgia Institute of Technology

6B.4

AFD-Based Method for Signal Line EM Reliability Evaluation

Zhong Guan, Malgorzata Marek-Sadowska

University of California, Santa Barbara

ISQED 2016 Best Papers

Best Papers

5A.1
Reliability and Energy-aware Cache Reconfiguration for Embedded Systems

Yuanwen Huang and Prabhat Mishra

University of Florida

5B.1
Digital IP Protection Using Threshold Voltage Control

Joseph Davis, Niranjan Kulkarni, Jinghua Yang, Aykut Dengi, Sarma Vrudhula

Arizona State University

* Authors of best papers are honored during the luncheon on Tuesday March 15

ISQED 2016 Organizing Committee

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Hangzhou Dianzi University

Taiwan Chair
Shih-Hsu Huang
Chung Yuan Christian
University

Brazil & South America Chair
Fabiano Passuelo Hessel
Pontificia Universidade Catolica do
Rio Grande do Sul, Brazil

TECHNICAL PROGRAM COMMITTEES

Brian Cline- ARM (Co-Chair)
Saibal Mukhopadhyay- *Georgia Institute of Technology* (Co-Chair)

Cognitive Computing in Hardware (CCH)

Yiran Chen, University of Pittsburgh (Chair)
Vikas Chandra, ARM (Co-Chair)

Committee Members:
Yu Cao - Arizona State University
Abishai Daniel - Intel
Miao Hu - HP Labs
Hao Jiang - San Francisco State University
Yang Yi - University of Kansas

Hardware and System Security (HSS)

Miodrag Potkonjak, UCLA (Chair)
Bao Liu, University of Texas at San Antonio (Co-Chair)

Committee Members:
Jia Di - University of Arkansas
Domenic Forte - University of Florida
Ken Mai - Carnegie Mellon University
Seetharam Narasimhan - Intel Corp
Nicolas Sklavos - Computer Engineering & Informatics Department, University of Patras
Xuehui Zhang - Oracle

Design Technology Co-Optimization (DTCO)

Fedor Pikus, Mentor Graphics (Chair)
Rajan Beera, Pall Corporation (Co-Chair)

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Tuhin Guha Neogi - GLOBALFOUNDRIES
Vivek Joshi - GLOBALFOUNDRIES
Murari Mani - AMD
Jimson Mathew - University of Bristol
Mustafa Berke Yelten - Istanbul Technical University
Vladimir Zolotov - IBM

Design Verification and Design Testability (DVFT)

Sreejit Chakravarty, Intel Corporation (Chair)
Vinod Viswanath, Real Intent (Co-Chair)

Committee Members:
George Alexiou - Univ. Of PATRAS
Alberto Bosio - LIRMM - UM
Serge Demidenko - Massey University
Ping Gao - Aries Design Automation
Abhilash Goyal - IEEE Member
Michael Hsiao - Virginia Tech
Jon Nafziger - Texas Instruments
Suriya Natarajan - Intel Corporation
Dimitris Nikolos - nikolosd
Kiran Puttaswamy - Samsung
Spyros Tragoudas - Southern Illinois University Carbondale
Miroslav N. Velev - Aries Design Automation
Arnaud Virazel - LIRMM
HUNG-PIN WEN - National Chiao Tung University
Cai Yu - SK Hynix
Wenwei Zha - Qualcomm Inc

EDA, Physical Design, and IP Cores (EDA)

Anand Iyer, Microsoft (Chair)
Vamsi Srikantam (Co-Chair)

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Yici Cai - Tsinghua Univ.
Zhuo Feng - Michigan Technological University
Eric Foreman - IBM
Dhruva Ghai - ORIENTAL UNIVERSITY INDORE
Shih-Hsu Huang - Chung Yuan Christian University
Srinivas Katkoori - University of South Florida
Srini Krishnamoorthy - Advanced Micro Devices Inc.
Yu-min Lee - National Chiao Tung University
Rung-Bin Lin - Yuan Ze University
Ofelya Manukyan - Synopsys
Rajeev Murgai - Synopsys India Pvt. Ltd.
Andre Reis - UFRGS
Emre Salman - Stony Brook University
Takashi Sato - Kyoto University
Jia Wang - Illinois Institute of Technology
Hua Xiang - IBM Research
Guo Yu - Oracle
Min Zhao - oracle

Emerging Process&Device Tech. &Design Issues (EDT)

Paul Tong, Pericom Semiconductor (Chair)
Swaroop Ghosh, University of South Florida (Co-Chair)

Committee Members:
Shih-Hung Chen - Imec
Qiang Cui - Qorvo Inc.
Jayita Das - Intel
Nikos Konofaos - AUTh
Chun-Yu Lin - National Taiwan Normal University
Guofu Niu - guofu.niu
Renato ribas - UFRGS
Swatilekha Saha - Cypress Semiconductor Corporation
Aida Todri-Sanial - CNRS-LIRMM
Rasit Onur Topaloglu - IBM
Huaqiang Wu - Tsinghua University

Integrated Circuit Design (ICD)

Charles Augustine, Intel Circuit Research Lab (Chair)
Steve Heinrich-Barna, Texas Instruments, Inc (Co-Chair)

Committee Members:
Ali Afzali-Kusha - University of Tehran
Plamen Asenov - Gold Standard Simulations
Karan Bhatia - Texas Instruments, Inc.
Srinivas Bodapati - Intel
Paulo Butzen - Universidade Federal do Rio Grande - FURG
Subho Chatterjee - Intel corporation
Minki Cho - Intel Corp.
Mike DiRenzo - Texas Instruments
Guanming Huang - Synopsys
Ajay Joshi - Boston University
Rouwaida Kanj - American University of Beirut
Jin-Fu Li - National Central University
Aswin Mehta - Texas Instruments Inc
Riaz Naseer - Intel Corporation
Arijit Raychowdhury - Georgia Institute of Technology
Kurt Schwartz - Texas Instruments
Jeremy Tolbert - Samsung Austin R&D Center
Haibo Wang - Texas A&M International University
Cheng Zhuo - Intel Corp.Cheng Zhuo - Intel

Smart Sensors for IoT –Design &Technology (SSDT)

Xiaoning Qi, Intel (Chair)
Vijay Raghunathan, Purdue University (Co-Chair)

Committee Members:
Vittorio Ferrari - University of Brescia
Kamesh Gadepally - GigaCom Semiconductor
Michel Maharbiz - U.C. Berkeley
Libor Rufer - University of Grenoble
Thilo Sauter - Danube University Krems

System-level Design and Methodologies (SDM)

Rajesh Berigei, Texas Instruments(Chair)
Shiyan Hu, Michigan Technological University (Co-Chair)

Committee Members:
Ik Joon Chang - Kyunghee University
Kai Cong - Intel Corporation
Rosilde Corvino - Intel
Abhijit Davare - Intel
Fabiano Hessel - PUCRS
Selcuk Kose - University of South Florida
Hana Kubatova - CTU in Prague
Hai (Helen) Li - University of Pittsburgh
Duo Liu - Chongqing University
Vivek Nandakumar - Synopsys
Gabriela Nicolescu - Ecole Polytechnique de Montréal
Antonio Nunez - University of Las Palmas GC
Sudeep Pasricha - Colorado State University
Shana-Jang Ruan - National Taiwan University of Sci. and Tech.
Tuna Tarim - Texas Instrument, Inc.
Tianyi Wang - Florida International University
Yu Wang - Auburn University
Bei Yu - The Chinese University of Hong Kong

3 Dimensional Integration &Adv. Packaging (TDIP)

Sung Kyu Lim, Georgia Tech (Chair)
Kambiz Samadi, Qualcomm Technologies, Inc. (Co-Chair)

Committee Members:
Ismail Bustany - Mentor Graphics
Nauman Khan - Intel Coporation
Dae Hyun Kim - Washington State University
Manuel Luschas - Broadcom
Shreepad Panth - Altera Corporation
Yiyu Shi - University of Notre Dame
Saurabh Sinha - ARM Inc.
Jianyong Xie - Intel
HL Yiu - Hong Kong Science and Technology Parks
Hirokazu Yonezawa - Panasonic Corporation
Payman Zarkesh-Ha - University of New Mexico
Ehrenfried Zschech - Fraunhofer IKTS

ISQED 2016
GENERAL INFORMATION

March 15-16, 2016
Santa Clara Convention Center
5001 Great America Pkwy, Santa Clara, CA 95054

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Embedded Tutorials

Chair:
Hai (Helen) Li - *University of Pittsburgh*

Co-Chair:
Vinod Viswanath - *Real Intent*
•••••••••••••
Tuesday, March 15, 4:00PM - 4:50PM
Great America Ballrooms

On-Chip Nonvolatile Memory Designs for Energy-Efficient IoT

Prof. Meng-Fan (Marvin) Chang
National Tsing Hua University (NTHU), Taiwan

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Tuesday, March 15, 4:50PM - 5:40PM
Great America Ballrooms

Pattern Recognition and Learning with Neuromorphic Cognitive Systems

Prof. Giacomo Indiveri
University of Zurich, Switzerland
•••••••••••••
Wednesday, March 16, 10:10AM - 11:00AM
Great America Ballrooms

Low Power SoC System Design
A Systems Approach to Power Management Techniques, Power and Performance Optimizations, Thermal and Energy Management of Systems-on-Chip

Rajiv Muralidhar
Senior Platform Architect, Intel Corporation

Wednesday, March 16, 11:00AM - 11:50AM
Great America Ballrooms

Building Neuromorphic Computing Systems with Emerging Device Technologies

Dr. John Paul Strachan
Senior Research Scientist, Hewlett Packard Laboratories

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KEYNOTE SPEECHES

Tuesday, March 15, 9:00AM - 10:10AM
Great America Ballrooms

New Frontiers in Hardware Security & Trust

Prof. Mark M. Tehranipoor
Charles E. Young Professor in Cybersecurity
ECE Department
University of Florida

Avoiding The Dark Side Of The Cloud Using Secure And Reliable IoT Devices

Navraj Nandra
Sr. Director of Marketing
DesignWare Interface and Analog IP
Synopsys

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12:35PM-1:45PM
Luncheon Panel Discussion
Hardware and System Security in IoT Era

Chair & Moderator
Prof. Gang Qu - *University of Maryland*

Panelists:
Dr. Seetharam Narasimhan - *Intel*
Prof. Mark M. Tehranipoor - *Florida Institute for Cybersecurity*
Tom Katsioulas - *Mentor Graphics*
Michele D. Guel - *Cisco Systems*
Mohit Arora - *NXP Semiconductors*
Dr. Pim Tuyls - *Intrinsic-ID*

ISQED LUNCH & AWARDS CEREMONY

Tuesday, March 15, 12:00PM-12:35PM
Great America Ballroom

ISQED Best Paper Awards

Recipients of the ISQED 2016 Best Paper Award will be recognized during the ISQED luncheon on Tuesday. List of best papers is shown in Page 3 of this document.

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TECHNICAL SESSIONS

There are a total of 16 paper sessions held on Tuesday and Wednesday. Technical sessions are held in the format of three parallel tracks in **Great America Meeting Rooms 1-3**.

Poster Papers & Mixer

Poster display will take place on Tuesday afternoon 5:30PM-7:00PM in the Atrium area outside of **Great America Meeting Rooms 1-3**. Authors will be available to discuss their works and to answer questions. Refreshments will be served.

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ON-SITE REGISTRATION

Tentative time schedule of on-site registration is as follows:

Tuesday, March 15   *8:00AM-5:00PM*
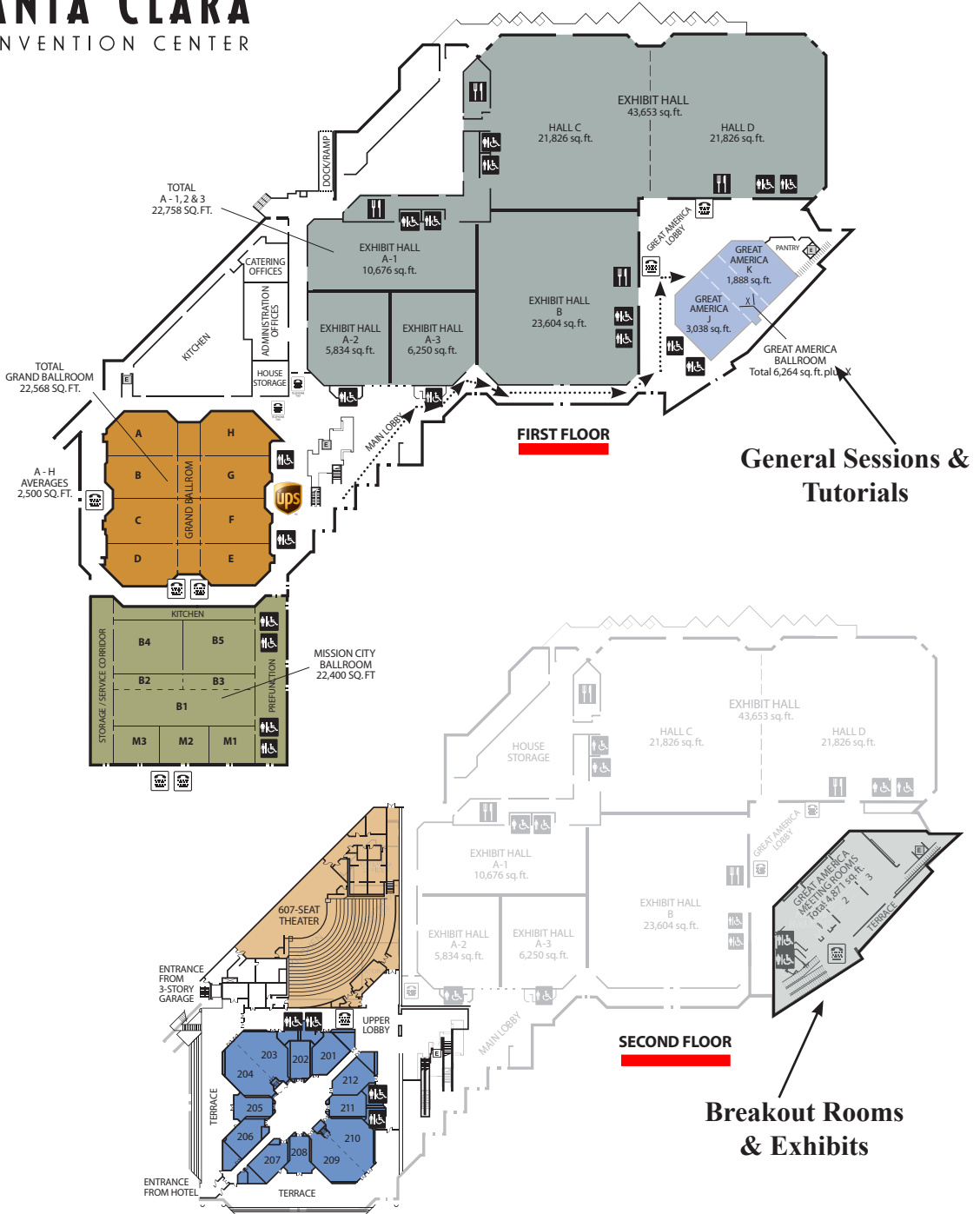*Wednesday, March 16*   *8:00AM-1:00PM*

Registration desk location will be alternate between the location beside Great America meeting rooms 1-3, and the location right outside Great America Ballrooms.

Co-located Events

IoT Summit
March 17-18
Great America Ballrooms
www.IoT-Summit.org

SANTA CLARA
CONVENTION CENTER

FIRST FLOOR

EXHIBIT HALL
43,653 sq.ft.

HALL C
21,826 sq.ft.

HALL D
21,826 sq.ft.

DOCK/RAMP

TOTAL
A - 1,2 & 3
22,758 SQ. FT.

CATERING OFFICES

ADMINISTRATION OFFICES

HOUSE STORAGE

KITCHEN

EXHIBIT HALL
A-1
10,676 sq.ft.

EXHIBIT HALL
A-2
5,834 sq.ft.

EXHIBIT HALL
A-3
6,250 sq.ft.

EXHIBIT HALL B
23,604 sq.ft.

GREAT AMERICA LOBBY

GREAT AMERICA K
1,888 sq.ft.

PANTRY

GREAT AMERICA J
3,038 sq.ft.

GREAT AMERICA BALLROOM
Total 6,264 sq.ft. plus X

TOTAL
GRAND BALLROOM
22,568 SQ. FT.

A - H
AVERAGES
2,500 SQ. FT.

GRAND BALLROM

A	H
B	G
C	F
D	E

MAIN LOBBY

UPS

General Sessions & Tutorials

KITCHEN

STORAGE / SERVICE CORRIDOR

PREFUNCTION

B4	B5
B2	B3
B1	
M3	M2	M1

MISSION CITY BALLROOM
22,400 SQ. FT

SECOND FLOOR

EXHIBIT HALL
43,653 sq.ft.

HALL C
21,826 sq.ft.

HALL D
21,826 sq.ft.

HOUSE STORAGE

EXHIBIT HALL
A-1
10,676 sq.ft.

EXHIBIT HALL B
23,604 sq.ft.

EXHIBIT HALL
A-2
5,834 sq.ft.

EXHIBIT HALL
A-3
6,250 sq.ft.

GREAT AMERICA LOBBY

GREAT AMERICA MEETINGROOMS
Total 4,871 sq. ft.

TERRACE

607-SEAT THEATER

ENTRANCE FROM 3-STORY GARAGE

UPPER LOBBY

MAIN LOBBY

203	202	201
204		212
205		211
206		210
207	208	209

TERRACE

ENTRANCE FROM HOTEL

TERRACE

Breakout Rooms & Exhibits

PROGRAM AT A GLANCE

ISQED 2016 PROGRAM AT A GLANCE

DATE	TIME	
TUESDAY 3/15/2016	*9:00AM-10:10AM*	**PLENARY SESSION 1P** (GREAT AMERICA BALLROOMS) **KEYNOTE SPEECHES BY:** **PROF. MARK M. TEHRANIPOOR** - *UNIVERSITY OF FLORIDA*, **NAVRAJ NANDRA** - *SYNOPSYS*
	10:10AM-10:30AM	**MORNING BREAK**
	10:30AM-11:50AM	**SESSION 1A** LOW POWER MEMORY & LOGIC DESIGN GREAT AMERICA MEETING ROOM 1 · **SESSION 1B** ADVANCED THREE-DIMENSIONAL INTEGRATED CIRCUITS GREAT AMERICA MEETING ROOM 2 · **SESSION 1C** TECHNOLOGY BEYOND CMOS GREAT AMERICA MEETING ROOM 3
	12:00PM-1:45PM	**ISQED PANEL & LUNCHEON** (GREAT AMERICA BALLROOMS) **BEST PAPER AWARDS , COMMITTEE RECOGNITION** **LUNCHEON PANEL DISCUSSION** **HARDWARE AND SYSTEM SECURITY IN IOT ERA** CISCO SYSTEMS, INTEL, MENTOR GRAPHICS, NXP SEMICONDUCTORS, INTRINSIC-ID, UNIVERSITY OF FLORIDA, UNIVERSITY OF MARYLAND
	2:00PM-3:40PM	**SESSION 2A** NETWORK ON A CHIP GREAT AMERICA MEETING ROOM 1 · **SESSION 2B** IOT DESIGN CONCEPTS GREAT AMERICA MEETING ROOM 2 · **SESSION 2C** CIRCUITS AND ARCHITECTURE FOR EMERGING LOGIC AND MEMORY TECHNOLOGIES GREAT AMERICA MEETING ROOM 3
	3:40PM-4:00PM	**AFTERNOON BREAK**
	4:00PM-4:50PM	**EMBEDDED TUTORIAL 1** ON-CHIP NONVOLATILE MEMORY DESIGNS FOR ENERGY-EFFICIENT IOT GREAT AMERICA BALLROOMS · **SESSION 3A** ON-CHIP MACHINE LEARNING AND NEUROMORPHIC COMPUTING
	4:50PM-5:40PM	**EMBEDDED TUTORIAL 2** PATTERN RECOGNITION AND LEARNING WITH NEUROMORPHIC COGNITIVE SYSTEMS GREAT AMERICA BALLROOMS · GREAT AMERICA MEETING ROOM 1
	5:40PM-7:00PM	**POSTER PAPERS & MIXER** HALLWAY OUTSIDE GREAT AMERICA MEETINGS ROOMS
WEDNESDAY 3/16/2016	*8:30AM-9:50AM*	**SESSION 4A** POWERING IOT GREAT AMERICA MEETING ROOM 1 · **SESSION 4B** ENABLING 5NM TECHNOLOGY NODE GREAT AMERICA MEETING ROOM 2 · **SESSION 4C** ADVANCED TESTING CONCEPTS GREAT AMERICA MEETING ROOM 3
	9:50AM-10:10AM	**MORNING BREAK**
	10:10AM-11:00AM	**EMBEDDED TUTORIAL 3** LOW POWER SOC SYSTEM DESIGN - A SYSTEMS APPROACH TO POWER MANAGEMENT TECHNIQUES, POWER AND PERFORMANCE OPTIMIZATIONS, THERMAL AND ENERGY MANAGEMENT OF SYSTEMS-ON-CHIP GREAT AMERICA BALLROOMS
	11:00AM-11:50AM	**EMBEDDED TUTORIAL 4** BUILDING NEUROMORPHIC COMPUTING SYSTEMS WITH EMERGING DEVICE TECHNOLOGIES GREAT AMERICA BALLROOMS
	12:00PM-1:00PM	**LUNCH BREAK**
	1:00PM-2:40PM	**SESSION 5A** EMBEDDED SYSTEMS GREAT AMERICA MEETING ROOM 1 · **SESSION 5B** HARDWARE AND SYSTEM SECURITY GREAT AMERICA MEETING ROOM 2 · **SESSION 5C** ANALOG DESIGN GREAT AMERICA MEETING ROOM 3
	2:40PM-3:00PM	**AFTERNOON BREAK**
	3:00PM-4:20PM	**SESSION 6A** DESIGN OPTIMIZATION FOR PERFORMANCE, RELIABILITY, AND YIELD GREAT AMERICA MEETING ROOM 1 · **SESSION 6B** EDA FOR DESIGN EXPLORATION & ANALYSIS BEYOND MOORE'S LAW GREAT AMERICA MEETING ROOM 2 · **SESSION 6C** SENSORS FOR IOT GREAT AMERICA MEETING ROOM 3

Tuesday March 15

9:00AM-9:30AM
Great America Ball Rooms

New Frontiers in Hardware Security and Trust

Prof. Mark M. Tehranipoor
Florida Institute for Cybersecurity

Hardware security domain has received significant attention from researchers in academia, industry, and government due mainly to the globalized design, fabrication, and assembly of integrated circuits and systems. The complexity of today's electronic components and systems supply chain has made it increasingly vulnerable to malicious activities, security attacks, and counterfeiting activities. In this talk, we will first analyze these vulnerabilities and threats. We will then present challenges dealing with emerging attacks and threats and present potential solutions to addressing them. Finally, we will present opportunities that securing hardware can provide at different application domains, different levels of abstraction, and from nano-device to systems.

About Mark M. Tehranipoor
Mark Tehranipoor is currently the Intel Charles E. Young Professor in Cybersecurity at the ECE Department, University of Florida. His current research interests include: hardware security and trust, counterfeit electronics detection and prevention, supply chain risk management, and reliable and testable circuit design. Dr. Tehranipoor has published over 250 journal articles and refereed conference papers and has given more than 150 invited talks and keynote addresses since 2006. He has published six books and ten book chapters. He is a recipient of several best paper awards as well as the 2008 IEEE Computer Society (CS) Meritorious Service Award, the 2012 IEEE CS Outstanding Contribution, the 2009 NSF CAREER Award, and the 2014 MURI award. His projects are sponsored by both the industry (Semiconductor Research Corporation (SRC), Texas Instruments, Freescale, Comcast, Honeywell, LSI, Avago, Mentor Graphics,R3Logic, Cisco, Qualcomm, MediaTeck, etc.) and Government (NSF, ARO, MDA, DOD, AFOSR, DOE, etc.). He serves on the program committee of more than a dozen leading conferences and workshops. He served as Program and General Chairs of several leading conferences and workshops. Prior to joining UF, Dr. Tehranipoor was the founding director of CHASE and CSI centers at the University of Connecticut. He co-founded a new symposium called IEEE International Symposium on Hardware-Oriented Security and Trust (HOST) and served as HOST-2008 and HOST-2009 General Chair. He is currently serving as HOST's Chair of Steering Committee. He is also the co-founder of Trust-Hub (www.trust-hub.org). He served as an Associate EIC for IEEE Design & Test, an IEEE Distinguished Speaker, and an ACM Distinguished Speaker from 2010 to 2014. He is currently serving as an Associate Editor for JETTA, JOLPE, Transactions on VLSI (TVLSI), and Transactions on Design Automation for Electronic Systems (TODAES). Dr. Tehranipoor is a Senior Member and Golden Core Member of the IEEE and Member of ACM and ACM SIGDA.

Tuesday March 15

9:30AM-10:00AM
Great America Ball Rooms

Avoiding The Dark Side Of The Cloud Using Secure And Reliable IoT Devices

Navraj Nandra
Synopsys

Keeping the enormous amounts of data being generated by billions of smart connected devices ultimately stored in the cloud – secure - is a hotly debated topic. The number of connected devices is expected to reach 50 billion by the end of this decade. Today, it is estimated that 70% of IoT devices contain serious security vulnerabilities, 100 car models are affected with security flaws. This presentation will provide proposals for integrated silicon solutions that help prevent a wide range of evolving security threats in connected devices such as theft, tampering, side channels attacks, malware and data breaches.

About Navraj Nandra

Navraj Nandra is the Sr. Director of Marketing for the DesignWare Interface and Analog IP at Synopsys. He has worked in the semiconductor industry since the mid 80's as an analog/mixed signal IC designer for Philips Semiconductors, Austria Micro Systems, (San Jose & Austria) and EM-Marin (Switzerland). He has been responsible for the complete design of a number of analog front ends in application areas such as digital audio, RFID and automotive. He joined Synopsys from Barcelona Design where he was Director of Application Engineering. During his four years at Barcelona he was responsible for pre- and post-sales support for Barcelona's analog synthesis technology. Navraj holds a masters degree in Microelectronics, majoring in analog IC design, from Brunel University and a post-graduate diploma in Process Technology from Middlesex University. He has presented at numerous technical conferences on mixed-signal design, analog IP and analog synthesis/EDA.

Tuesday March 15

12:35PM–1:45PM
Great America Ball Rooms

Hardware and System Security in IoT Era

Chair & Moderator:
Prof. Gang Qu - University of Maryland

Panelists:
Seetharam Narasimhan - Intel
Mark M. Tehranipoor - Florida Institute for Cybersecurity
Tom Katsioulas - Mentor Graphics
Michele D. Guel - Cisco Systems
Mohit Arora - NXP Semiconductors
Pim Tuyls - Intrinsic-ID

Summary:
Hardware is the foundation of any security system. In recent years, a growing number of software-based security solutions have been migrated to hardware for enhanced resistance against software-based attacks. However, recent research has revealed that hardware is also subject to a number of security attacks. The emerging Internet-of-Things and Cyber-Physical Systems further demand achieving security for a complex system including software, hardware and firmware components against software, hardware and/or firmware-based attacks in a dynamic and possibly hostile environment under tight resource constraints. In this interactive session, a group of leading industry experts will explore the various opportunities and challenges that the security requirement brings to the semiconductor industry.

Prof. Gang Qu
University of Maryland

Gang Qu received his Ph.D. degree in computer science from the University of California, Los Angeles, in 2000. He is currently a professor in the Department of Electrical and Computer Engineering and Institute for Systems Research, University of Maryland at College Park. He is also a member of the Maryland Cybersecurity Center and the Maryland Energy Research Center. Dr. Qu is the director of Maryland Embedded Systems and Hardware Security (MeshSec) Lab and the Wireless Sensors Laboratory. His primary research interests are in the area of embedded systems and VLSI CAD with focus on low power system design and hardware related security and trust. He studies optimization and combinatorial problems and applies his theoretical discovery to applications in VLSI CAD, wireless sensor network, bioinformatics, and cybersecurity.

Seetharam Narasimhan
Intel

Seetharam Narasimhan is a Lead Security Researcher at the Security Center of Excellence, Platform Engineering Group of Intel Corporation, Hillsboro, Oregon, USA. He obtained a Ph.D. in Computer Engineering from Case Western Reserve University (USA) in 2012 and a B.E. (Hons.) in Electronics and Telecommunication Engineering from Jadavpur University (India) in 2006. His research interests include: Hardware Security, Ultralow power and reliable nanoscale circuits, as well as Bio-medical circuits and systems. He is the co-author of three book chapters, and more than 40 publications in international journals and conferences of repute.

Tom Katsioulas
Mentor Graphics

Tom Katsioulas is currently heading the market development ecosystem strategy for the Design for Security initiative at Mentor Graphics. Tom has several years' experience in semiconductor, IP, EDA, embedded systems, and enterprise software applications. He has led or advised many startups in design methodology, analytics-driven process automation, industrial IoT, and enterprise software applications. Tom led corporate strategy at Forte Design Automation and founded AmmoCore Technology, where he invented its massively parallel physical design platform. He was also a methodology consultant at Synopsys, a marketing director at Cadence, and an applications engineer, chip designer, and CAD software developer at Digital Equipment Corporation. Tom holds an M.S. in Electrical Engineering and Computer Science from the University of Massachusetts (Amherst, MA) and a B.S. in Computer Engineering from the University of Bridgeport (Connecticut).

Michele D. Guel
Cisco Systems

Michele's passion is to inspire, lead and mentor people. She joined Cisco in March 1996 as the founding member of Cisco's internal security team, which is now the Security and Trust Organization under John Stewart. During her 20 years at Cisco, she has had the opportunity to work on all facets of cybersecurity security. In 2010, Michele was promoted to Distinguished Engineer, one of 8 female DEs across Cisco. She recently co-founded the Cisco Women in Cybersecurity Community which has strong focus on expanding awareness about the numerous and exciting opportunities in the field of cybersecurity. Outside of Cisco, Michele has been an avid participant, speaker, teacher, influencer and evangelist in the cyber security industry for over 27 years. Her most recent work focuses on developing & codifying the practice and art of Information Security Engineering & Architecture, with an emphasis on cloud and IoT. Her motto is all about "Building it in and not bolting it on".

Mohit Arora
NXP Semiconductors

Mohit Arora is a Senior Design and Security Architect with NXP Semiconductors, Security and Connectivity business group and is located in Austin. Within NXP, he is responsible for architecture of i.MX low power family of application processors with "Embedded Security" as one of his main expertise. Previously as a system architect, he has been involved in definition and architecture for MCU/MPU based SoCs targeted for general purpose, smart metering and Point of Sale(PoS) market space. He is actively involved as "Industrial Liaison" in several SRC security research projects. He earned a Bachelor's degree in Electronics and Communication Engineering from Netaji Subhas Institute of Technology (NSIT), India in 2000. He is also the author of the book "The Art of Hardware Architecture" and have more than 50 international publications and several patents in the field of embedded security.

Pim Tuyls
Intrinsic-ID

Dr. Pim Tuyls is one of the pioneers of the field of Physical Unclonable Functions and holds 50+ patents in this field. He started the scientific and technological work within Philips Research in the early 2000's where he co-founded Intrinsic-ID. He has been a visiting professor at COSIC from 2004-2008. Pim is heading Intrinsic-ID the world-leader in Cyber Physical Security Systems, since 2010. Recently, he moved to Silicon Valley to accelerate its further growth.

Tutorial 1

Tuesday March 15

4:00PM-4:50PM
Great America Ball Rooms

On-chip Nonvolatile Memory Designs for Energy-efficient IoT

Prof. Meng-Fan (Marvin) Chang
National Tsing Hua University (NTHU), Taiwan

Summary: Memory has become one of the bottlenecks in the development of IoT and wearable devices with low energy consumption. This tutorial addresses trends in the development of on-chip (embedded) non-volatile memory (NVM) for energy-efficient IoT applications. We will examine a variety of NVM technologies, including Flash, OTP/MTP, resistive RAM, phase-change memory (PCM), and STT-MRAM. This tutorial will explore the challenges faced by researchers in the design of low-power and high-speed circuits for on-chip NVM macros. We will also look at some state-of-the-art silicon-verified circuit techniques, including high-speed and low-voltage NVM macros. The implementation of NVM devices beyond conventional applications, such as nonvolatile-logics (nvLogics) and nonvolatile-SRAM/TCAM (nvSRAM/nvTCAM) for nonvolatile processors, will also be discussed.

About Meng-Fan (Marvin) Chang

Dr. Chang is a full Professor in the Dept. of Electrical Engineering of National Tsing Hua University (NTHU), Taiwan. Since 2011, he has also served as the Associate Executive Director of National Program for Intelligent Electronics (NPIE) in Taiwan. Dr. Change obtained considerable practical experience before joining NTHU in 2006, having spent more than ten years working in industry. Between 1997 and 2006, Dr. Chang worked in the development of SRAM/ROM/Flash macros/compilers at Mentor Graphics (New Jersey, US), TSMC (Taiwan), and the Intellectual Property Library Company (Taiwan). His research interests include circuit design for volatile and nonvolatile memory, 3D-Memory, spintronics and memristor logics, computing-in-memory, and circuit-device-interactions in non-CMOS devices. Since 2010, Dr. Chang has authored or co-authored more than 40 conference papers (including 11 ISSCC, 11 VLSI Symposia, 5 IEDM, 3 DAC papers) as well as 25+ IEEE journal papers. He also holds more than 25 U.S. patents and has been serving on technical program committees for IEDM, A-SSCC, ISCAS, VLSI-DAT, EDSSC, NVMSA, and numerous international conferences. He received the Academia Sinica Junior Research Investigators Award in 2012, the Ta-You Wu Memorial Award of National Science Council (NSC-Taiwan) in 2011, and the Outstanding Industrial Collaboration Award from NTHU in 2012. He has also received numerous awards from the Taiwan National Chip Implementation Center (CIC), the Macronix Golden Silicon Awards, and ITRI.

<u>Tuesday March 15</u>

4:50PM-5:40PM
Great America Ball Rooms

Pattern Recognition and Learning with Neuromorphic Cognitive Systems

Prof. Giacomo Indiveri
University of Zurich, Switzerland

Summary: Artificial computing systems are vastly outperformed by biological neural processing ones for many practical tasks that involve sensory perception and real-time interactions with the environment, especially when size and energy consumption are factored in. One of the reasons is that the architecture of nervous systems, in which billions of neurons communicate in parallel mainly via asynchronous action potentials, is very different from that of today's mainly serial and synchronous logic devices and systems. Recent machine learning algorithms have taken inspiration from the nervous system to develop neuro-computing algorithms that are showing state-of-the-art performance in pattern recognition tasks. In parallel, different types of brain-inspired hardware architectures are being developed that reproduce some of the principles of computation used by the nervous system. These architectures represent a promising technology for both implementing the latest generation of neural networks, and for building faithful models of biological neural processing systems. In this tutorial I will present examples of spike-based neural network architectures that can be used to perform neural computation, signal processing, and pattern recognition. I will cover the design of large-scale networks of spiking neurons in VLSI technology, presenting a set of analog and digital electronic circuits that can be used to implement spiking neurons and spike-timing dependent plasticity learning synapses. I will show examples of VLSI neuromorphic information processing systems and present application examples that exploit their on-line learning properties.

About Giacomo Indiveri

Giacomo Indiveri is a Professor at the Faculty of Science of the University of Zurich, Switzerland. He obtained an M.Sc. degree in Electrical Engineering and a Ph.D. degree in Computer Science from the University of Genoa, Italy. Indiveri was a post-doctoral research fellow in the Division of Biology at the California Institute of Technology (Caltech) and at the Institute of Neuroinformatics of the University of Zurich and ETH Zurich, where he attained the Habilitation in Neuromorphic Engineering in 2006. He is an ERC fellow and an IEEE Senior member. His research interests lie in the study of real and artificial neural processing systems, and in the hardware implementation of neuromorphic cognitive systems, using full custom analog and digital VLSI technology.
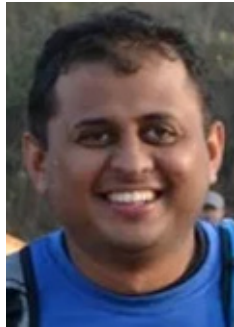
<u>Wednesday March 16</u>

10:10AM-11:00AM
Great America Ball Rooms

Low Power SoC System Design

Rajiv Muralidhar
Intel Corporation

Summary: The last few years has seen the emergence of highly integrated embedded System-on-a-chip (SoC) architectures for several usages and platforms like high end mobile devices, tablets, smartphones and wearables. While each SoC component or accelerator can be optimized in various ways through the design phase, overall platform integration and platform power optimization is a growing challenge that is done in several different ways, specific to the final end system, operating system, and end usage intended for the device. Another trend has been the emergence of multi-core and multi-threaded architectures for all kinds of computing devices, ranging from cell phones, tablets, laptops, and netbooks, to high end computing systems, servers, etc. As the number of cores and threads-per-core increases, such systems present unique challenges in terms of scheduling, energy efficiency, temperature, heterogeneity, etc. Power management and optimization research in the last couple of decades has spanned multiple areas such as process technology, circuit/design optimizations, hardware, micro-architectural techniques for processors, caches, memories, dynamic voltage/frequency scaling of processors and other components, power management of individual components such as hard drives, external memories, and network interfaces, power-aware compiler optimizations, operating system optimizations for energy efficiency, and system/platform-wide power and thermal management. This tutorial covers end to end system design techniques from a power, energy and thermal perspective covering the most important energy efficiency techniques used in current generation Android, Chrome and Windows based smartphones, tablets, wearables and other small form factor devices.

About Rajiv Muralidhar

Rajeev Muralidhar is a Senior Platform Architect in Intel's Mobile Communications Group, where he works on power management architectures for Intel SOC platforms. Previously, he worked in Intel Architecture Labs on network processor stacks, stability of internet routing and control plane protocols and quality of service for wired and wireless networks. Rajeev has been with Intel since 2000; he has a Bachelors from NIT, Surathkal (India) and Masters from Rutgers University, both in Computer Engineering. He is also a visiting researcher at Rutgers University's NSF Center for Autonomic Computing, where he collaborates with researchers on power management in large many core systems.

Tutorial 4

<u>Wednesday March 16</u>

11:00AM-11:50AM
Great America Ball Rooms

Building Neuromorphic Computing Systems with Emerging Device Technologies

Dr. John Paul Strachan
Hewlett Packard Laboratories

Summary: Neuromorphic – or brain-inspired – computing is a multi-disciplinary field of research aimed at extending our computational capabilities to tackle traditionally difficult problems, including perception, decision-making, prediction, and sensorimotor control. There is added urgency with the simultaneously decreasing benefits of CMOS scaling and increasing data processing demands. Along with new neuromorphic architectures and algorithms, an important area of research goes down to the device level to attempt to mimic neural functions. There are a number of emerging device technologies that may be attractive candidates for this functionality, including memristors. This tutorial will survey the device level concepts and properties of memristors and how they can be applied to building future brain-inspired computing systems. Topics covered include the conceptual requirements for mimicking the nervous system with some of the open questions. Chua's local activity principle will be introduced, how it underpins the generation of spiking behavior in neurons, and some physical realizations. Various examples of artificial neural networks and their implementations with emerging devices will be surveyed, including recurrent and convolutional neural networks, perceptrons, Hopfield networks, and associative memories.

About John Paul Strachan

John Paul Strachan is a Principle Researcher at Hewlett Packard Laboratories. He received a B.S. and M.E. at the Massachusetts Institute of Technology and a PhD in the Department of Applied Physics at Stanford University. After finishing a postdoc at Hewlett Packard Labs, he took a permanent position, joining a broad team of device physicists, materials scientists, architects, electrical engineers, and computer scientists to build future computing machines. His interests include using novel device technologies for applications in memory, computing, and sensing.

SESSION 1A

Tuesday March 15

Low Power Memory & Logic Design

Chair: **Kurt Schwartz**, Texas Instruments
Co-Chair: **Charles Augustine**, Intel

10:30AM
1A.1
Sizing-Priority Based Low-Power Embedded Memory for Mobile Video Applications
Seyed Alireza Pourbakhsh, Xiaowei Chen, Dongliang Chen, Xin Wang, Na Gong, Jinhui Wang
North Dakota State University

10:50AM
1A.2
Bit-Upset Vulnerability Factor for eDRAM Last Level Cache Immunity Analysis
Navid Khoshavi, Xunchao Chen, Jun Wang, Ronald F. DeMara
University of Central Florida

11:10AM
1A.3
Optimizing SRAM Bitcell Reliability and Energy for IoT Applications
Harsh Patel, Farah Yahya, Benton Calhoun
University of Virginia

11:30AM
1A.4
Variability- and Correlation-Aware Logical Effort for Near-Threshold Circuit Design
Jun Shiomi, Tohru Ishihara, Hidetoshi Onodera
Kyoto University

SESSION 1B

Tuesday March 15

Advanced Three-Dimensional Integrated Circuits

Chair: **Payman Zarkesh-Ha**, University of New Mexico

10:30AM
1B.1
Design Challenges and Methodologies in 3D Integration for Neuromorphic Computing Systems
M. Amimul Ehsan[1], Hongyu An[1], Zhen Zhou[2], Yang Yi[1]
[1]University of Kansas, [2]Intel

10:50AM
1B.2
Optimization of Dynamic Power Consumption in Multi-Tier Gate-Level Monolithic 3D ICs
Sheng-En(David) Lin, Partha Pande, Dae Hyun Kim
Washington State University

11:10AM
1B.3
Electromigration-Aware Placement for 3D-ICs
Tiantao Lu[1], Zhiyuan Yang[2], Ankur Srivastava[1]
[1]ECE Department, University of Maryland, [2]University of Maryland, College Park

11:30AM
1B.4
Monolithic 3D IC Design: Power, Performance, and Area Impact at 7nm
Kartik Acharya[1], Kyungwook Chang[1], Bon Woong Ku[1], Shreepad Panth[1], Saurabh Sinha[2], Brian Cline[2], Greg Yeric[2], Sung Kyu Lim[3]
[1]Georgia Institute of Technology, [2]ARM Inc, [3]Georgia Tech

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SESSION 1C

Tuesday March 15

Technology beyond CMOS

Chair: **Brian Cline**, ARM
Co-Chair: **Rajan Beera**, Pall Corporation

10:30AM
1C.1
Nanodevices to Nanosystems: Carbon Nanotube Digital VLSI
Gage Hills[1], Max Shulaker[2], Chi-Shuen Lee[2], H.-S. Philip Wong[2], Subhasish Mitra[2]
[1]Department of Electrical Engineering, Stanford University, [2]Stanford University

10:50AM
1C.2
Negative Capacitance for Low Power Computing
Asif Khan and S Salahuddin
University of California, Berkeley

11:10AM
1C.3
Tunnel-FET: The Prospects and Challenges Ahead
Uygar Avci, Daniel Morris, Ian Young
Intel

11:30AM
1C.4
Beyond Moore's Law: It's More than Just Transistors
Saurabh Sinha, Greg Yeric, Lucian Shifren, Brian Cline
ARM Inc.

SESSION 2A

Tuesday March 15

Network on a Chip

Chair: **Hai (Helen) Li**, University of Pittsburgh
Co-Chair: **Rajesh Berigei**, Texas Instruments

2:00PM
2A.1
Maximizing the Performance of NoC-based MPSoCs under Total Power and Power Density Constraints
Alireza Shafaei Bejestan[1], Yanzhi Wang[1], Lizhong Chen[2], Shuang Chen[1], Massoud Pedram[3]
[1]University of Southern California, [2]Oregon State University, [3]USC

2:20PM
2A.2
Process Variation Aware Crosstalk Mitigation for DWDM based Photonic NoC Architectures
SAI VINEEL REDDY CHITTAMURU, Ishan Thakkar, Sudeep Pasricha
Colorado State University

2:40PM
2A.3
Memory-Aware Circuit Overlay NoCs for Latency Optimized GPGPU Architectures
Venkata Yaswanth Raparti[1] and Sudeep Pasricha[2]
[1]Colorado State University, Fort Collins, [2]Colorado State University

3:00PM
2A.4
Design Guidelines for Embedded NoCs on FPGAs
Noha Gamal[1], Hossam Fahmy[2], Yehea Ismail[3], Hassan Mostafa[2]
[1]Mentor Graphics, [2]Cairo University, [3]CND at Zewail city and AUC

3:20PM
2A.5
A Delay Variation and Floorplan Aware High-level Synthesis Algorithm with Body Biasing
Koki Igawa, Youhua Shi, Masao Yanagisawa, Nozomu Togawa
Waseda University

SESSION 2B

Tuesday March 15

IoT Design Concepts

Chair: **Stephen Heinrich-Barna**, Texas Instruments
Co-Chair: **Charles Augustine**, Intel

2:00PM
2B.1
IoT Memory Trends
Rashmi Sachan
Texas Instruments

2:20PM
2B.2
NVM Memory Requirements for a Secure IoT Ecosystem
Jim Lipman
Sidense Corp

2:40PM
2B.3
Challenges and Trends in Switched Capacitor Power Converters in an IoT World
Mervin John and Yogesh Ramadass
Texas Instruments

3:00PM
2B.4
Embedded Integrated Microdevices for the Internet of Things
Mark Bachman
University of California, Irvine

3:20PM
2B.5
Designing for Security in SoC-driven Supply Chains
Tom Katsioulas
Mentor Graphics

SESSION 2C

Tuesday March 15

Circuits and Architecture for Emerging Logic and Memory Technologies

Chair: **Paul Tong**, Pericom Semiconductor
Co-Chair: **Swaroop Ghosh**, University of South Florida

2:00PM
2C.1
Exploring the Use of Volatile STT-RAM for Energy Efficient Video Processing
Hengyu Zhao[1], Hongbin Sun[1], Qiang Yang[2], Tai Min[1], Nanning Zheng[1]
[1]Xi'an Jiaotong University, [2]Changhong Electric Co., Ltd

2:20PM
2C.2
Low Power Data-Aware STT-RAM based Hybrid Cache Architecture
Mohsen Imani[1], Shruti Patil[1], Tajana Rosing[2]
[1]University of California San Diego, [2]UCSD

2:40PM
2C.3
Yield estimation and statistical design of memristor cross-point memory systems
Jizhe Zhang[1] and Sandeep Gupta[2]
[1]Electrical Engineering Department, University of Southern California, [2]University of Southern California (USC)

3:00PM
2C.4
ReMAM: Low Energy Resistive Multi-Stage Associative Memory for Energy Efficient Computing
Mohsen Imani[1], Pietro Mercati[2], Tajana Rosing[2]
[1]University of California San Diego, [2]UCSD

3:20PM
2C.5
Ultra-Low-Power Compact TFET Flip-Flop Design for High-Performance Low-Voltage Applications
Navneet Gupta[1], Adam Makosiej[2], Andrei Vladimirescu[3], Amara Amara[3], Costin Anghel[3]
[1]Institut supérieur d'électronique de Paris, France; LETI, Commissariat à l'Energie Atomique et aux Energies Alternatives (CEA-LETI) France;, [2]CEA-LETI, France, [3]Institut supérieur d'électronique de Paris, France

SESSION T12

Tuesday March 15

Tutorial 1 & 2

Chair: **Hai (Helen) Li**, University of Pittsburgh
Co-Chair: **Vinod Viswanth**, Real Intent

4:00PM-4:50PM
T1
On-chip Nonvolatile Memory Designs for Energy-efficient IoT
Meng-Fan (Marvin) Chang
National Tsing Hua University

4:50PM-5:40PM
T2
Pattern Recognition and Learning with Neuromorphic Cognitive Systems
Giacomo Indiveri
University of Zurich

SESSION 3A

Tuesday March 15

On-Chip Machine Learning and Neuromorphic Computing

Chair: **Rouwaida Kanj**, American University of Beirut

4:00PM
3A.1
Sparsely Connected Neural Networks in FPGA for Handwritten Digit Recognition
Luca Saldanha and C Bobda
University of Arkansas

4:20PM
3A.2
Neuromorphic Architectures with Electronic Synapses
S Burc Eryilmaz[1], Siddharth Joshi[2], Emre Neftci[3], Weier Wan[1], Gert Cauwenberghs[2], H.-S. Wong[1]
[1]Stanford University, [2]University of California, San Diego, [3]Department of Cognitive Sciences, University of California Irvine

4:40PM
3A.3
Towards a Scalable Neuromorphic Hardware for Classification and Prediction with Stochastic No-Prop Algorithms
Dan Christiani, Cory Merkel, Dhireesha Kudithipudi
Rochester Institute of Technology

5:00PM
3A.4
High-Performance and Low-Power MPSoC Architectures for Advanced Mobile and Wearable IoT Systems
Lech Jozwiak
Eindhoven University of Technology

SESSION P

Tuesday March 15

Posters

Chair: **Brian Cline**, ARM
Co-Chair: **Kamesh Gadepally**, GigaCom Semiconductor

5:40PM
P1
Equivalence Checking between SLM and RTL Using Machine Learning Techniques
Jian Hu[1], Tun Li[2], Sikun Li[2]
[1]National University of Defense Technology, College of Computer, [2]National University of Defense Technology, School of Computer

5:40PM
P2
Very low supply voltage room temperature test to screen low temperature soft blown fuse fails which result in a resistive bridges
Peter Sarson
ams AG

5:40PM

P3

On-Line Harmonic-Aware Partitioned Scheduling For Real-Time Multi-Core Systems Under RMS

Ming Fan[1], Rong Rong[2], Xinwei Niu[3]

[1]Broadcom Corporation, [2]Florida International University, [3]Penn State Erie, The Behrend College

5:40PM

P4

CovGen: A Framework for Automatic Extraction of Functional Coverage Models

Eman El Mandouh[1] and Amr G. Wassal[2]

[1]Mentor Graphics Corporate, [2]Computer Engineering Dept, Cairo University

5:40PM

P5

In-situ Trojan Authentication for Invalidating Hardware-Trojan Functions

Masaru Oya, Youhua Shi, Masao Yanagisawa, Nozomu Togawa

Waseda University

5:40PM

P6

A 1.3µW, 5pJ/cycle sub-threshold MSP430 processor in 90nm xLP FDSOI for energy-efficient IoT applications

Abhishek Roy[1], Peter Grossmann[2], Steven Vitale[2], Benton Calhoun[3]

[1]University of Virginia, [2]MIT Lincoln Laboratory, Lexington, MA USA, [3]University of Virginia, Charlottesville, VA USA

5:40PM

P7

Statistical Quality Modeling of Approximate Hardware

Seogoo Lee[1], Dongwook Lee[2], Kyungtae Han[3], Emily Shriver[3], Lizy John[2], Andreas Gerstlauer[2]

[1]The Univeristy of Texas at Austin, [2]The University of Texas at Austin, [3]Intel Corporation

5:40PM

P8

Performance Evaluation of Stacked Gate-All-Around MOSFETs at 7 and 10 nm Technology Nodes

Meng-Yen Wu and Meng-Hsueh Chiang

National Cheng Kung University

5:40PM

P9

Fast Stress Analysis for Runtime Reliability Enhancement of 3D IC Using Artificial Neural Network

Lang Zhang[1], Hai Wang[1], Sheldon Tan[2]

[1]University of Electronic Science and Technology of China, [2]University of California at Riverside

5:40PM

P10

Detection of Malicious Hardware Components in Mobile Platforms

Fatih Karabacak[1], Umit Ogras[1], Sule Ozev[2]

[1]Arizona State University, [2]ASU

5:40PM

P11

An Effective BIST Architecture for Power-Gating Mechanisms in Low-Power SRAMs

Alberto Bosio[1], Luigi Dilillo[1], Patrick Girard[1], Arnaud Virazel[1], Leonardo Zordan[2]

[1]LIRMM, [2]Intel Mobile Communication

5:40PM

P12

Performance Evaluation Considering Mask Misalignment in Multiple Patterning Decomposition

Haitong Tian and Martin Wong

University of Illinois at Urbana Champaign

5:40PM

P13

UM-BUS: An Online Fault-Tolerant Bus for Embedded Systems

Jiqin Zhou[1], Weigong Zhang[2], Keni Qiu[2], Xiaoyan Zhu[2]

[1]Beijing Center for Mathematics and Information Interdisciplinary Sciences, [2]College of Information Engineering, Capital Normal University

5:40PM

P14

Low-Leakage and Process-Variation-Tolerant Write-Read Disturb-Free 9T SRAM Cell Using CMOS and FinFETs

Ayushparth Sharma and Kusum Lata

The LNM Institute of Information Technology

5:40PM

P15

Ruggedness evaluation and design improvement of automotive power MOSFETs

Tianhong Ye and Kuan Chee

The University of Nottingham Ningbo China

5:40PM

P16

Device/System Performance Modeling of Stacked Lateral NWFET Logic

Victor Huang[1], Chenyun Pan[1], Azad Naeemi[1], Dmitry Yakimets[2], Praveen Raghavan[2]

[1]Georgia Institute of Technology, [2]imec

5:40PM

P17

Accelerating Physical Level Sub-Component Power Simulation by Online Power Partitioning

Siddharth S. Bhargav, Andrew Kolb, Young H. Cho

University of Southern California

5:40PM

P18

Power Efficient Router Architecture for Wireless Network-on-Chip

Hemanta Kumar Mondal[1], Sri Harsha Gade[2], Raghav Kishore[1], Shashwat Kaushik[1], Sujay Deb[1]

[1]IIIT Delhi, [2]iiitd.ac.in

5:40PM

P19

Preventing Integrated Circuit Piracy via Custom Encoding of Hardware Instruction Set

Vinay Patil[1], Arunkumar Vijayakumar[2], Sandip Kundu[1]
[1]Department of Electrical and Computer Engineering, University of Massachusetts Amherst, [2]Department of Electrical and Computer Engineering, University of Massachusetts, Amherst

5:40PM

P20

Preventing Design Reverse Engineering with Recongurable Spin Transfer Torque LUT Gates

Ted Winograd[1], Hassan Salmani[2], Hamid Mahmoodi[3], Houman Homayoun[1]
[1]George Mason University, [2]Howard University, [3]San Francisco State University

5:40PM

P21

Portable Bio-sensor for Chronic Malaria Detection

Lalitha Sivaraj, nurul amziah md yunus, Mohamad Nazim Mohtar, samsuzana abd aziz, M iqbal saripan, Fakhrul Zaman Rokhani, Zurina Zainal Abidin
University Putra Malaysia

5:40PM

P22

Performance Modeling and Optimization for On-Chip Interconnects in 3D Memory Arrays

Javaneh Mohseni, Chenyun Pan, Azad Naeemi
Georgia Institute of Technology

5:40PM

P23

Near-threshold Circuit Variability in 14nm FinFETs for Ultra-low Power Applications

Sriram Balasubramanian, Ninad Pimparkar, Mangesh Kushare, Vinayak Mahajan, Juhi Bansal, Takashi Shimizu, Vivek Joshi, Kun Qian, Arunima Dasgupta, Karthik Chandrasekaran, Chad Weintraub, Ali Icel
GLOBALFOUNDRIES

5:40PM

P24

An Efficient Timing Analysis Model for 6T FinFET SRAM using Current-Based Method

Tiansong Cui[1], Ji Li[1], Alireza Shafaei Bejestan[1], Shahin Nazarian[1], Massoud Pedram[2]
[1]University of Southern California, [2]USC

SESSION 4A

Wednesday March 16

Powering IoT

Chair: **Stephen Heinrich-Barna**, Texas Instruments
Co-Chair: **Charles Augustine**, Intel

08:30AM
4A.1
Energy Harvesting and Power Management Opportunities in IOT
Harish Krishnamurthy, Jason Mix, Lilly Huang, Krishnan Ravichandran
Intel

08:50AM
4A.2
Linear, Point-of-Load Regulators for Fine-Grained Power Management of Digital Circuits
Saad Bin Nasir, Samantak Gangopadhyay, Arijit Raychowdhury
Georgia Institute of Technology

09:10AM
4A.3
Multi-Ratio Switched-Capacitor DC-DC Converters for Power Management Applications
Patrick Mercier and Loai Salem
University of California, San Diego

09:30AM
4A.4
Low-Power Circuit Techniques for IoT Energy Harvesting
Inhee Lee, Wanyeong Jung, Dennis Sylvester, David Blaauw
University of Michigan

SESSION 4B

Wednesday March 16

Enabling 5nm Technology Node

Chair: **Brian Cline**, ARM
Co-Chair: **Rajan Beera**, Pall Corporation

08:30AM
4B.1
Nanowire Transistor Solutions for 5nm and Beyond
Asen Asenov[1], Y Wang[2], B Cheng[1], X Wang[3], P Asenov[1], T Al-Ameri[3], V. P. Georgiev[3]
[1]Gold Standard Simulations, [2]Peking University, Beijing, [3]University of Glasgow

08:50AM
4B.2
5nm: Has the Time for a Device Change Come?
Praveen Raghavan, Marie Garcia Bardon, Pieter Schuddinck, Doyoung Jang, Dmitry Yakimets, Rogier Baert, Peter Debacker, Diederik Verkest, Aaron Thean
imec

09:10AM
4B.3
Transistor Design for 5nm and Beyond: Slowing Down Electrons to Speed Up Transistors
Victor Moroz[1], Joanne Huang[1], Reza Arghavani[2]
[1]Synopsys, [2]Lam Research

09:30AM
4B.4
Decomposition Technologies for Advanced Nodes
Fedor Pikus
Mentor Graphics, Inc

SESSION 4C

Wednesday March 16

Advanced Testing Concepts

Chair: **Vinod Viswanath**, Real Intent
Co-Chair: **Sreejit Chakravarty**, Intel

08:30AM
4C.1
Low Capture Power Dictionary based Test Data Compression
Panagiotis Sismanoglou and Dimitris Nikolos
University of Patras

08:50AM
4C.2
Analysis of Setup & Hold Margins Inside Silicon for Advanced Technology Nodes
Deepak Kumar Arora[1], Darayus Adil Patel[2], Shahabuddin Qureshi[1], Sanjay Kumar[1], Navin Kumar Dayani[1], Balwant Singh[1], Sylvie Naudet[1], Arnaud Virazel[3], Alberto Bosio[3]
[1]STMicroelectronics, [2]STMicroelectronics / LIRMM, [3]LIRMM

09:10AM
4C.3
Protocol-Guided Analysis of Post-silicon Traces Under Limited Observability
Hao Zheng[1], Yuting Cao[1], Sandip Ray[2], Jin Yang[2]
[1]University of South Florida, [2]Intel

09:30AM
4C.4
Nonlinear Delay-Table Approach for Full-Chip NBTI Degradation Prediction
Song Bian, Michihiro Shintani, Shumpei Morita, Masayuki Hiromoto, Takashi Sato
Kyoto University

SESSION T34

Wednesday March 16

Tutorial 3 & 4

Chair: **Hai (Helen) Li**, University of Pittsburgh
Co-Chair: **Vinod Viswanth**, Real Intent

10:10AM-11:00AM
T3
Low Power SoC System Design – A Systems Approach to Power Management Techniques, Power and Performance Optimizations, Thermal and Energy Management of Systems-on-Chip
Rajiv Muralidhar
Intel

11:00AM-11:50AM
T4
Building Neuromorphic Computing Systems with Emerging Device Technologies
John Strachan
Hewlett Packard Laboratories

SESSION 5A

Wednesday March 16

Embedded Systems

Chair: **Yang Yi**, University of Kansas
Co-Chair: **Rajesh Berigei**, Texas Instruments

1:00PM
5A.1
Reliability and Energy-aware Cache Reconfiguration for Embedded Systems
Yuanwen Huang and Prabhat Mishra
University of Florida

1:20PM
5A.2
Architecting STT Last-Level-Cache for Performance and Energy Improvement
Fazal Hameed[1] and Mehdi Tahoori[2]
[1]Chair of Dependable Nano Computing KIT - Karlsruhe Institute of Technology, [2]Karlsruhe Institute of Technology

1:40PM

5A.3

Instruction Cache Aging Mitigation Through Instruction Set Encoding

Anteneh Gebregiorgis[1], Fabian Oboril[1], Mehdi B. Tahoori[1], Said Hamdioui[2]

[1]Karlsruhe Institute of Technology, [2]Delft University of Technology

2:00PM

5A.4

Harvesting-aware Adaptive Energy Management in Solar-Powered Embedded Systems

Nga Dang[1], Zana Ghaderi[2], Eli Bozorgzadeh[3], Moonju Park[4]

[1]Google Inc., [2]University of California, Irvine, [3]Univ. of California, Irvine, [4]Incheon National University, South Korea

2:20PM

5A.5

Negotiation-Based Resource Provisioning and Task Scheduling Algorithm for Cloud Systems

Ji Li[1], Yanzhi Wang[2], Xue Lin[1], Shahin Nazarian[1], Massoud Pedram[3]

[1]University of Southern California, [2]Syracuse University, [3]USC

SESSION 5B

Wednesday March 16

Hardware and System Security

Chair: **Gang Qu**, Univeristy of Maryland

1:00PM

5B.1

Digital IP Protection Using Threshold Voltage Control

Joseph Davis, Niranjan Kulkarni, Jinghua Yang, Aykut Dengi, Sarma Vrudhula

Arizona State University

1:20PM

5B.2

Trojan Detection in Digital Systems Using Current Sensing of Pulse Propagation in Logic Gates

Sabyasachi Deyati[1], Abhijit Chatterjee[2], Barry Muldrey[1]

[1]Georgia Institute of Technology, [2]Georgia Tech

1:40PM

5B.3

Active Protection against PCB Physical Tampering

Steven Paley[1], Tamzidul Hoque[2], Swarup Bhunia[2]

[1]Case Western Reserve University, [2]University of Florida

5B.4

SVM-based Real-Time Hardware Trojan Detection for Many-Core Platform

Amey Kulkarni[1], Youngok Pino[2], Tinoosh Mohsenin[1]

[1]University of Maryland, Baltimore County, [2]Information Sciences Institute , University of Southern California

5B.5

On Testing Physically Unclonable Functions for Uniqueness

Arunkumar Vijayakumar[1], Vinay Patil[2], Sandip Kundu[1]

[1]Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, [2]Department of Electrical and Computer Engineering, University of Massachusetts Amherst

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SESSION 5C

Wednesday March 16

Analog Design

Chair: **Riaz Naseer**, Intel
Co-Chair: **Stephen Heinrich-Barna**, Texas Instruments

5C.1

Neuromorphic Computing with Resistive Synaptic Arrays: Devices, Circuits and Systems

Yu Cao[1], Shimeng Yu[1], Yu Wang[2], Pai-Yu Chen[1], Lixue Xia[2], Huazhong Yang[2]

[1]Arizona State University, [2]Tsinghua University

5C.2

Dot-Product Engine as Computing Memory to Accelerate Machine Learning Algorithms

Miao Hu, John Paul Strachan, Zhiyong Li, R. Stanley Williams

Hewlett Packard Labs

5C.3

0.5-V 50-mV-Swing 1.2-GHz 28-nm-FD-SOI 32-bit Dynamic Bus Architecture with Dummy Bus

Khaja Ahmad Shaik, Kiyoo Itoh, Amara Amara

Institut supérieur d'électronique de Paris (ISEP)

5C.4

Analysis and Design of a Triangular Active Charge Injection for Stabilizing Resonant Power Supply Noise

Masahiro Kano, Toru Nakura, Kunihiro Asada
The University of Tokyo

2:20PM
5C.5
An Ultra-fast and Low-power Design of Analog Circuit Network for DoG Pyramid Construction of SIFT Algorithm
Zheyu Liu, Fei Qiao, Qi Wei, Xinghua Yang, Yi Li, Huazhong Yang
Dept.of Electronic Engineering, Tsinghua University

SESSION 6A

Wednesday March 16

Design Optimization for Performance, Reliability, and Yield

Chair: **Fedor Pikus**, Mentor Graphics
Co-Chair: **Vivek Joshi**, GlobalFoundries

3:00PM
6A.1
Impact of Interconnect Variability on Circuit Performance in Advanced Technology Nodes
Divya Madapusi Srinivas Prasad, Chenyun Pan, Azad Naeemi
Georgia Institute of Technology

3:20PM
6A.2
Hotspot Detection Using Machine Learning
Kareem Madkour[1], Sarah Mohamed[1], Dina Tantawy[2], Mohab Anis[3]
[1]Mentor Graphics, [2]Cairo Univeristy, [3]American University in Cairo

3:40PM
6A.3
Efficient Analog Circuit Optimization Using Sparse Regression and Error Margining
Mohamed Baker Alawieh[1], Fa Wang[2], Rouwaida Kanj[1], Xin Li[2], Rajiv Joshi[3]
[1]American University of Beirut, [2]Carnegie Mellon University, [3]IBM

4:00PM
6A.4
State Encoding Based NBTI Optimization in Finite State Machines
Shilpa Pendyala and Srinivas Katkoori
University of South Florida Tampa

SESSION 6B

Wednesday March 16

EDA for Design Exploration & Analysis Beyond Moore's Law

Chair: **Takashi Sato**, Kyoto University
Co-Chair: **Ofelya Manukyan**, Synopsys

3:00PM
6B.1
Gate Movement for Timing Improvement on Row Based Dual-VDD Designs
Hua Xiang, Lakshmi Reddy, Haifeng Qian, Ching Zhou, Yu-Shiang Lin, Fanchieh Yee, Andrew Sullivan, Pong-Fei Lu
IBM Research

3:20PM
6B.2
Multiple Shift-vector Importance Sampling Method using Support Vector Machine and Clustering for High-Density DRAM Designs
Jinyoung Lee, Sunghee Yun, Jeongha Kim, Dongsoo Kang, Jeongyeol Kim, Sanghoon Lee
Samsung Electronics

3:40PM
6B.3
Fully Automated PLL Compiler Generating Final GDS from Specification
Toru Nakura and Kunihiro Asada
The University of Tokyo

4:00PM
6B.4
AFD-Based Method for Signal Line EM Reliability Evaluation
Zhong Guan[1] and Malgorzata Marek-Sadowska[2]
[1]UC Santa Barbara, ECE department, [2]University of California, Santa Barbara

SESSION 6C

Wednesday March 16

Sensors for IOT

Chair: **Kamesh Gadepally**, GigaCom Semiconductor
Co-Chair: **Charles Augustine**, Intel

3:00PM
6C.1
A Smart ECG Sensor with In-Situ Adaptive Motion-Artifact Compensation for Dry-Contact Wearable Healthcare Devices
Shuang Zhu, Jingyi Song, Balaji Chellappa, Ali Enteshari, Tuo Shan, Mengxun He, Yun Chiu
University of Texas at Dallas

3:20PM
6C.2
Making Unreliable Chem-FET Sensors Smart via Soft Calibration
Fatih Karabacak[1], Uwadiae Obahiagbon[1], Umit Ogras[1], Sule Ozev[2], Jennifer Blain Christen[1]
[1]Arizona State University, [2]ASU

3:40PM
6C.3
Novel design of a silicon photodetector and its integration in a 4×4 CMOS pixel array
Hari Shanker Gupta[1], Satyajit Mohapatra[2], Nihar R. Mohapatra[2], D K Sharma[3]
[1]Space Applications Centre, [2]Department of Electrical Engineering, Indian Institute of Technology, Gandhinagar, Ahmedabad, India, [3]Department of Electrical Engineering, Indian Institute of Technology, Bombay, Mumbai, India

4:00PM
6C.4
Time-Division Multiple Access Based Intra-body Communication for Wearable Health Tracker
Tan Chee Phang[1], Mohammad Harris Mokhtar[2], Mohd Nazim Mohtar[1], fakhrul zaman rokhani[1]
[1]University Putra Malaysia, [2]Telecom Research