# Final Program

# ISQED

## 2022
## 23rd International Symposium on

# QUALITY ELECTRONIC DESIGN

AI/ML & Electronic Design. Autonomous Vehicles. Security.
IoT. Quantum Computing.

**April 6-7, 2022**
**Virtual Conference**
**California Pacific Daytime**
**San Jose, CA USA**



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ISQED

www.ISQED.com

ISQED'22 is produced and sponsored by the
**International Society for Quality Electronic Design**

# WELCOME TO ISQED'22

On behalf of the ISQED conference and technical committees, we are pleased to welcome you to the 23nd anniversary of the International Symposium on Quality Electronic Design, ISQED'22.

For the past 23 years, ISQED has been the leading voice and pioneer in Quality Electronic Design (QED). With the drastic increase in complexity of semiconductor technology and design, following QED and its underlying principles are becoming more necessary and essential as never before. ISQED'22 strives to lead the community in that direction with a comprehensive program consisting of keynotes, panel, tutorials, and over 100 peer-reviewed articles.

The conference is conducted in a virtual format this year, with the technical sponsorship of the IEEE Electron Devices Society, the IEEE Circuits and Systems Society, IEEE Reliability Society, and in-cooperation with ACM/SigDA. Conference proceedings & papers will be published in IEEE Xplore digital library and indexed by Scopus.

ISQED'22 is organized around the important trends in AI/ML, Autonomous Vehicles, Security, IoT, and Quantum Computing. The conference program consists of two keynote talks, two embedded tutorials, a panel discussion, and many peer-reviewed technical papers with focus on these timely and hot topics.

We are pleased to see the number of quality papers submitted to the conference this year. The two-day technical program with four parallel sessions packs over 90 peer-reviewed papers highlighting the latest trends in electronic circuit and system design & automation, testing, verification, sensors, security, semiconductor technologies, cyber-physical systems, etc.

All technical presentations, plenary sessions, panel discussions, tutorials and related events will take place on April 6-7, conducted virtually, at Pacific Daylight Time (PDT).

We would like to thank the ISQED'22 corporate sponsors: Synopsys, Siemens EDA, and Innovotek for their valuable financial support of this conference. Welcome to another exciting year of ISQED and thanks for your support and participation.

# ISQED'22 Best Papers

**1A.1**

## Hybrid Learning for Orchestrating Deep Learning Inference in Multi-user Edge-cloud Networks

*Sina Shahhosseini[1], Tianyi Hu[1], Dongjoo Seo1, Anil Kanduri[2], Bryan Donyanavard[3], Amir M. Rahmani1, Nikil Dutt[1]*

**[1] University of California, Irvine, [2] University of Turku, Finland, [3] San Diego State University**

**3A.1**

## A Parallel SystemC Virtual Platform for Neuromorphic Architectures

*Melvin Galicia, Farhad Merchant and Rainer Leupers*

**Institute for Communication Technologies and Embedded Systems**

**RWTH Aachen University, Aachen, Germany**

Authors of best papers are acknowledged during the morning plenary session on Wednesday April 6.

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## GENERAL INFORMATION
## ISQED'22

*April 6-7, 2022*
*Virtual Event*
*Pacific Daylight Time (PDT)*

## AWARDS & RECOGNITIONS

*Wednesday April 6, 9:00 AM - 9:20 AM*
**Track A**

### Best Paper Awards

Recipients of the ISQED'22 Best Paper Awards will be recognized in this segment of the program. The best papers are shown in Page 2 of this document.

## Keynotes

*Wednesday, April 6, 9:20 AM - 9:55 AM*
**Track A**

### Guaranteeing Accuracy with Machine Learning

**Jeff Dyck**
Senior Director of Engineering
**Siemens EDA**

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*Thursday April 7, 9:00 AM - 9:35 AM*
**Track A**

### Superconductive Quantum Circuits for Energy Efficient Cloud Computing

**Prof. Eby G. Friedman**
**University of Rochester**

.....

## Panel Discussion

*Wednesday, April 6, 2:35 PM - 4:05 PM*
**Track A**

### VLSI Technology in Health Care - Externally Worn Devices to monitor, store and transmit

Healthy life is the most important all of us. Due to COVID pandemic, we certainly realized this importance and started taking our health more seriously how to monitor and control our health conditions in the ordinary daily life. One important factors, now adays, is not going to the clinics or hospitals, the monitoring and the self-diagnosing at the personal wearable devices remotely. In this panel session, the bi-osensing experts in the healthcare filed get together and will discuss about the current health sensing/monitoring technology and their business situation with focus on bio-sensing device on VLSI technologies, like what bio-sensing devices are available, how to combine with Si-base VLSI technologies, what is a gap what we're seeing now and how modern circuitry in biomedical devices is changing and where are we headed for the future.

***Panelists:***
**Shintaro Izumi -** Kobe University
**Arindam Sanyal -** Arizona State University
**Aveek Sarkar -** Synopsys
**Ali Kabiri -** *Rockley Photonics*

***Moderator:***
**Alodeep Sanyal -** LifePlus

***Chairs:***
**Shigeki Tomishima -** Intel Corporation (Chair)
**Siddha Ganju -** Nvidia (Co-Chair)

## Embedded Tutorials

***Chair & Moderators:***
**José Pineda de Gyvez -** NXP Semiconductors (Chair)
**Yu Pu -** Alibaba (Co-Chair)

**Track A**

**Tutorial 1**

*Wednesday, April 6, 11:35 AM - 12:35 PM*

**Neuromorphic processing at the sensor edge: Engineering tiny brain**

**Amir Zjajo**
Innatera Nanosystems

**Tutorial 2**

*Thursday April 7, 1:05 PM - 2:05 PM*

**Analog, Mixed Signal and Power Integrated Circuits (ICs) - Automotive Applications and Testing Methodology for Quality**

**Sri Navaneeth Easwaran**
Texas Instruments Inc, Dallas, TX, USA

### TECHNICAL SESSIONS

There are a total of 20 paper sessions held on Wednesday to Friday. Technical sessions are held in the format of four parallel virtual tracks **A, B, C,** and **D**.

# PROGRAM AT A GLANCE

## WEDNESDAY APRIL 6

Please note all shown times are Pacific Daylight Time (PDT)

| | | | | |
|---|---|---|---|---|
| 9:00am–9:55am | **Plenary Session 1:** | | | |
| 9:00am–9:20am | **Introduction, Awards, and Recognitions**<br>**Best Paper Awards** | | | |
| 9:20am–9:55am | **Keynote:**<br>**Guaranteeing Accuracy with Machine Learning**<br>**Jeff Dyck - *Senior Director of Engineering, Siemens EDA*** | | | |
| 9:55am-10:05am | **Break** | | | |
| 10:05am–11:25am | **Session 1A**<br>**Efficient Deep Learning System Design** | **Session 1B**<br>**Modeling and Simulation Methodologies in Electronic Designs** | **Session 1C**<br>**Testing and Formal Verification of Circuits** | **Session 1D**<br>**Recent Advances in Hardware-Assisted Security** |
| 11:25am-11:35am | **Break** | | | |
| 11:35am-12:35pm | **Embedded Tutorial 1**<br>**Neuromorphic processing at the sensor edge: Engineering tiny brain**<br>*Presenter:*<br>**Dr. Amir Zjajo - *Chief Scientist and co-founder at Innatera Nanosystems*** | | | |
| 12:35pm-12:45pm | **Break** | | | |
| 12:45pm-2:25pm | **Session 2A**<br>**Design & Automation for Low-power Real-time System** | **Session 2B**<br>**Estimation and Optimization Methodologies in VLSI Designs** | **Session 2C**<br>**Novel AI Computing Architecture** | **Session 2D**<br>**Smart sensing in Internet of Things (IoT)** |
| 2:30pm-2:35pm | **Break** | | | |
| 2:35pm-4:05pm | **Panel Discussion**<br>**VLSI Technology in Health Care - Externally Worn Devices to monitor, store and transmit**<br>*Panelists:*<br>**Shintaro Izumi, Arindam Sanyal, Aveek Sarkar, Ali Kabiri** | | | |

# PROGRAM AT A GLANCE

## THURSDAY APRIL 7

Please note all shown times are Pacific Daylight Time (PDT)

| | | | | |
|---|---|---|---|---|
| 8:50am–9:35am | **Plenary Session 2:** | | | |
| 8:50am-9:00am | **Welcome** | | | |
| 9:00am-9:35am | **Keynote:**<br>**Superconductive Quantum Circuits for Energy Efficient Cloud Computing**<br>**Prof. Eby G. Friedman - *University of Rochester*** | | | |
| 9:35am-9:45am | **Break** | | | |
| 9:45am-11:05am | **Session PW1**<br>**Poster & WIP Session 1** | **Session PW2**<br>**Poster & WIP Session 2** | **Session 3DIC**<br>**Approximate Computing & Monolithic 3D ICs** | **Session 3SS**<br>**Intelligent Internet of Battery-less Things** |
| 11:05am-11:15am | **Break** | | | |
| 11:15am-12:55pm | **Session 3A**<br>**Acceleration and Efficiency of Computation and Storage** | **Session 3B**<br>**AI Accelerator Hardware Design** | **Session 3C**<br>**Keep the Chip Secrets Safe: Side-channel Attacks and Defenses** | **Session 3D**<br>**Advanced 2.5D and 3D Heterogeneous Integration for State-of-the-Art Computing** |
| 12:55pm-1:05pm | **Break** | | | |
| 1:05pm-2:05pm | **Embedded Tutorial 2**<br>**Analog, Mixed Signal and Power Integrated Circuits (ICs) for automotive applications and testing methodology for quality**<br>*Presenter:*<br>**Dr. Navaneeth Easwaran - *Texas Instruments***<br>**Dr. Robert Weigel - *University of Erlangen-Nuremberg, Erlangen, Germany*** | | | |
| 2:05pm-2:15pm | **Break** | | | |
| 2:15pm-3:55pm | **Session 4A**<br>**Machine Learning Systems towards Practical Applications** | **Session 4B**<br>**Physical Implementation Considerations in VLSI Designs** | **Session 4C**<br>**Physical Attacks on PUFs and Secure Hardware Design** | **Session 4D**<br>**Approximate Computing: From Circuit Design to System Integration** |

Wednesday April 6

*9:20 AM - 9:55 AM*

Track A

# Guaranteeing Accuracy with Machine Learning

**Jeff Dyck**

***Senior Director of Engineering, Siemens EDA***

Machine learning methods are effective at cutting down verification runtimes and increasing coverage - it is common to see 2X-1000X improvements in these areas. In practice, these speedups are often too good to be true, as they come with questionable accuracy, where they can give incorrect answers without being able to tell. These fast, but inaccurate verification methods are not suitable for verifying engineering designs, and end up being no more than cool demos, with no practical application. This talk reviews a suite of proven techniques used in Solido's verification tools for meeting specific accuracy criteria and proving that the answer is correct, while still delivering big machine learning speedups.

**About Jeff Dyck**

Jeff Dyck is Senior Director of Engineering at Siemens EDA, responsible for R&D for three software product lines in the integrated circuit verification solutions (ICVS) division. Prior to joining Siemens, Jeff was VP of Engineering at Solido Design Automation, where he led Solido's R&D teams, managed Solido's product lines, and co-invented Solido's machine learning technologies. Solido was acquired by Siemens in 2017. Jeff is now working on evolving the active learning technology in Solido's products, as well as developing new disruptively differentiated tools within the Siemens EDA analog mixed signal product line.

Thursday April 7

*9:00 AM - 9:35 AM*

Track A

# Superconductive Quantum Circuits for Energy Efficient Cloud Computing

**Prof. Eby G. Friedman**

***University of Rochester***

The scaling of semiconductor CMOS technology is now approaching fundamental physical limitations, encouraging the development of novel beyond-CMOS emerging technologies to supplement existing electronic systems. One rapidly growing application area for these beyond-CMOS circuits is energy efficient, large scale stationary computing – data centers and supercomputers. A particularly appropriate technology for this important application is superconductive electronics; in particular, single flux quantum (SFQ) circuits - the most widely adopted superconductive digital logic family. This technology exhibits speeds in the tens to hundreds of gigahertz while dissipating 100 to 1000X less power than CMOS. The fabrication capabilities of modern superconductive foundries currently approach a million logic gates per integrated circuit. Algorithms and methodologies aware of the issues posed by the large scale integration of SFQ circuits are topics of great currency. In this lecture, superconductive electronic circuits are introduced, and issues and solutions to enable the large scale integration of complex SFQ integrated circuits and systems are presented. Particular emphasis is placed on the many challenges faced by modern superconductive logic circuits and large scale digital systems. Among these issues are compact and efficient cryogenic memory, synchronization of sub-terahertz digital systems, interconnect routing, energy efficient current bias networks, and design for testability. Single flux quantum circuits are capable of transforming large scale computing systems - an increasingly important application due to the movement of data storage and processing onto remote cloud servers. Models, circuits, algorithms, and design methodologies to enable the development of next generation, large scale SFQ systems are the primary topics of this presentation.

## About Eby G. Friedman

Eby G. Friedman received the B.S. degree in electrical engineering from Lafayette College and the M.S. and Ph.D. degrees in electrical engineering from the University of California at Irvine. He was with Hughes Aircraft Company from 1979 to 1991, rising to Manager of the Signal Processing Design and Test Department, where he was responsible for the design and test of high performance digital and analog ICs. He has been with the Department of Electrical and Computer Engineering, University of Rochester since 1991, where he is a Distinguished Professor and the Director of the High Performance VLSI/IC Design and Analysis Laboratory. He is also a Visiting Professor with the Technion — Israel Institute of Technology. He has authored almost 600 papers and book chapters, 24 patents, and authored or edited 19 books in the fields of high speed and low power CMOS design techniques, 3-D design methodologies, high speed interconnect, superconductive circuits, and the theory and application of synchronous clock and power distribution networks. His current research and teaching interests include high performance synchronous digital and mixed-signal circuit design and analysis with application to high speed portable processors, low power wireless communications, and server farms. Dr. Friedman is a recipient of the IEEE Circuits and Systems Mac Van Valkenburg Award, the IEEE Circuits and Systems Charles A. Desoer Technical Achievement Award, the University of Rochester Graduate Teaching Award, and the College of Engineering Teaching Excellence Award. He was the Editor-in-Chief and Chair of the steering committee of the IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Editor-in-Chief of the Microelectronics Journal, Regional Editor of the Journal of Circuits, Systems and Computers, an editorial board member of numerous journals, and a program and technical chair of several IEEE conferences. He is an IEEE Fellow, Senior Fulbright Fellow, National Sun Yat-sen University Honorary Chair Professor, and an inaugural member of the UC Irvine Engineering Hall of Fame.

Wednesday April 6

*2:35 PM–4:05 PM*
Track A

# VLSI Technology in Health Care - Externally Worn Devices to Monitor, Store and Transmit

**Panel Committee:**
**Shigeki Tomishima -** Intel Corporation (Chair)
**Siddha Ganju -** Nvidia (Co-Chair)

**Summary**:
Healthy life is the most important all of us. Due to COVID pandemic, we certainly realized this importance and started taking our health more seriously how to monitor and control our health conditions in the ordinary daily life. One important factors, now adays, is not going to the clinics or hospitals, the monitoring and the self-diagnosing at the personal wearable devices remotely. In this panel session, the biosensing experts in the healthcare filed get together and will discuss about the current health sensing/monitoring technology and their business situation with focus on biosensing device on VLSI technologies, like what bio-sensing devices are available, how to combine with Si-base VLSI technologies, what is a gap what we're seeing now and how modern circuitry in biomedical devices is changing and where are we headed for the future.

**Panelists:**
**Shintaro Izumi -** Kobe University
**Arindam Sanyal -** Arizona State University
**Aveek Sarkar -** Synopsys
**Ali Kabiri -** Rockley Photonics

**Modedrator:**
**Alodeep Sanyal -** LifePlus

Wednesday April 6

*11:35 AM - 12:35 PM*
Track A

# Neuromorphic Processing at the Sensor Edge: Engineering Tiny Brain

**Amir Zjajo**
***Innatera Nanosystems***

**Summary:**
Brain-inspired, neuromorphic spiking neural network emulators form distributed, parallel, and event-driven system offering signal transmission energy-efficiency, and intelligence or inference capabilities to resource-constrained devices. Computational elements of the reconfigurable neuromorphic networks, typically, only partially include dendritic, and subsequently, synaptic properties. However, increased experimental evidence indicates the existence of a large diversity of dendritic channels, which modify synaptic response by amplification, regulation, the dendritic structure scaling, etc. We abstract the fundamental dendritic functions by extracting the underlying dynamics governed by bio-chemical processes; this increase in dimensionality allows more states and transitions (and time constants), offering more flexibility in the implementation of plastic and metaplastic interactions, i.e. providing mechanism to realize and maintain robust neural computation, in addition to enhancing specifics of the sensory signal processing, e.g. accentuate changes in stimulus parameters, prevent spiking frequency saturation, tune frequency responses to specific stimulus features. In this tutorial, we address several important questions such as i) how do we leverage all the advantages of dendritic bio-chemical signal processing at different levels of time-granularity or hierarchy, and ii) how the main principles of a tiny-brain translate to competitive (sub-pJ level synaptic operation) neuromorphic hardware platforms, and software/hardware co-alignment in terms of distributed processing, technological variability, and neural network definitions and mapping. Enabling such paradigms and concepts open in-roads towards several high-potential use-cases geared specifically towards processing incoming data in an always-on, event-driven fashion facilitating truly smart-sensing and energy-optimized sensor systems.

**About Amir Zjajo**
Amir Zjajo is co-founder of Innatera Nanosystems B.V., and serves as its Chief Scientist. Prior to that, he was a member of research staff in the Mixed Signal Circuits and Systems Group at Philips Research Laboratories between 2000 and 2006, and subsequently, with Corporate Research at NXP Semiconductors until 2009. He joined the Delft University of Technology the same year, and was responsible for leading research into intelligent systems within a range of EU-funded research projects. Dr. Zjajo has authored 3 books, and published more than 90 papers in referenced journals and conference proceedings in the areas of mixed-signal VLSI design, and neuromorphic circuits and systems. He received the M.Sc. and DIC degrees from the Imperial College London, London, U.K., in 2000, and the PhD. degree from Eindhoven University of Technology, Eindhoven, The Netherlands in 2010, all in electrical engineering. His research interests include energy-efficient circuit and system design for on-chip machine learning and inference, and bionic electronic circuits for autonomous cognitive systems. Dr. Zjajo won best/excellence paper award at BioDevices'15 and LifeTech'19. He is a senior member of IEEE.

Thursday April 7

*1:05 PM - 2:05 PM*

Track A

# Analog, Mixed Signal and Power Integrated Circuits (ICs) - Automotive Applications and Testing Methodology for Quality

**Sri Navaneeth Easwaran**

*Texas Instruments Inc, Dallas, TX, USA*

**Summary**:
Power transistors form the main component of automotive Integrated Circuits (ICs) and they handle several amperes of current (>2A). State of the Art is to integrate several power MOSFETs along with their gate drivers (including charge pumps or boost converters that supply the gate drivers) whose operating voltage range is from 5V to 60V. Reliability of these integrated gate drivers and power transistors is a key factor to meet the high-quality demands of the automotive applications. In this tutorial, challenges related to the design and reliability of circuits like LDOs, High Side (HS) drivers, Low Side (LS) drivers and configurable HS/ LS drivers are discussed along with information related to floating nodes, aging and reliability related concerns like NBTI/PBTI, HCI etc. and proven design techniques to simulate and mitigate these challenges. These gate drivers have to be thoroughly designed for robustness w.r.to. Electrical and Thermal Safe Operating Area (SOA) and its test methodology by shorting the outputs to ground and battery will be discussed. In this tutorial, Design FMEA (Failure Mode Effect Analysis) based analysis to mitigate risks at design and system level along with test concepts towards very low dppm (defective parts per million) will be discussed. This tutorial will be valuable for the design, product and test engineers developing ICs for automotive and industrial applications

.**About Sri Navaneeth Easwaran**
Dr. –Ing. Sri Navaneeth Easwaran, Senior Member IEEE, received his Bachelor's (1998, Bharathidasan University), Master's (2006, University Twente) degrees in Electrical Engineering and Dr. –Ing. degree from University of Erlangen-Nuremberg in 2017. He worked at SPIC Electronics, STMicroelectronics, Philips Semiconductors between 1998 and 2006. From 2006 he is with Texas Instruments (TI) where he was the design lead of airbag squib driver ICs. and System Basis Chips. He is an IET Fellow (Feb 2021), TI Senior Member Technical Staff, has 20+ granted patents and 14 publications. He has offered tutorials on automotive ICs at IEEE Conferences. Since Dec 2020, he is offering iDLP (Industrial Distinguished Lecturer Program) CASS seminars on smart automotive circuits.

# SESSION 1A

## Wednesday April 6

## Efficient Deep Learning System Design

Chair: **Cong Hao**, Georgia Institute of Technology
Co-Chair: **Bo Yuan**, Rutgers University

*10:05AM*
**1A.1**
93 **Hybrid Learning for Orchestrating Deep Learning Inference in Multi-user Edge-cloud Networks**
*Sina Shahhosseini[1], Tianyi Hu[1], Dongjoo Seo[1], Anil Kanduri[2], Bryan Donyanavard[3], Amir M. Rahmani[1], Nikil Dutt[4]*
[1]University of California, Irvine, [2]University of Turku, [3]San Diego State University, [4]UC Irvine

*10:25AM*
**1A.2**
56 **X-NVDLA: Runtime Accuracy Configurable NVDLA based on Employing Voltage Overscaling Approach**
*Hassan Afzali-Kusha and Massoud Pedram*
USC

*10:45AM*
**1A.3**
76 **Analysis of the Effect of Off-chip Memory Access on the Performance of an NPU System**
*Keonjoo Lee, Donghyun Kang, Duseok Kang, Soonhoi Ha*
Seoul National University

*11:05AM*
**1A.4**
143 **Design and Challenges of Embedded AI on Front End Electronics for HEP Applications**
*Sandeep Miryala[1] and Srinivas Katkoori[2]*
[1]Brookhaven National Laboratory, [2]University of South Florida

# SESSION 1B

## Wednesday April 6

## Modeling and Simulation Methodologies in Electronic Designs

Chair: **Srini Krishnamoorthy**, Intel Corp.
Co-Chair: **Rui Zhang**, Cadence

*10:05AM*
**1B.1**
2 **Low-IR-Drop Test Pattern Regeneration Using A Fast Predictor**
*Shi-Tang Liu[1], Jia-Xian Chen[1], Yu-Tsung Wu[1], Chao-Ho Hsieh[1], Ying-Shiun Li[2], Wen-Tze Chuang[2], Norman Chang[2], Chien-Mo Li[1]*
[1]National Taiwan University, [2]Ansys

*10:25AM*
**1B.2**
33 **Simulation methodology for timing analysis and design optimization in digital Superconducting Electronics**
*Sam Lo, Aaron Barker, Stephen Whiteley, Eric Mlinar, Jiajun Chen, Dehuang Wu, Kishore Singhal*
Synopsys

*10:45AM*
**1B.3**
34 **Functional Level Abstraction and Simulation of Verilog-AMS Piecewise Linear Models**
*SADIA AZAM[1], Nicola Dall'Ora[2], Enrico Fraccaroli[3], Franco Fummi[4]*
[1]University of Verona ,italy, [2]University of Verona, [3]Università degli Studi di Verona, [4]Universita' di Verona

*11:05AM*
**1B.4**
45 **Predicting Post Route Quality of Results Estimates for HLS Designs using Machine Learning**
*Pingakshya Goswami and Dinesh Bhatia*
University of Texas at Dallas

# SESSION 1C

## Wednesday April 6

## Testing and Formal Verification of Circuits

Chair: **Deepashree Sengupta**, Synopsys Inc.
Co-Chair: **Miroslav Velev**, Aries Design Automation

*10:05AM*
**1C.1**
**Investigation on Realistic Stuck-on/off Defects to Complement IEEE P2427 Draft Standard**
10 *SADIA AZAM[1], Nicola Dall'Ora[2], Enrico Fraccaroli[3], André Alberts[4], Renaud Gillon[5], Franco Fummi[6]*
[1]University of Verona ,italy, [2]University of Verona, [3]Università degli Studi di Verona, [4]Sydelity B.V., Kruisem, Belgium, [5]Sydelity B.V., Kruisem, Belgium, [6]Universita' di Verona

*10:25AM*
**1C.2**
24 **Formal Analysis of Integer Multipliers by building Binary Decision Diagram of Adder Trees**
*Jitendra Kumar[1], Asutosh Srivastava[1], Masahiro Fujita[2]*
[1]Jawaharlal Nehru University, [2]University of Tokyo

*10:45AM*
**1C.3**
78 **DEEQ: Data-driven End-to-End EQuivalence Checking of High-level Synthesis**
*Mohammed Abderehman, Chandan Karfa, Rakesh Reddy*
Indian Institute Of Technology–Guwahati

*11:05AM*
**1C.4**
69 **Transaction Level Stimulus Optimization in Functional Verification Using Machine Learning Predictors**
*Saumil Gogri, Aakash Tyagi, Mike Quinn, Jiang Hu*
Texas A&M University

# SESSION 1D

## Wednesday April 6

### Recent Advances in Hardware-Assisted Security

Chair: **Hossein Sayadi**, California State University, Long Beach

*10:05AM*
**1D.1**
116 **Accelerated Machine Learning for On-Device Hardware-Assisted Cybersecurity in Edge Platforms**
*Hosein Mohammadi Makrani[1], Zhangying He[2], Setareh Rafatirad[1], Hossein Sayadi[2]*
[1]University of California, Davis, [2]California State University, Long Beach

*10:25AM*
**1D.2**
128 **Does Aging Matter? The Curious Case of Fault Sensitivity Analysis**
*Mohammad Ebrahimabadi[1], Bijan Fadaeinia[2], Amir Moradi[2], Naghmeh Karimi[1]*
[1]University of Maryland Baltimore County, [2]Ruhr University Bochum

*10:45AM*
**1D.3**
132 **Challenges and Opportunities for Hardware-Assisted Security Improvements in the Field**
*Benjamin Tan*
University of Calgary

*11:05AM*
**1D.4**
145 **Adaptive-Gravity: A Defense Against Adversarial Samples**
*Ali Mirzaeian[1], Zhi Tian[1], Sai Manoj P D[1], Banafsheh Saber Latibari[2], Ioannis Savidis[3], Houman Homayoun[2], Avesta Sasan[2]*
[1]George Mason University, [2]University of California, Davis, [3]Drexel University

# SESSION 2A

## Wednesday April 6

### Design & Automation for Low-power Real-time System

Chair: **Yu Bai**, California State University Fullerton
Co-Chair: **Shiyan Hu**, University of Southampton

*12:45PM*
**2A.1**
83 **An Efficient Error Estimation Technique for Pruning Approximate Data-Flow Graphs in Design Space Exploration**
*Marzieh Vaeztourshizi and Massoud Pedram*
USC

*1:05PM*
**2A.2**
95 **A Heterogeneous Solution to the All-pairs Shortest Path Problem using FPGAs**
*Mihnea Chirila[1], Paolo D'Alberto[2], Hsin-Yu Ting[1], Alexander Veidenbaum[1], Alexandru Nicolau[1]*
[1]University of California, Irvine, [2]Xilinx Inc.

*1:25PM*
**2A.3**
19 **Integrated Power Delivery Methodology for 3D ICs**
*Yousef Safari and Boris Vaisband*
McGill University

*1:45PM*
**2A.4**
7 **FastMem: A Fast Architecture-aware Memory Layout Design**
*Alok Parmar[1], Kailash Prasad[2], Nanditha Rao[1], Joycee Mekie[2]*
[1]International Institute of Information Technology, Bangalore, [2]Indian Institute of Technology, Gandhinagar

# SESSION 2B

## Wednesday April 6

## Estimation and Optimization Methodologies in VLSI Designs

Chair: **Siddhartha Nath**, Nvidia
Co-Chair: **Emre Salman**, Stony Brook University

*12:45PM*
**2B.1**

47 **Reinforcement-Learning-based Mixed-Signal IC Placement for Fogging Effect Control**
*Mohammad Hajijafari, Mehrnaz Ahmadi, Zhenxin Zhao, Lihong Zhang*
Memorial University of Newfoundland

*1:05PM*
**2B.2**

57 **Routability-driven Global Routing with 3D Congestion Estimation Using a Customized Neural Network**
*Yuxuan Pan, Zhonghua Zhou, Andre Ivanov*
the University of British Columbia

*1:25PM*
**2B.3**

58 **Model Auto Extraction for Gate-All-Around Silicon Nanowire MOSFETs Using A Decomposition-Based Many-Objective Evolutionary Algorithm**
*Ya-Shu Yang[1] and Yiming Li[2]*
[1]National Yang Ming Chiao Tung University, [2]National Chiao Tung University

*1:45PM*

**2B.4**

**Building Post-layout Performance Model of Analog/RF Circuits by Fine-tuning Technique**

70 *Zhikai Wang[1], Wenfei Hu[1], Jingbo Zhou[2], Wenyuan Zhang[3], Ruitao Wang[4], Jian ZHang[5], Dejing Dou[6], Zuochang Ye[5], Yan Wang[7]*

[1]School of Integrated Circuits, Tsinghua University, [2]Baidu Research, Business Intelligence Lab, [3]Beijing Institute of Technology, [4]Shool of Integrated Circuits, Tsinghua University, [5]School of Integrated Circuits, Tsinghua university, [6]Big Data Lab, Baidu Research, [7]School of Integrated Circuits, Tsinghua University

*2:05PM*

**2B.5**

79 **On Predicting Solution Quality of Maze Routing Using Convolutional Neural Network**

*Kuei-Huan Chang[1], Hsin-Hung Pan[1], Ting-Chi Wang[1], Po-Yuan Chen[2], Chin-Fang Shen[2]*

[1]National Tsing Hua University, [2]Synopsys Taiwan Co., Ltd.

# SESSION 2C

## Wednesday April 6

## Novel AI computing architecture

Chair: **Shaahin Angizi**, New Jersey Institute of Technology
Co-Chair: **Arman Roohi**, University of Nebraska Lincoln

*12:45PM*
**2C.1**
25 **Beta Oscillation Detector Design for Closed-Loop Deep Brain Stimulation of Parkinson's Disease with Memristive Spiking Neural Networks**
*Zachary Kerman, Chunxiu Yu, Hongyu An*
Michigan Technological University

*1:05PM*
**2C.2**
94 **Memristor-based Deep Spiking Neural Network with a Computing-In-Memory Architecture**
*Fabiha Nowshin and Cindy Yang Yi*
Virginia Tech

*1:25PM*
**2C.3**
28 **LogGen: A Parameterized Generator for Designing Floating-Point Logarithm Units for Deep Learning**
*Pragnesh Patel, Aman Arora, Earl Swartzlander, Lizy John*
University of Texas at Austin

*1:45PM*
**2C.4**
135 **Cross-layer Designs against Non-ideal Effects in ReRAM-based Processing-in-Memory System**
*Chen Nie[1], Zongwu Wang[2], Qidong Tang[2], Chenyang Lv[2], Li Jiang[1], Zhezhi He[3]*
[1]Shanghai Jiao Tong University, [2]Shanghai Jiaotong University, [3]Department of Computer Science and Engineering, Shanghai Jiao Tong University

# SESSION 2D

## Wednesday April 6

## Smart Sensing in Internet of Things (IoT)

Chair: **Prabha Sundaravadivel**, University of Texas at Tyler
Co-Chair: **Shawana Tabassum**, University of Texas at Tyler

*12:45PM*
**2D.1**

123 **An IoT-enabled Electronic Textile-based Flexible Body Sensor Network for Real-time Health Monitoring in Assisted Living during Pandemic**
*Nafize Ishtiaque Hossain and Shawana Tabassum*
The University of Texas at Tyler

*1:05PM*
**2D.2**

124 **EasyBand2.0: A Framework with Context-Aware Recommendation Mechanism for Safety-Aware Mobility during Pandemic Outbreaks**
*Seema G. Aarella[1], Ajaya K. Tripathy[2], Saraju Mohanty[3], Elias Kougianos[4]*
[1]Department of Computer Science, University of North Texas, USA., [2]School of Computer Science, Gangadhar Meher University, India., [3]University of North Texas, [4]Department of Electrical Engineering, University of North Texas, USA.

*1:25PM*
**2D.3**

133 **i-lete: An IoT-based physical stress monitoring framework for athletes**
*Prosenjit Ghosh[1] and Prabha Sundaravadivel[2]*
[1]The University of Texas at Tyler, [2]University of Texas at Tyler

*1:45PM*
**2D.4**

139 **An Automatic and Efficient BERT Pruning for Edge AI Systems**
*Shaoyi Huang[1], Ning Liu[2], Yueying Liang[1], Hongwu Peng[1], Hongjia Li[2], Dongkuan Xu[3], Mimi Xie[4], Caiwen Ding[1]*
[1]University of Connecticut, [2]Northeastern University, [3]The Pennsylvania State University, [4]The University of Texas at San Antonio

# SESSION PW1

## Thursday April 7

## Poster and WIP Session 1

Chair: **Cindy Yang Yi**, Virginia Tech

*9:45AM*
**PW1.1**
**Lightweight Neural Network Architectures for Resource-Limited Devices**
*April Reed[1], Xiaokun Yang[1], Shi Sha[2]*
[1]University of Houston Clear Lake, [2]Wilkes University

*9:50AM*
**PW1.2**
**Computation of Soft Error Rates Considering Test Pattern Sequences**
*Danushka Senarathna and Spyros Tragoudas*
Southern Illinois University Carbondale

*9:55AM*
**PW1.3**
**Machine Learning Approach to Characteristic Fluctuation of Bulk FinFETs Induced by Random Interface Traps**
*Rajat Butola[1], Yiming Li[2], Sekhar Kola[1]*
[1]National Yang Ming Chiao Tung University, [2]National Chiao Tung University

*10:00AM*
**PW1.4**
**A Unified Statistical Analysis of Comprehensive Fluctuations of Gate-All-Around Silicon Nanosheet MOSFETs Induced by RDF, ITF, and WKF Simultaneously**
*Sekhar Kola[1], Yiming Li[2], Chieh-Yang Chen[1], Min-Hui Chuang[1]*
[1]National Yang Ming Chiao Tung University, [2]National Chiao Tung University

*10:05AM*

**PW1.5**

**Hardware Trojans for Confidence Reduction and Misclassifications on Neural Networks**

*Mahdieh Grailoo[1], Mairo Leier[2], Samuel Pagliarini[2]*

[1]Dpt. of Computer Systems, Tallinn University of Technology, Estonia, [2]Tallinn University of Technology (TalTech)

*10:10AM*

**PW1.6**

**Reusing Verification Assertions as Security Checkers for Hardware Trojan Detection**

*Mohammad Eslami[1], Tara Ghasempouri[2], Samuel Pagliarini[3]*

[1]Department of Computer Systems, Tallinn University of Technology, [2]Department of Computer System, Tallinn University of Technology, Estonia, [3]Tallinn University of Technology (TalTech)

*10:15AM*

**PW1.7**

**HPAM: An 8-bit High-Performance Approximate Multiplier Design for Error Resilient Applications**

*Divy Pandey[1], Vishesh Mishra[1], Saurabh Singh[1], Sagar Satapathy[2], Babita Jajodia[1], Dip Sankar Banerjee[2]*

[1]Indian Institute of Information Technology Guwahati, [2]Indian Institute of Technology Jodhpur

*10:20AM*

**PW1.8**

**Hardware-aware 3D Model Workload Selection and Characterization for Graphics and ML Applications**

*Ruihao Li[1], Aman Arora[1], Sikan Li[1], Qinzhe Wu[2], Lizy John[1]*

[1]The University of Texas at Austin, [2]University of Texas at Austin

# SESSION PW2

## Thursday April 7

## Poster and WIP Session2

Chair: **Sara Tehranipoor**, Santa Clara University

*9:45AM*
**PW2.1**
40 **Pushing Low Power Limits on Multi-Core High Performance SoC**
*Venkateswar Kowkutla, Siva Kothamasu, Kazunobu Shin, Chunhua Hu*
Texas Instruments Inc.

*9:50AM*
**PW2.2**
87 **Beyond Verilog: Evaluating Chisel versus High-level Synthesis with Tiny Designs**
*Xiangdong Wei and Xinfei Guo*
Shanghai Jiao Tong University

*9:55AM*
**PW2.3**
29 **Quantum Technology for Comparator Circuit**
*Hafiz Hasan Babu[1], Khandaker Mohi Uddin[2], Rownak Himel[3], Nitish Biswas[2]*
[1]University of Dhaka, [2]Dhaka International University, [3]Dhaka International University

*10:00AM*
**PW2.4**
31 **Density Aware Cell Library Design for Design-Technology Co-Optimization**
*Shinichi Nishizawa and Toru Nakura*
Fukuoka University

*10:05AM*
**PW2.5**
21 **Examining Vulnerability of HLS-designed Chaskey-12 Circuits to Power Side-Channel Attacks**
*Saya Inagaki[1], Mingyu Yang[1], Yang Li[2], Kazuo Sakiyama[2], Yuko Hara-Azumi[1]*
[1]Tokyo Institute of Technology, [2]The University of Electro-Communications

*10:10AM*

**PW2.6**

27 **Challenges of Securing Low-Power LoRaWAN Devices Deployed in Advanced Manufacturing**

*Mohammad Monjur, Joseph Heacock, Joshua Calzadillas, Rui Sun, Qiaoyan Yu*
University of New Hampshire

*10:15AM*

**PW2.7**

35 **Sub-Space Modeling: An Enrollment Solution for XOR Arbiter PUF using Machine Learning**

*Amir Alipour[1], David Hély[2], Vincent Beroulle[2], Giorgio Di Natale[3]*
[1]Universite Grenoble Alpes - LCIS, [2]Grenoble INP LCIS, [3]CNRS TIMA

*10:20AM*

**PW2.8**

**An Offline Hardware Security Assessment Approach using Symbol Assertion and**

50 **Code Shredding**

*zahra kazemi[1], Amin Norollah[2], mahdi fazeli[3], David hely[3], Vincent Beroulle[4]*
[1]PhD. Candidate, [2]Computer Engineering Dept., IUST, [3]Accosiate Proffessor, [4]Proffessor

# SESSION 3DIC

## Thursday April 7

### Approximate Computing & Monolithic 3D ICs

Chair: **Tobias Gemmeke**, RWTH Aachen University
Co-Chair: **Ankur Guha Roy**, Broadcom

*9:45AM*
**3DIC.1**
**EFCSA: An Efficient Carry Speculative Approximate Adder with Rectification**
39 *Saurabh Singh[1], Vishesh Mishra[1], Sagar Satapathy[2], Divy Pandey[1], Kaustav Goswami[3], Dip Sankar Banerjee[2], Babita Jajodia[1]*
[1]Indian Institute of Information Technology Guwahati, [2]Indian Institute of Technology Jodhpur, [3]University of California Davis

*10:05AM*
**3DIC.2**
61 **Thermal Modeling and Design Exploration for Monolithic 3D ICs**
*Baoli Peng[1], Vasilis Pavlidis[2], Yi-Chung Chen[3], Yuanqing Cheng[1]*
[1]Beihang University, [2]University of Manchester, [3]Tennessee State University

*10:25AM*
**3DIC.3**
148 **Discrete Steps towards Approximate Computing**
*Michael Gansen, Jie Lou, Florian Freye, Tobias Gemmeke, Farhad Merchant, Albert Zeyer, Mohammad Zeineldeen, Ralf Schlüter, Xin Fan*
RWTH Aachen University

# SESSION 3SS

## Thursday April 7

## Intelligent Internet of Battery-less Things

Chair: **Mimi Xie**, University of Texas at San Antonio

*9:45AM*

**3SS.1**

**An Intermittent OTA Approach to Update the DL Weights on Energy Harvesting Devices**

136

*Wei Wei[1], Sahidul Islam[2], Jishnu Banerjee[2], Jieren Deng[3], Chen Pan[4], Caiwen Ding[3], Mimi Xie[2]*

[1]UTSA, [2]The University of Texas at San Antonio, [3]University of Connecticut, [4]Texas A&M University-Corpus Christi

*10:05AM*

**3SS.2**

137 **Aperiodic Tasks Scheduling of Energy Harvesting Embedded Systems**

*Hongzhi Xu[1], Binlian Zhang[1], Chen Pan[2]*

[1]Jishou University, [2]Texas A&M University-Corpus Christi

*10:25AM*

**3SS.3**

138 **Joint-optimization of Node placement and UAV's trajectory for Self-sustaining Air-Ground IoT system**

*Wen Zhang[1], Wenlu Wang[1], Mehdi Sookhak[1], Chen Pan[2]*

[1]Texas A&M University--Corpus Christi, [2]Texas A&M University-Corpus Christi

*10:45AM*

**3SS.4**

**Multilayered Triboelectric Energy Harvester as a Smart Floor Mat**

134

*Fatma Özüdoğru[1], Sercan Koca[1], Seval Kınden[1], Shawana Tabassum[2]*

[1]Eskisehir Technical University, Dept. of Electrical and Electronics Engineering, Eskisehir, [2]The University of Texas at Tyler, Dep. of Electrical Engineering, Tyler, Texas

# SESSION 3A

## Thursday April 7

## Acceleration and Efficiency of Computation and Storage

Chair: **Rasit Topaloglu**, IBM
Co-Chair: **Vita Pi-Ho Hu**, National Taiwan University

*11:15AM*
**3A.1**
6 **A Parallel SystemC Virtual Platform for Neuromorphic Architectures**
*Melvin Galicia[1], Farhad Merchant[2], Rainer Leupers[1]*
[1]RWTH Aachen University, [2]Institute for Communication Technologies and Embedded Systems, RWTH Aachen University

*11:35AM*
**3A.2**
12 **ReFACE: Efficient Design Methodology for Acceleration of Digital Filter Implementations**
*Arman Roohi[1], Shaahin Angizi[2], Pooriya Navaeilavasani[3], MohammadReza Taheri[3]*
[1]University of Nebraska - Lincoln, [2]New Jersey Institute of Technology, [3]Independent Researcher

*11:55AM*
**3A.3**
**In-storage Processing of I/O Intensive Applications on Computational Storage Drives**
72 *Ali HeydariGorji[1], Mahdi Torabzadehkashi[2], Siavash Rezaei[3], hossein bobarshad[4], Vladimir Alves[3], Pai Chou[5]*
[1]University of California, Irvine, [2]University of California, Irvine - NGD Systems, Inc, [3]NGD Systems, Inc., [4]NGDSystems, [5]National Tsing Hua University

*12:15PM*
**3A.4**
129 **Development of On-Wafer EUV Detector for In-Chamber Monitoring in Advanced CMOS Production**
*Ya-Chin King*
National Tsing-Hua University

# SESSION 3B

## Thursday April 7

## AI Accelerator Hardware Design

Chair: **Soheil Salehi**, UC Davis

*11:15AM*
**3B.1**
110 **FPGA based Reservoir computing with optimized reservoir node architecture**
*Chunxiao Lin, Yibin Liang, Yang (Cindy) Yi*
Virginia Tech

*11:35AM*
**3B.2**
102 **A High-Speed CNN Hardware Accelerator with Regular Pruning**
*Yuan Song, Bi Wu, Tian Yuan, Weiqiang Liu*
Nanjing University of Aeronautics and Astronautics

*11:55AM*
**3B.3**
49 **Low-Precision Quantization Techniques for Hardware-Implementation-Friendly BERT Models**
*Xinpei Zhang[1], Yi Ding[1], Mingfei Yu[1], Shin-ichi O'uchi[2], Masahiro Fujita[3]*
[1]the University of Tokyo, [2]AIST-UTokyo AI Chip Design Open Innovation Laboratory, [3]the University of Tokyo, AIST-UTokyo AI Chip Design Open Innovation Laboratory

*12:15PM*
**3B.4**
112 **Integrated Sensing and Computing using Energy-Efficient Magnetic Synapses**
*Shaahin Angizi[1] and Arman Roohi[2]*
[1]New Jersey Institute of Technology, [2]University of Nebraska - Lincoln

# SESSION 3C

## Thursday April 7

## Keep the Chip Secrets Safe: Side-channel Attacks and Defenses

Chair: **Nima Karimian**, San Jose State University

*11:15AM*
**3C.1**
**BIC: Blind Identification Countermeasure for Malicious Thermal Sensor Attacks in Mobile SoCs**
15 *Mostafa Abdelrehim[1], Ahmad Patooghy[2], Amin Malekmohammadi[1], Abdel-Hameed Badawy[3]*
[1]California State University at Bakersfield, [2]North Carolina A&T State University, [3]New Mexico State University

*11:35AM*
**3C.2**
41 **Large-Scale Logic-Locking Attack via Simulation**
*Ruben Purdy and R.D. (Shawn) Blanton*
Carnegie Mellon University

*11:55AM*
**3C.3**
68 **Stealthy Attack on Algorithmic-Protected DNNs via Smart Bit Flipping**
*Behnam Ghavami, Seyd Movi, Zhenman Fang, Lesley Shannon*
Simon Fraser University

*12:15PM*
**3C.4**
88 **Self-timed Sensors for Detecting Static Optical Side Channel Attacks**
*Sourav Roy[1], Tasnuva Farheen[1], Shahin Tajik[2], Domenic Forte[1]*
[1]University of Florida, [2]Worcester Polytechnic Institute

91

*12:35PM*

**3C.5**

**Corruption Exposes You: Statistical Key Recovery from Compound Logic Locking**

*ARSHDEEP KAUR[1], Sayandeep Saha[2], Chandan Karfa[3], Debdeep Mukhopadhyay[4]*
[1]Intel India Pvt. Ltd., [2]IIT Kharagpur, [3]IIT Guwahati, [4]Department of Computer Science and Engineering, Indian Institute of Technology Kharagpur

# SESSION 3D

## Thursday April 7

## Advanced 2.5D and 3D Heterogeneous Integration for State-of-the-Art Computing

Chair: **Srinivasan Gopal**, Broadcom

*11:15AM*
**3D.1**
**Design methodology for scalable 2.5D/3D heterogenous tiled chiplet systems**
142 *srivatsa rangachar srinivasa[1], Jainaveen Sundaram Priya[2], Dileep Kurian[3], Erika Ramirez Lozano[1], Satish Yada[1], Saransh Chhabra[1], Kamakhya Prasad Sahu[4], Paolo Aseron[1], Ronald Kalim[1], Tanay Karnik[4], Anuradha Srinivasan[4]*
[1]Intel Labs, [2]Intel Corporation, [3]Intel technologies, [4]Intel

*11:35AM*
**3D.2**
119 **NoC-enabled 3D Heterogeneous Manycore Systems for Big-Data Applications**
*Biresh Kumar Joardar[1], Jana Doppa[2], Partha Pratim Pande[2], Krishnendu Chakrabarty[1]*
[1]Duke University, [2]Washington State University

*11:55AM*
**3D.3**
118 **Analysis of the Security Vulnerabilities of 2.5-D and 3-D Integrated Circuits**
*Vaibhav Rao[1], Avesta Sasan[2], Ioannis Savidis[1]*
[1]Drexel University, [2]University of California, Davis

*12:15PM*
**3D.4**
**SCIP to the Next Generation of Computing: Extending More than Moore with**
140 **Silicon Photonics Chiplets in Package (SCIP)**
*Vivek Raghunathan, Karl Muth, Bapiraju Vinnakota, Prasad Venugopal, Rebecca Schaevitz, Manish Mehta*
Broadcom

# SESSION 4A

## Thursday April 7

## Machine Learning Systems towards Practical Applications

Chair: **Bo Yuan**, Rutgers University
Co-Chair: **Shiyan Hu**, University of Southampton

*2:15PM*
**4A.1**

117 **An Audio Frequency Unfolding Framework for Ultra-Low Sampling Rate Sensors**
*Zhihui Gao, Minxue Tang, Ang Li, Yiran Chen*
Duke University

*2:35PM*
**4A.2**

147 **BLCR: Towards Real-time DNN Execution with Block-based Reweighted Pruning**
*Xiaolong Ma[1], Geng Yuan[1], Zhengang Li[1], Yifan Gong[1], Tianyun Zhang[2], Wei Niu[3], Zheng Zhan[1], Pu Zhao[1], Ning Liu[4], Jian Tang[4], Xue Lin[1], Bin Ren[3], Yanzhi Wang[1]*
[1]Northeastern University, [2]Cleveland State University, [3]William & Mary, [4]Midea Group

*2:55PM*
**4A.3**

113 **Double Deep Q-Learning Based Irrigation and Chemigation Control**
*Jianfeng Song[1], Dana Porter[1], Jiang Hu[1], Thomas Marek[2]*
[1]Texas A&M University, [2]Texas A&M AgriLife Research and Extension

*3:15PM*
**4A.4**

111 **Enery Consumption and Runtime Performance Optimizations Applied to Hyperspectral Imaging Cancer Detection**
*Eduardo Juarez[1], Raquel Lazcano[2], Daniel Madroñal[2], Cesar Sanz[1]*
[1]Universidad Politecnica de Madrid, [2]Universitá degli Studi di Sassari

# SESSION 4B

## Thursday April 7

## Physical Implementation Considerations in VLSI Designs

Chair: **Srinivas Katkoori**, University of South Florida
Co-Chair: **Sheikh Ariful Islam**, University of Texas, Rio Grande Valley

*2:15PM*
**4B.1**
81 **Path-Based Pre-Routing Timing Prediction for Modern Very Large-Scale Integration Designs**
*Li-Wei Chen[1], Yao-Nien Sui[2], Tai-Cheng Lee[2], I-Ching Tsai[3], Tai-Wei Kung[3], En-Cheng Liu[3], Yun-Chih Chang[3], Yih-Lang Li[2], Mango C.-T. Chao[2]*
[1]National Yng-Ming Chiao-Tung University, [2]National Yang-Ming Chiao-Tung University, [3]Realtek Semiconductor Corp

*2:35PM*
**4B.2**
89 **Multi-Objective Variation-Aware Sizing for Analog CNFET Circuits**
*Zahra Heshmatpour, Lihong Zhang, Howard Heys*
Memorial University of Newfoundland

*2:55PM*
**4B.3**
97 **Layout-based Vulnerability Analysis of LEON3 Processor to Single Event Multiple Transients using Satisfiability Modulo Theories**
*Sowmith Nethula, Vivek Bansal, Ghaith Hamad, Otmane Ait Mohamed*
Concordia University

*3:15PM*

**4B.4**

**Peak Prediction Using Multi Layer Perceptron(MLP) for Edge Computing ASICs Targeting Scientific Applications**

101

*Sandeep Miryala[1], Md Adnan Zaman[2], Sandeep Mittal[1], Yihui Ren[1], Grzegorz Deptuch[1], Gabriella Carini[1], Sioan Zohar[1], Shinjae Yoo[1], Jack Fried[1], Jin Huang[1], Srinivas Katkoori[2]*

[1]Brookhaven National Laboratory, [2]University of South Florida

*3:35PM*

**4B.5**

106 **Improving Pin Accessibility of Standard Cell Libraries in 7nm Technology**

*Tsao-Hsuan Peng, Chih-Chun Hsu, Po-Chun Wang, Rung-Bin Lin*

Yuan Ze University

# SESSION 4C

## Thursday April 7

## Physical Attacks on PUFs and Secure Hardware Design

Chair: **Nima Karimian**, San Jose State University

*2:15PM*
**4C.1**
126 **Joint Optimization of NCL PUF Using Frequency-based Analysis and Evolutionary Algorithm**
*Rabin Yu Acharya and Domenic Forte*
University of Florida

*2:35PM*
**4C.2**
37 **An Efficient Approach to Model Strong PUF with Multi-Layer Perceptron using Transfer Learning**
*Amir Alipour[1], David Hély[2], Vincent Beroulle[2], Giorgio Di Natale[3]*
[1]Universite Grenoble Alpes - LCIS, [2]Grenoble INP LCIS, [3]CNRS TIMA

*2:55PM*
**4C.3**
109 **A Lightweight Neighbor-Averaging Technique for Reducing Systematic Variations in Physically Unclonable Functions**
*Andres Martinez-Sanchez, Deva Borah, Wenjie Che*
New Mexico State University

*3:15PM*
**4C.4**
127 **Characterization of mitigation schemes against timing-based side-channel attacks on PCIe hardware**
*Usman Ali, Salman Abdul Khaliq, Omer Khan*
University of Connecticut

*3:35PM*

**4C.5**

125 **Strong PUF Security Metrics: Response Sensitivity to Small Challenge Perturbations**

*Fynn Kappelhoff[1], Rasmus Rasche[1], Debdeep Mukhopadhyay[2], Ulrich Rührmair[1]*

[1]Ludwig-Maximilians Universität München, [2]IIT Kharagpur, Kharagpu

# SESSION 4D

## Thursday April 7

## Approximate Computing: From Circuit Design to System Integration

Chair: **Iraklis Anagnostopoulos**, Southern Illinois University Carbondale

*2:15PM*
**4D.1**
120 **How much is too much error? Analyzing the impact of approximate multipliers on DNNs**
*Ourania Spantidi and Iraklis Anagnostopoulos*
Southern Illinois University Carbondale

*2:35PM*
**4D.2**
121 **AxBy-ViT: Reconfigurable Approximate Computation Bypass for Vision Transformers**
*Dongning Ma, Xue Qin, Xun Jiao*
Villanova University

*2:55PM*
**4D.3**
122 **Approximate Decision Trees For Machine Learning Classification on Tiny Printed Circuits**
*Konstantinos Balaskas[1], Georgios Zervakis[2], Kostas Siozios[3], Mehdi Tahoori[2], Joerg Henkel[4]*
[1]Aristotle University of Thessaloniki, [2]Karlsruhe Institute of Technology, [3]Department of Physics, Aristotle University of Thessaloniki, [4]KIT

*3:15PM*
**4D.4**
130 **HW/SW Codesign for Approximate In-Memory Computing**
*Simon Thomann, Hong Nguyen, Hussam Amrouch*
University of Stuttgart

*3:35PM*

**4D.5**

131 **On the Resiliency of an Analog Memristive Architecture against Adversarial Attacks**

*Bijay Raj Paudel[1], Vasileios Pentsos[2], Spyros Tragoudas[1]*

[1]Southern Illinois University Carbondale, [2]Southen Illinois University Carbondale

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