Final Program

ISQED

2019
20th International Symposium on

QUALITY ELECTRONIC DESIGN

Security, IoT, ML/AI & Electronic Design

March 6-7, 2019
Santa Clara Convention Center,
Santa Clara, CA USA

IEEE | Electron Devices Society | CAS | Reliability Society | ISQED

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ISQED 2019 is produced and sponsored by the
International Society for Quality Electronic Design

WELCOME TO ISQED 2019

On behalf of the ISQED 2019 conference and technical committees, we are pleased to welcome you to the 20th anniversary of the International Symposium on Quality Electronic Design.

ISQED is the premier interdisciplinary and multidisciplinary electronic design conference aimed at bridging the gap among electronic/semiconductor ecosystem members and providing electronic design tools, integrated circuit techniques, semiconductor manufacturing, advanced 3D integration, and assembly and test methodologies to achieve the overall design quality.

ISQED 2019 is held with the technical sponsorship of the IEEE Electron Devices Society, the IEEE Circuits and Systems Society, and the IEEE Reliability Society. All Conference proceedings & Papers have been published in IEEE Xplore digital library and indexed by Scopus. ISQED continues to provide and foster a unique opportunity to participants to interact and engage themselves in cutting edge tutorials, presentations, and panel and plenary sessions.

This conference is organized around the theme "Security, IoT, ML/AI & Electronic Design". We have invited distinguished keynote speakers, tutorial speakers and panelists who will focus on these timely topics.

The two-day technical program with three parallel sessions packs over 50 peer-reviewed papers highlighting the latest trends in electronic circuit and system design & automation, testing, verification, sensors, security, semiconductor technologies, cyber-physical systems, etc. ISQED 2019 also features a panel discussion, entitled "Hype or hope: Is machine learning the next generation of design and design automation?" on Wednesday, March 6th.

All of the technical presentations, plenary sessions, panel discussions, tutorials and related events will take place on March 6-7 at the Santa Clara Convention Center in Santa Clara, CA USA.

We would like to thank the ISQED corporate sponsors: Synopsys, and Mentor Graphics, for their valuable support of this conference. Welcome to another exciting year of ISQED! It couldn't have happened without your support and participation.

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ISQED 2019 Best Paper

1C.1

Using Spin-Hall MTJs to Build an Energy-Efficient In-memory Computation Platform

Masoud Zabihi[1] *, Zhengyang Zhao*[1] *, Mahendra DC*[2] *, Zamshed I. Chowdhury*[1]
Salonik Resch[1] *, Thomas Peterson*[2] *, Ulya R. Karpuzcu*[1] *, Jian-Ping Wang*[1]
Sachin S. Sapatnekar[1]

[1]Department of Electrical and Computer Engineering, University of Minnesota
[2]School of Physics and Astronomy, University of Minnesota

* Authors of best papers are honored during the Synopsys sponsored luncheon on Wednesday March 6

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NOTES

ISQED 2019 GENERAL INFORMATION

March 6-7, 2019
Santa Clara Convention Center
5001 Great America Pkwy, Santa Clara, CA 95054

KEYNOTE SPEECHES

Wednesday, March 6, 8:45 AM - 9:45 AM
Meeting Rooms 203/204

Adversarial attacks on Security and Privacy of Machine Learning Systems

Sandip Kundu
Program Director
National Science Foundation (NSF)

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Thursday, March 7, 9:00 AM - 9:45 AM
Meeting Rooms 203/204

Machine Learning is Changing the Game for Variability and Characterization and will soon help Analog and Digital Verification

Amit Gupta
General Manager of the IC Verification Solutions
Solido division
Mentor, a Siemens Business

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Luncheon Panel Discussion

Wednesday, March 6, 12:00 PM - 1:25 PM
Meeting Rooms 203/204

Hype or hope: Is Machine Learning the Next Generation of Design and Design Automation?

Machine Learning (ML) has become popular in recent technology. Knowingly or not knowingly we benefit from different ML applications: Google Maps takes us to our destination in the most efficient way and tells us about an accident that may have happened, Amazon Alexa answers our questions and plays our favorite songs, our favorite online shopping site recommends items for us to purchase. We may not love it but we can not leave it either as ML is here to stay. This panel will discuss the impact of ML on design and design automation. How is the semiconductor industry adopting ML, what design automation applications are we working on, what is the outcome? Is ML hype or hope? Join us to listen to our panelists' thoughts on ML and its place in design and design automation.

Chair & Moderator:
Tuna Tarim - *Texas Instruments (Chair)*
Li-C Wang - *University of California – Santa Barbara (Co-Chair)*
Peng Li - *Texas A&M University (Co-Chair)*

Panelists:
Elyse Rosenbaum - *Melvin and Anne Louise Hassebrock Professor in Electrical and Computer Engineering , University of Illinois at Urbana-Champaign*
Mark Ren - *Principal Research Scientist, NVIDIA*
Noel Menezes - *Director Strategic CAD Labs, Intel*
Pradiptya Ghosh - *Sr. Director of Engineering, Mentor Graphics*
Sachin Sapatnekar - *Distinguished McKnight University Professor and the Henle Chair Professor in Electrical and Computer Engineering at the University of Minnesota*

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ISQED LUNCH & AWARDS CEREMONY

Wednesday, March 6, 11:20 AM - 12:00 PM
Meeting Rooms 203/204

ISQED Best Paper Awards

Recipients of the ISQED 2019 Best Paper Award will be recognized during the ISQED luncheon on Wednesday. The best paper is shown in Page 2 of this document.

Embedded Tutorials

Chair & Moderators:
Shiyan Hu - *Michigan Technological University (Chair)*
José Pineda de Gyvez- *Eindhoven University of technology (Co-Chair)*
Jie Gu- *Northwestern University (Co-Chair)*

Meeting Rooms 203/204

Wednesday, March 6, 1:35 PM - 2:35 PM

Tools and approaches to efficiently implement Deep Learning in embedded systems

Dr. Marc Duranton
CEA (French Atomic Energy Commission)

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Wednesday, March 6, 2:35 PM - 3:35 PM

Spiking Neural Networks for Artificial Vision. From Sensing, to Processing and Learning

Dr. B. Linares-Barranco
Scientist , Instituto de Microelectronica de Sevilla

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Embedded Tutorials

Meeting Rooms 203/204

Thursday, March 7, 1:30 PM - 2:30 PM

Developments and Practices for Testing MRAM Memories

Dr. Patrick Girard
LIRMM - CNRS / France

.....

Thursday, March 7, 2:30 PM - 3:30 PM

High Energy Efficient Reconfigurable Neural Network Processor Design

Dr. Shouyi Yin
Professor/Vice Director , Institute of Microelectronics
Tsinghua University

TECHNICAL SESSIONS

There are a total of 13 paper sessions held on Wednesday and Thursday. Technical sessions are held in the format of two-three parallel tracks in **Meeting Rooms 201, 206 & 207**.

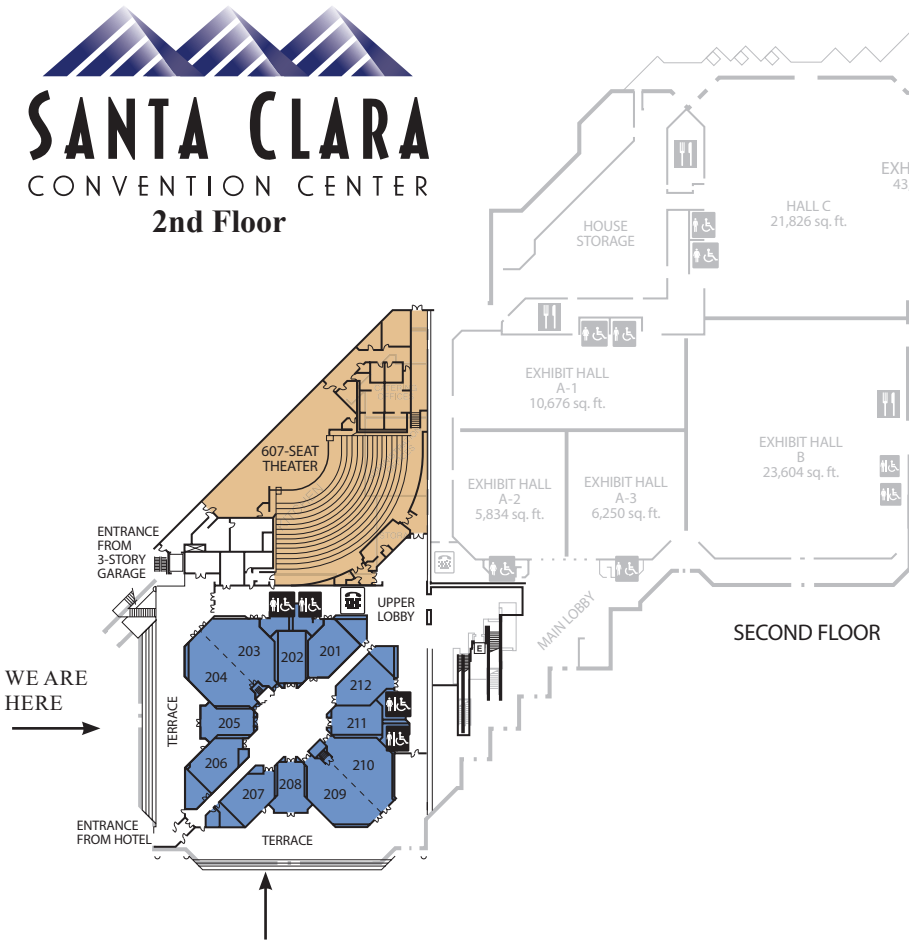
ON-SITE REGISTRATION

Schedule of on-site registration is as follows:

Wednesday, March 6	*8:00 AM - 3:00 PM*
Thursday, March 7	*8:00 AM -1:00 PM*

Registration desk location will be beside the Meeting rooms 203/204.

FLOOR PLAN



Santa Clara Convention Center
2nd Floor
<u>General Sessions & Tutorials:</u>
Meeting Rooms 203/204

<u>Breakout Rooms:</u>
Meeting Rooms, 201, 206 and 207

PROGRAM AT A GLANCE

ISQED 2019 PROGRAM AT A GLANCE				
DATE	**TIME**			
WEDNESDAY 3/6/2019	*8:45AM -9:45AM*	**KEYNOTE SPEECH** **(MEETING ROOMS 203/204)** **ADVERSARIAL ATTACKS ON SECURITY AND PRIVACY OF MACHINE LEARNING SYSTEMS** *SANDIP KUNDU - NATIONAL SCIENCE FOUNDATION(NSF)*		
	9:45 AM - 10:00 AM	**MORNING BREAK**		
	10:00 AM -11:20 AM	**SESSION 1A** **MACHINE LEARNING IN CONVENTIONAL AND EMERGING PLATFORMS** **MEETING ROOM 201**	**SESSION 1B** **MODERN HIGH-LEVEL AND LOGIC SYNTHESIS** **MEETING ROOM 206**	**SESSION 1C** **EMERGING MEMORY AND SPINTRONICS TECHNOLOGIES FOR FUTURE ENERGY EFFICIENT APPLICATIONS** **MEETING ROOM 207**
	11:20 AM -12:00 PM	**ISQED LUNCHEON & PANEL** **MEETING ROOMS 203/204** **BEST PAPER AWARDS , COMMITTEE RECOGNITION** SYNOPSYS® Silicon to Software		
	12:00 PM -1:25 PM	**PANEL DISCUSSION** **HYPE OR HOPE: IS MACHINE LEARNING THE NEXT GENERATION OF DESIGN AND DESIGN AUTOMATION?**		
	1:25 PM -1:35 PM	**BREAK**		
	1:35 PM -2:35 PM	**EMBEDDED TUTORIAL 1** **TOOLS AND APPROACHES TO EFFICIENTLY IMPLEMENT DEEP LEARNING IN EMBEDDED SYSTEMS** **MEETING ROOMS 203/204**		
	2:35 PM -3:35 PM	**EMBEDDED TUTORIAL 2** **SPIKING NEURAL NETWORKS FOR ARTIFICIAL VISION. FROM SENSING, TO PROCESSING AND LEARNING** **MEETING ROOMS 203/204**		
	3:35 PM -3:45 PM	**AFTERNOON BREAK**		
	3:45 PM -5:25 PM	**SESSION 2A** **ADVANCES IN SIMULATION, DESIGN OPTIMIZATION AND DEBUG** **MEETING ROOM 201**	**SESSION 2B** **SYSTEM LEVEL TOOLS, FLOWS, METHODS** **MEETING ROOM 206**	**SESSION 2C** **HIGH PERFORMANCE APPLICATION SPECIFIC ARCHITECTURE** **MEETING ROOM 207**
	5:25 PM -6:45 PM	**POSTER PAPERS AND MIXER**		
THURSDAY 3/7/2019				
	9:00 AM -9:45 AM	**KEYNOTE SPEECH** **(MEETING ROOMS 203/204)** Mentor® A Siemens Business **MACHINE LEARNING IS CHANGING THE GAME FOR VARIABILITY AND CHARACTERIZATION AND WILL SOON HELP ANALOG AND DIGITAL VERIFICATION** *AMIT GUPTA - GENERAL MANAGER OF THE IC VERIFICATION SOLUTIONS SOLIDO DIVISION OF MENTOR, A SIEMENS BUSINESS*		
	9:45 AM -10:00 AM	**MORNING BREAK**		
	10:00 AM -11:20 AM	**SESSION 3A** **DEEP LEARNING CIRCUITS AND ARCHITECURES** **MEETING ROOM 201**	**SESSION 3B** **INNOVATIONS IN CLASSIC HARDWARE SECURITY PROBLEMS** **MEETING ROOM 206**	**SESSION 3C** **CO-OPTIMIZATIONS OF DEVICE PERFORMANCE AND DESIGN RELIABILITY FROM STATE-OF-THE-ART FINFET TO QUANTUM TECHNOLOGIES** **MEETING ROOM 207**
	11:20 AM -11:40 AM	**MORNING BREAK**		
	11:40 AM -1:00 PM	**SESSION 4A** **ARTIFICIAL INTELLIGENCE FOR EFFICIENT APPLICATION SPECIFIC HARDWARE** **MEETING ROOM 201**	**SESSION 4B** **VERIFICATION, ATPG AND FAILURE ANALYSIS** **MEETING ROOM 206**	
	1:00 PM -1:30 PM	**LUNCH BREAK**		
	1:30 PM -2:30 PM	**EMBEDDED TUTORIAL 3** **DEVELOPMENTS AND PRACTICES FOR TESTING MRAM MEMORIES** **MEETING ROOMS 203/204**		
	2:30 PM -3:30 PM	**EMBEDDED TUTORIAL 4** **HIGH ENERGY EFFICIENT RECONFIGURABLE NEURAL NETWORK PROCESSOR DESIGN** **MEETING ROOMS 203/204**		
	3:30 PM -3:40 PM	**AFTERNOON BREAK**		
	3:40 PM -5:00 PM	**SESSION 5A** **PHYSICAL DESIGN OPTIMIZATION** **MEETING ROOM 201**	**SESSION 5B.1** **3D INTEGRATION & ADVANCED PACKAGING** **SESSION 5B.2** **FUTURE OF SOC ARCHITECTURES AND VERIFICATION** **MEETING ROOM 206**	

ISQED Keynote 1P.1

Wednesday March 6

8:45 AM - 9:45 AM
Meeting Rooms 203/204

Adversarial Attacks on Security and Privacy of Machine Learning

Sandip Kundu
Program Director, National Science Foundation (NSF)

As applications of machine learning (ML) have become commonplace in healthcare, security, finance and many other mission critical systems, the security risk of machine-learning systems is emerging as a concern. Machine learning applications evolve through multiple stages including data collection, preparation, labeling, model training, testing and deployment. Malicious actors can impact the reliability and dependability of machine learning system by exploiting vulnerability at any of these stages. In this talk, we present a taxonomy for attack that categorizes an attack based on three fundamental pillars of information security, namely, confidentiality, integrity, and availability. In confidentiality violation, an adversary uses the ML responses to infer the model parameters, or the secret information used in learning process. In an integrity violation, the attacker causes to allow harmful instances to slip through the ML model as false negatives. In an availability violation, the attacker creates a denial of service event. We conclude the talk with various approaches for defending against adversarial attack on ML system.

About Sandip Kundu
Sandip Kundu is a Program Director at the National Science Foundation in the CNS division within the CISE directorate. He is serving in this position on leave from the University of Massachusetts at Amherst, where he is a professor in Electrical and Computer Engineering Department. Kundu began his career at IBM Research as a Research Staff Member; then worked at Intel Corporation as a Principal Engineer before joining UMass Amherst as a professor in 2005. He has published over 250 research papers in VLSI design and test, holds several key patents including ultra-drowsy sleep mode in processors, and has given more than a dozen tutorials at various conferences. He is a Fellow of the IEEE, Fellow of the Japan Society for Promotion of Science (JSPS), Senior International Scientist of the Chinese Academy of Sciences and was a Distinguished Visitor of the IEEE Computer Society. He is currently an Associate Editor of the IEEE Transactions on Dependable and Secure Computing. Previously, he has served as an Associate Editor of the IEEE Transactions on Computers, IEEE Transactions on VLSI Systems and ACM Transactions on Design Automation of Electronic Systems. He has been Technical Program Chair/General Chair of multiple conferences including ICCD, ATS, ISVLSI, DFTS and VLSI Design Conference.

NOTES

Panel Discussion

Wednesday March 6

12:00 PM –1:25 PM
Meeting Rooms 203/204

Hype or Hope: Is Machine Learning the Next Generation of Design and Design Automation?

Summary: Machine Learning (ML) has become popular in recent technology. Knowingly or not knowingly we benefit from different ML applications: Google Maps takes us to our destination in the most efficient way and tells us about an accident that may have happened, Amazon Alexa answers our questions and plays our favorite songs, our favorite online shopping site recommends items for us to purchase. We may not love it but we can not leave it either as ML is here to stay. This panel will discuss the impact of ML on design and design automation. How is the semiconductor industry adopting ML, what design automation applications are we working on, what is the outcome? Is ML hype or hope? Join us to listen to our panelists' thoughts on ML and its place in design and design automation.

Moderator and Chairs:

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Mark Ren - *Principal Research Scientist, NVIDIA*
Noel Menezes - *Director Strategic CAD Labs, Intel*
Pradiptya Ghosh - *Sr. Director of Engineering, Mentor Graphics*
Sachin Sapatnekar - *Distinguished McKnight University Professor and the Henle Chair Professor in Electrical and Computer Engineering at the University of Minnesota*
Manish Pandey - *Synopsys Fellow, and an Adjunct Professor at Carnegie Mellon University*

Thursday March 7

9:00 AM - 9:45 AM
Meeting Rooms 203/204

Machine Learning is Changing the Game for Variability and Characterization and will soon help Analog and Digital Verification

Amit Gupta
General Manager of the IC Verification Solutions Solido division
Mentor Graphics, a Siemens Business

The Golden Age of machine learning is upon EDA. Over the past four years, we have seen large EDA suppliers and customers grow their internal ML teams and strategies, and ML research projects are emerging in all areas of EDA. But, we have not yet seen much of this investment convert into real production flows and work. This talk reviews a set of challenges that make it difficult to bring ML solutions to production for semiconductor design, and discusses approaches for solving them. We will discuss how these approaches are already benefiting variation-aware design and characterization flows, and the broader applicability to analog and digital verification.

About Amit Gupta
Amit Gupta is General Manager of the IC Verification Solutions Solido division of Mentor, a Siemens Business. Previously, he founded Solido Design Automation Inc. in 2005 and served as its President and CEO until its acquisition by Mentor in 2017. Solido is a leader in machine learning variation-aware design and characterization software. In 1999, he founded Analog Design Automation Inc. (ADA), and served as its President, CEO and VP of Business Development until it was acquired by Synopsys in 2004. ADA was a leader in analog optimization software. He has previously served as a Director of the Electronic Design Automation Consortium. Amit holds degrees in both Electrical Engineering and Computer Science with great Distinction from the University of Saskatchewan, and was awarded the 2005 outstanding alumni award for significant accomplishments since graduation.

Embedded Tutorial 1

Wednesday March 6

1:35 PM - 2:35 PM
Meeting Rooms 203/204

Tools and approaches to efficiently implement Deep Learning in embedded systems

Dr. Marc Duranton
CEA (French Atomic Energy Commission)

Summary: Artificial Intelligence, and more particularly Deep Learning are enablers of new applications, and allow computing systems to better interact with the real world by extracting information from signals, images and sounds. But they are demanding in computing power and therefore energy, and pose challenges for being used in embedded systems. This presentation will present some uses cases, tools, approaches and hardware allowing to select neural networks and hardware implementations tuned for embedded applications (Deep Learning at the edge). It will also include some highlight on Auto-ML and on computations using "spiking" data representation."

About Marc Duranton
Dr. Marc Duranton is a member of the Architecture, IC Design & Embedded Software Division of the Research and Technology Department of CEA (French Atomic Energy Commission), where he is involved in realizations for Deep Learning and on Cyber Physical Systems. He previously spent more than 23 years in Philips and Philips Semiconductors where he led the development of the family of L-Neuro chips, digital processors using artificial neural networks techniques. He also worked on several video coprocessors for the VLIW processor TriMedia and for various Nexperia platforms. In NXP Semiconductors, he was in charge of Ne-XVP project that targeted the design of the hardware and software of a multi-core processor for real-time applications and for consumer video processing.
His interests include Deep Learning, Artificial Intelligence and emerging paradigms for computing systems, HPC, embedded systems, (Cognitive) Cyber Physical Systems, parallel architectures for high performance and real-time processing, models of computation and communication with time guaranties. He is a member of the College of Ethics of CEA on "Moral issues in automatic decision-making processes".

Wednesday March 6

2:35 PM -3:35 PM
Meeting Rooms 203/204

Spiking Neural Networks for Artificial Vision. From Sensing, to Processing and Learning

Dr. B. Linares-Barranco
Scientist , Instituto de Microelectronica de Sevilla

Summary: The brain processes information in a very efficient manner by using some kind of spike encoding technique, despite the fact that the underlying technology (neurons) is slow, faulty, and noisy. Since decades neuromorphic engineering has attempted to imitate the sensing and processing of biological neural systems with the hope to develop artificial systems capable of approaching the brain capabilities. We will present CMOS spiking vision sensors and spiking based processing techniques that allow for extremely fast recognition capabilities. Additionally, emerging memory technologies (such as RRAM) have the potential to be exploited for implementing self-learning and/or highly compact spike processing systems. We will review show some techniques for implementing such capabilities.

About B. Linares-Barranco
B. Linares-Barranco received a PhD degree in 1990 from Univ. of Sevilla, Spain on Analog CMOS Oscillators, and a second PhD degree from Texas A&M Univ. in 1991 on CMOS Analog Neural Networks Implementations. In 1991 he became Tenured Scientist of the Spanish Research Council (CSIC) at the "Instituto de Microelectronica de Sevilla" (Sevilla Microelectronics Institute). In 2004 he was promoted to CSIC Full Professor, and since February 2018 he is the Director of the Institute. His research has focused on Neuromorphic Engineering, developing event-driven (spiking) vision sensors, convolution processors, and unsupervised spike-based learning systems. He is co-founder of Prophesee and GrAI-Matter-Labs, two companies whose objectives include commercializing spiking vision sensor applications. During the past two decades he has been involved in several European projects for developing spiking systems, neuromorphic computing systems, and application of emerging memory nanotechnologies to neuromorphic systems. He has also been part of the Human Brain Project (European Commission Flagship).

Embedded Tutorial 3

Thursday March 7

1:30 PM - 2:30 PM
Meeting Rooms 203/204

Developments and Practices for Testing MRAM Memories

Dr. Patrick Girard
LIRMM - CNRS / France

Summary: Memories occupy most of the silicon area in nowadays System-on-Chips. Though widely used, non-volatile Flash memories still have several drawbacks. MRAMs have the potential to mitigate almost all Flash related issues. However, they are prone to defects as any other kind of memories. This embedded tutorial provides an up-to-date and practical coverage of MRAM testing. The first part gives some background on Magnetic Tunnel Junction and existing MRAM technologies. Then, an MRAM architecture used to illustrate the development of test and reliability solutions is presented. The next part detailed resistive-open, resistive-bridge and capacitive defect injection campaigns that are usually performed in order to analyze specific failure mechanisms of MRAMs. Specific functional fault models associated to these failure mechanisms are then described. The last part of the tutorial presents March test algorithms developed for MRAM testing and their validation in industrial environments.

About Patrick Girard

Patrick GIRARD received a M.Sc. degree in Electrical Engineering and a Ph.D. degree in Microelectronics from the University of Montpellier, France, in 1988 and 1992 respectively. He is currently Research Director at CNRS (French National Center for Scientific Research) and works in the Microelectronics Department of the Laboratory of Informatics, Robotics and Microelectronics of Montpellier (LIRMM) - France. From 2010 to 2014, he was head of this Microelectronics Department. He is co-Director of the International Associated Laboratory « LAFISI » (French-Italian Research Laboratory on Hardware-Software Integrated Systems) created in 2013 by the CNRS and the University of Montpellier with the Politecnico di Torino, Italy. His research interests include all aspects of digital testing and memory testing, with emphasis on critical constraints such as timing and power. Reliability and fault tolerance are also part of his research activities. He has served on numerous conference committees and is the founder and Editor-in-Chief of the ASP Journal of Low Power Electronics (JOLPE). He is also an Associate Editor of the IEEE Transactions on Computers, IEEE Transactions on CAD and the Journal of Electronic Testing – Theory and Applications (JETTA - Springer). He has supervised 37 PhD dissertations and has published 7 books or book chapters, 65 journal papers, and more than 230 conference and symposium papers on these fields. Patrick Girard is a Fellow of IEEE.

Embedded Tutorial 4

Thursday March 7

2:30 PM - 3:30 PM
Meeting Rooms 203/204

High Energy Efficient Reconfigurable Neural Network Processor Design

Dr. Shouyi Yin

Professor/Vice Director , Institute of Microelectronics Tsinghua University

Summary: With the rapid development of information technology, the emerging applications, especially artificial intelligence (AI), bring severe challenges to both energy efficiency (the ratio of performance to energy consumption) and flexibility of computing chips. The traditional computing chips with software programming (such as CPU) or hardware programming (such as FPGA) are difficult to meet the requirements of high energy efficiency. Application Specific Integrated Circuit (ASIC) has high energy efficiency, but the poor flexibility restricts its application under the pressure of high cost of <10nm process technology. Coarse-grained reconfigurable computing is a promising solution which combines high energy-efficiency of hardwired logics and high flexibility of software programming. In the reconfigurable architecture, computing units, storage units and interconnection resources compose a regular parallel and distributed processing element (PE) array, which is dynamic reconfigurable. The software applications (programmed by high-level language, such as C) are synthesized into configuration context for reconfiguring hardware resources at run time. In this tutorial, a survey of basic ideas and recent techniques of coarse-grained reconfigurable architecture (CGRA) is presented. A preliminary analysis of the current challenges and future trends of AI processors are introduced to understand the system constraints, and translate them into design specifications. Then several practical reconfigurable processors are presented to demonstrate the potential and benefits of CGRA. As particularly important case, low-power neural networks processors are discussed by highlighting the "reconfigurability" that are enabling the recent and very rapid improvements in energy efficiency.

About Shouyi Yin

Dr. Shouyi Yin received the B.S., M.S., and Ph.D. degrees in electronic engineering from Tsinghua University, Beijing, China, in 2000, 2002, and 2005, respectively. He has worked with Imperial College, London, U.K., as a Research Associate. He is currently associate professor (Tenured) and vice director of Institute of Microelectronics in Tsinghua University. His research interests include reconfigurable computing, domain-specific reconfigurable architecture design and high level synthesis. He has published more than 100 journal papers and more than 50 conference papers. He has received ACM/IEEE ISLPED Design Contest Award (2017), Second Prize of China's State Technological Innovation Award (2015), China's Patent Golden Award (2015), First Prize of Technological Innovation Award of Ministry of Education, China (2014), and Best Paper Award in China Communications IC Technology and Application Conference (2011). Dr. Shouyi Yin is the Secretary-General of EDA Chapter in Chinese Institute of Electronics. He is also the technical committee member of Asia Pacific Signal and Information Processing Association. Dr. Shouyi Yin has been served as program committee member and organizer in the tops VLSI and EDA conferences such as A-SSCC, DAC, ICCAD and ASPDAC. He is the associate editor of Integration, the VLSI journal and editorial board member of Journal of Low Power Electronics.

SESSION 1A

Wednesday March 6

Machine Learning in Conventional and Emerging Platforms

Chair: **Prof. Ronald DeMara**, University of Central Florida
Co-Chair: **Dr. Sicheng Li**, HPE

10:00AM
1A.1
kNN-CAM: A k-Nearest Neighbors-based Configurable Approximate Floating Point Multiplier
Ming Yan[1], Yuntao Song[2], Yiyu Feng[2], Ghasem Pasandi[3], Massoud Pedram[2], Shahin Nazarian[2]
[1]University of Southern California, Ming Hsieh Department of Electrical Engineering, [2]USC, [3]University of Southern California

10:20AM
1A.2
Processing-In-Memory Acceleration of Convolutional Neural Networks for Energy-Efficiency, and Power-Intermittency Resilience
Arman Roohi[1], Shaahin Angizi[2], Deliang Fan[3], Ronald F DeMara[3]
[1]Computer Systems and Architecture Laboratory, Department of EECS, University of Central Florida, [2]Department of Electrical and Computer Engineering, University of Central Florida, [3]University of Central Florida

10:40AM
1A.3
Towards Collaborative Intelligence Friendly Architectures for Deep Learning
Amir Erfan Eshratifar[1], Amirhossein Esmaili[1], Massoud Pedram[2]
[1]University of Southern California, [2]USC

11:00AM
1A.4
A General Framework to Map Neural Networks onto Neuromorphic Processor
haowen fang[1], Amar Shrestha[1], Ziyi Zhao[1], Yanzhi Wang[2], Qinru Qiu[1]
[1]syracuse university, [2]University of Southern California

SESSION 1B

Wednesday March 6

Modern High-Level and Logic Synthesis

Chair: **Srinivas Katkoori**, University of South Florida
Co-Chair: **Srini Krishnamoorthy**, Apple

10:00AM
1B.1
Approximate Logic Synthesis: A Reinforcement Learning-Based Technology Mapping Approach
Ghasem Pasandi[1], Shahin Nazarian[2], Massoud Pedram[2]
[1]University of Southern California, [2]USC

10:20AM
1B.2
Fast Mapping-Based High-Level Synthesis of Pipelined Circuits
Chaofan Li[1], Sachin S. Sapatnekar[2], Jiang Hu[3]
[1]Synopsys Inc., [2]University of Minnesota, [3]Texas A&M University

10:40AM
1B.3
Characterization of Fast, Accurate Leakage Power Models for IEEE P2416
Barkha Gupta and W. Rhett Davis
North Carolina State University

11:00AM
1B.4
Synthesis of Algorithm Considering Communication Structure of Distributed/Parallel Computing
Yukio Miyasaka[1], Ashish Mittal[2], Masahiro Fujita[1]
[1]University of Tokyo, [2]Indian Institute of Technology Bombay

SESSION 1C

Wednesday March 6

Emerging Memory and Spintronics Technologies for Future Energy Efficient Applications

Chair: **Aswin Mehta**, Texas Instruments
Co-Chair: **Prof. Vita Hu**, National Central University, Taiwan

10:00AM
1C.1
Using Spin-Hall MTJs to Build an Energy-Efficient In-memory Computation Platform
Masoud Zabihi, Zhengyang Zhao, Mahendra DC, Zamshed I. Chowdhury, Salonik Resch, Thomas Peterson, Ulya R. Karpuzcu, Jian-Ping Wang, Sachin S. Sapatnekar
University of Minnesota

10:20AM
1C.2
Low Restoration-Energy Differential Spin Hall Effect MRAM for High-Speed Nonvolatile SRAM Application
Sonal Shreya and Brajesh Kumar Kaushik
Indian Institute of Technology Roorkee

10:40AM
1C.3
A Multi-Driver Write Scheme for Reliable and Energy Efficient 1S1R ReRAM Crossbar Arrays
Sherif Amer[1] and Garrett Rose[2]
[1]University of Tennessee, [2]The University of Tennessee

11:00AM
1C.4
Application of Probabilistic Spin Logic (PSL) in detecting satisfiability of a Boolean function
Vaibhav Agarwal[1] and Sneh Saurabh[2]
[1]IIITD, [2]Indraprastha Institute of Information Technology

SESSION 2A

Wednesday March 6

Advances in Simulation, Design Optimization and Debug

Chair: **Srini Krishnamoorthy**, Apple
Co-Chair: **Srinivas Katkoori**, University of South Florida

3:45PM
2A.1
A Compact Model of Negative Bias Temperature Instability Suitable for Gate-Level Circuit Simulation
Xu Liu[1], Alessandro Bernardini[2], Ulf Schlichtmann[2], Xing Zhou[1]
[1]Nanyang Technological University, [2]Technical University of Munich

4:05PM
2A.2
An Automated Design Flow for Synthesis of Optimal Switching Power Supply
Pradeep Chawda[1], Anupriya Prasad[1], Kunjal Rathod[2], Kritika Solanki[3]
[1]Texas Instruments, [2]VMWare, Inc, [3]Chhattisgarh Swami Vivekanand Technical University

4:25PM
2A.3
Robust Transistor Sizing for Improved Performances in Digital Circuits using Optimization Algorithms
Prateek Gupta[1], Harshini Mandadapu[2], Shirisha Gourishetty[2], Zia Abbas[2]
[1]IIIT H, [2]International Institute of Information Technology, Hyderabad

4:45PM
2A.4
Resilient Reorder Buffer Design for Network-on-Chip
Zheng Xu[1] and Jacob Abraham[2]
[1]ARM, Inc., [2]University of Texas

5:05PM
2A.5
Simulation Based Assessment of SRAM Data Retention Voltage
Zhipeng Dong, Xi Cao, Vivek Joshi, Muhammed Ahosan Ul Karim, Torsten Klick, Joerg Schmid
GLOBALFOUNDRIES

SESSION 2B

Wednesday March 6

System Level Tools, Flows, Methods

Chair: **Dr. Brajesh Kumar Kaushik**, Indian Institute of Technology-Roorkee
Co-Chair: **Swaroop Ghosh**, Pennsylvania State University

3:45PM
2B.1
Evaluating Design Space Subsetting for Multi-Objective Optimization in Configurable Systems
Mohamad Hammam Alsafrjalani[1], Tosiron Adegbija[2], Lokesh Ramamoorthi[1]
[1]University of Miami, [2]University of Arizona

4:05PM
2B.2
A Scalable Image/Video Processing Platform with Open Source Design and Verification Environment
Xiaokun Yang[1], Yunxiang Zhang[1], Lei Wu[2]
[1]University of Houston Clear Lake, [2]Auburn University at Montgomery

4:25PM
2B.3
Power-aware IoT based Smart Health Monitoring using Wireless Body Area Network
Jitumani Sarma[1], Akash Katiyar[2], Rakesh Biswas[2], Hemanta Kumar Mondal[2]
[1]Indian Institute of Information Technology, Guwahati, [2]Indian Institute of Information Technology Guwahati, India

4:45PM
2B.4
A Comprehensive Evaluation of Power Delivery Schemes for Modern Microprocessors
Jawad Haj-Yahya[1], Efraim Rotem[2], Avi Mendelson[3], Anupam Chattopadhyay[4]
[1]School of Computer Science and Engineering, Nanyang Technological University, [2]CPU Architect, Intel, Israel, [3]EE and CS Technion, Israel, [4]Nanyang Technological University

5:05PM

2B.5

State Preserving Dynamic DRAM Bank Re-Configurations for Enhanced Power Efficiency

Kaustav Goswami[1], Hemanta Kumar Mondal[1], Shirshendu Das[2], Dip Sankar Banerjee[2]
[1]Indian Institute of Information Technology Guwahati India, [2]Indian Institute of Information Technology Guwahati

SESSION 2C

Wednesday March 6

High Performance Application Specific Architecture

Chair: **Shomit Das**, AMD Research
Co-Chair: **Aswin Mehta**, Texas Instruments

3:45PM
2C.1
Deterministic Stochastic Computation Using Parallel Datapaths
Alexander Groszewski and Travis Lenz
University of Texas at Austin

4:05PM
2C.2
MAPIM: Mat Parallelism for High Performance Processing in Non-volatile Memory Architecture
Joonseop Sim[1], Minsu Kim[2], Yeseong Kim[3], Saransh Gupta[4], Behnam Khaleghi[4], Tajana Rosing[5]
[1]University of California, Sandiego, [2]University of Minnesota, [3]University of California San Diego, [4]University of California, San Diego, [5]UCSD

4:25PM
2C.3
Amoeba-Inspired Stochastic Hardware SAT Solver
Kazuaki Hara[1], Naoki Takeuchi[2], Masashi Aono[3], Yuko Hara-Azumi[1]
[1]Tokyo Institute of Technology, [2]Yokohama National University, [3]Keio University

4:45PM
2C.4
Accelerating Deterministic Bit-Stream Computing with Resolution Splitting
M. Hassan Najafi[1], Sayed Abdolrasoul Faraji[2], Bingzhe Li[2], David Lilja[2], Kia Bazargan[3]
[1]University of Louisiana at Lafayette, [2]University of Minnesota, Twin Cities, [3]University of Minnesota

5:05PM

2C.5

High-Performance NoCs employing the DSP48E1 blocks of the Xilinx FPGAs

Prabhu Prasad B M[1], Khyamling parane[2], Basavaraj Talawar[3]

[1]National Institute of Technology Karnataka, Surathkal, [2]National Institute of Technology Karnataka, [3]CSE, NITK, Surathkal

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SESSION 3A

Thursday March 7

Deep Learning Circuits and Architectures

Chair: **Dr. Sicheng Li**, HPE
Co-Chair: **Pravin Kumar Venkatesan**, Velodyne LiDAR

10:00AM
3A.1
MReC: A Multilayer Photonic Reservoir Computing Architecture
Dharanidhar Dhang, Syed Ali Hasnain, Rabi Mahapatra
Texas A&M University

10:20AM
3A.2
Dynamic Reconfiguration of CNNs for Input-Dependent Approximation
Maedeh Hemmat[1] and Azadeh Davoodi[2]
[1]University of Wisconsin-Madison, [2]University of Wisconsin, Madison

10:40AM
3A.3
An Application Specific Processor Architecture with 3D Inetegration for Recurrent Neural Networks
Sumon Dey and Paul D. Franzon
North Carolina State University

11:00AM
3A.4
Task-Based Neuromodulation Architecture for Lifelong Learning
Anurag Daram[1], Dhireesha Kudithipudi[1], Angel Yanguas-Gil[2]
[1]Rochester Institute of Technology, [2]Argonne National Laboratory,Lemont

SESSION 3B

Thursday March 7

Innovations In Classic Hardware Security Problems

Chair: **Dr. Lin Yuan**, Amazon
Co-Chair: **Anupam Chattopadhyay**, Nanyang Technological University

10:00AM
3B.1
PUF-PassSE: A PUF based Password Strength Enhancer for IoT Applications
Qian Wang[1], Mingze Gao[2], Gang Qu[3]
[1]University of Maryland, [2]University of Maryland, College Park, [3]Univ. of Maryland, College Park

10:20AM
3B.2
On SAT-Based Attacks On Encrypted Sequential Logic Circuits
Yasaswy Kasarabada, Suyuan Chen, Ranga Vemuri
University of Cincinnati

10:40AM
3B.3
A Darwinian Genetic Algorithm for State Encoding Based Finite State Machine Watermarking
Matthew Lewandowski and Srinivas Katkoori
University of South Florida

11:00AM
3B.4
Lightweight Secure-Boot Architecture for RISC-V System-on-Chip
Jawad Haj-Yahya[1], Ming Ming Wong[2], Vikramkumar Pudi[3], Shivam Bhasin[4], Anupam Chattopadhyay[4]
[1]Agency for Science Technology and Research (ASTAR), [2]NanyangTechnologicalUniversity, [3]Indian Institute of Technology Tirupati, [4]Nanyang Technological University

SESSION 3C

Thursday March 7

Co-Optimization of Device Performance and Design Reliability from State-of-the-art FinFET to Quantum Technologies

Chair: **Prof. Vita Hu**, National Central University, Taiwan
Co-Chair: **Aswin Mehta**, Texas Instruments

10:00AM
3C.1
VeriSFQ: A Semi-formal Verification Framework and Benchmark for Single Flux Quantum Technology
Alvin D. Wong[1], Kevin Su[1], Hang Sun[1], Arash Fayyazi[1], Massoud Pedram[2], Shahin Nazarian[1]
[1]University of Southern California, [2]USC

10:20AM
3C.2
Speed Optimization of Vertically Stacked Gate-All-Around MOSFETs with Inner Spacers for Low Power and Ultra-Low Power Applications
Ya-Chi Huang, Meng-Hsueh Chiang, Shui-Jinn Wang
National Cheng Kung University

10:40AM
3C.3
Impact of Self-heating on Performance and Reliability in FinFET and GAAFET Designs
Vidya A. Chhabria and Sachin S. Sapatnekar
University of Minnesota

11:00AM
3C.4
Device Designs and Analog Performance Analysis for Negative-Capacitance Vertical-Tunnel FET
Hung-Han Lin and Vita Pi-Ho Hu
National Central University

SESSION 4A

Thursday March 7

Artificial Intelligence for Efficient Application Specific Hardware

Chair: **Dr. Amey Kulkarni**, Velodyne LiDAR
Co-Chair: **Dr. Abhilash Goyal**, Velodyne LiDAR

11:40AM
4A.1
Behavioral Modeling of Tunable I/O Drivers with Pre-emphasis Using Neural Networks
Huan Yu[1], Jaemin Shin[2], Tim Michalka[2], Mourad Larbi[1], Madhavan Swaminathan[1]
[1]Georgia Institute of Technology, [2]Qualcomm Technologies, Inc.

12:00PM
4A.2
Small Memory Footprint Neural Network Accelerators
Kenshu Seto[1], Hamid Nejatollahi[2], Jiyoung An[3], Sujin Kang[4], Nikil Dutt[2]
[1]Tokyo City University, [2]University of California, Irvine, [3]Kyung Hee University, [4]Hanyang University

12:20PM
4A.3
Minimizing Classification Energy of Binarized Neural Network Inference for Wearable Devices
Morteza Hosseini[1], Hirenkumar Paneliya[1], Utteja Panchakshara Kallakuri Niyogi[2], mohit khatwani[2], Tinoosh Mohsenin[1]
[1]University of Maryland Baltimore County, [2]University of Maryland, Baltimore County

12:40PM
4A.4
Exploiting Energy-Accuracy Trade-off through Contextual Awareness in Multi-Stage Convolutional Neural Networks
Katayoun neshatpour, Farnaz Behnia, Houman Homayoun, Avesta Sasan
George Mason University

SESSION 4B

Thursday March 7

Verification, ATPG and Failure Analysis

Chair: **Vinod Vishwanath**, Real Intent, Inc.
Co-Chair: **Sreejit Chakravarty**, Intel Corporation

11:40AM
4B.1
Assertion Coverage Aware Trace Signal Selection in Post-Silicon Validation
Xiaobang Liu and Ranga Vemuri
University of Cincinnati

12:00PM
4B.2
A Communication-Centric Observability Selection for Post-Silicon System-on-Chip Integration Debug
Yuting Cao[1], Hao Zheng[1], Sandip Ray[2]
[1]University of South Florida, [2]University of Florida

12:20PM
4B.2
Automatic Test Pattern Generation for Double Stuck-at Faults Based on Test Patterns of Single Faults
Peikun Wang[1], Amir Masoud Gharehbaghi[2], Masahiro Fujita[1]
[1]University of Tokyo, [2]The University of Tokyo

12:40PM
4B.2
Deep Learning-Based Wafer-Map Failure Pattern Recognition Framework
Tsutomu Ishida, Izumi Nitta, Daisuke Fukuda, Yuzi Kanazawa
Fujitsu Laboratories Ltd.

SESSION 5A

Thursday March 7

Physical Design Optimization

Chair: **Rung-Bin Lin**, Yuan Ze University
Co-Chair: **Srinivas Katkoori**, University of South Florida

3:40PM
5A.1
Drive-Strength Selection for Synthesis of Leakage-Dominant Circuits
Mahfuzul Islam[1], Shinichi Nishizawa[2], Yusuke Matsui[3], Yoshinobu Ichida[3]
[1]Kyoto University, [2]Saitama University, [3]ROHM Semiconductor

4:00PM
5A.2
Estimating Pareto Optimum Fronts to Determine Knob Settings in Electronic Design Automation Tools
Billy Huggins, W. Rhett Davis, Paul Franzon
North Carolina State University

4:20PM
5A.3
An Artificial Intelligence Approach to EDA Software Testing: Application to Net Delay Algorithms in FPGAs
Madhu Raman, Nizar Abdallah, Julien Dunoyer
Microsemi

4:40PM
5A.4
Impact of Double-Row Height Standard Cells on Placement and Routing
Rung-Bin Lin and Yu-Xiang Chiang
Yuan Ze University

SESSION 5B.1

Thursday March 7

3D Integration & Advanced Packaging

Chair: **Ali A. Shahi**, GlobalFoundries
Co-Chair: **Vinod Vishwanath**, Real Intent, Inc.

3:40PM
5B.1.1
A Non-Slicing 3-D Floorplan Representation for Monolithic 3-D IC Design
Shantonu Das and Dae Hyun Kim
Washington State University

4:00PM
5B.1.2
Routing Complexity Minimization of Monolithic Three-Dimensional Integrated Circuits
Sheng-En(David) Lin and Dae Hyun Kim
Washington State University

SESSION 5B.2

Thursday March 7

Future of SOC Architectures and Verification

Chair: **Vinod Vishwanath**, Real Intent, Inc.
Co-Chair: **Ali A. Shahi**, GlobalFoundries

4:20PM
5B.2.1
Towards Energy Efficient non-von Neumann Architectures for Deep Learning
Antara Ganguly[1], Rajeev Muralidhar[2], Virendra Singh[1]
[1]Indian Institute of Technology, Bombay, [2]Telstra Communications

4:40PM
5B.2.2
Closing the Verification Gap with Static Sign-off
Pranav Ashar and Vinod Viswanath
Real Intent, Inc.

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- ***Advanced & 3D IC Packaging Technology***
- ***Hardware Security***
- ***PCB and PWB Technology & Manufacturing***
- ***Circuit & System Design***
- ***EDA Methodologies, Tools, Flows***
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- ***Test & Verification***
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