“Tomorrows High-quality SoCs Require High-quality Embedded Memories Today”

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Goal and Outline

IC designers: awareness of memory challenges
Memory designers: no surprises, hopefully!

- Dominance of embedded Memories
- Memory Design Challenges
- Manufacturability
- Reliability
- SoC Design Support

If Memory Does not Dominate Your Design Today, It Will Very Soon

- Manufacturing Cost (area, yield, wafer cost)
- Dynamic and leakage power consumption
- Performance
- UDSM effects (IR-drop, EM, leakage (gate!), well proximity, ...)
- Time-to-tapeout
- Time-to-volume

Maximum eSRAM content per IC at IFX

- eSRAM contents [Mbit]
8-Channels ADSL Chip

- **Complexity:** 36.7 mil transistors
- **Area:** 94.8 mm² (0.18µm C10N)
- **SRAM:** 4.6 Mbit (400 macros!!)
- **DSP:** 4 Oak’s
- **MIPS:** 5000 MIPS(Oak) ++
  + Trellis/Viterbi
- **Clock domains:** 11 independent clks
  ~ 200 dependent clocks
- **Frequency:** 150/120 MHz (2 PLL’s)

IWORX: Interworking Controller for 3G Mobile Base Station

- **Application:** ATM Line Card Controller for “Next Generation (3G) Mobile Infrastructure (UMTS Base Stations)”
- **Package:** BGA388
- **Process:** 0.18 µm CMOS
  6 Layer Metal (fat)
- **Chip Area:** 193.7 mm²
  13.72 mm x 14.12 mm
- **Transistors:** ~ 80 Mio.
- **Gate Count:** ~ 2,250,000
  (including Tricore™)
- **SRAM:** 11 Mbit (140 macros)
- **Test Concept:** Full Scan Path
  63 Chains x ~2000 FF
  MemoryBIST

Embedded DRAM Networking Switch Chip

- **Complexity:** 850k logic gates
- **Area:** 117 mm² (0.20µm C9DD1)
- **Memory:** 16 Mbit DRAM (4 Macros)
- **460 k SRAM**
  59 Register Files
  (241k total)
- **Frequency:** 100 MHz (1 PLL)

Memory Landscape changed dramatically over the last 10 years

**Challenges**

- Mostly SRAM
- Types: SP, DP, ROM
- Memories on shrinkpath
- Few EDA models
- Verification on Silicon

- SRAM/ROM, eDRAM, 1T, NVM, ....
  => integrated on SoC
- SoC vs. SIP
- Varied types, e.g. RFs, CAMs, ...
- New design for each generation
  > 15 EDA models; very high accuracy
- UDSM: Leakage; IR drop; EM; X-talk
- Tight coop. Design <=> TD / Fab
- Silicon Qualification essential

1990 2002
A high-quality Embedded Memory ...

- meets requirements specifications
- can be manufactured with high yield at low cost
- can be tested economically
- meets reliability criteria
- enables timely product design

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A high-quality Embedded Memory ...

- meets requirements specifications
  - area
  - performance
  - active power
  - standby power
  - correct and accurate EDA modeling
  - functionality
- can be manufactured with high yield at low cost
- can be tested economically
- meets reliability criteria
- enables timely product design

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UDSM Process Technologies result in major challenges

- Dramatically increasing junction leakage
- Gate leakage
- Relative manufacturing variations increasing
- Dominance of wiring delays

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Key Issues in Excellent Memory Design

- Bit Cell
  - As small as possible (DR waivers)
  - Tradeoff area / leakage / performance
  - Electrically robust
  - Tuned for the specific target fab
  - Running in high volume
- Architecture
  - Low Leakage / High Speed
  - Active Well / Virtual Rail
  - Global / Local Bitlines
  - Multi-Banking
  - Timing Control Circuitry
  - Compiler-Optimized
  - Redundancy
- Sense Amplifier
  - Voltage / Current Sensing
  - Robustness analysis (sensitivity, MC)
  - Layout critical (matching)
- Macro Layout
  - Power Routing: IR Drop, EM, Size Power-ring
  - Crosstalk
  - DfM rules (incl. DRC runsets)

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Excellent Quality Assurance - escorting the entire Development

Component development

MemLib

Continuous quality improvement

Test-chips

Regular reviews

Platform Qualific.

Macro Qualific.

Macros for qualification

Product-like chip

Library Verification on Silicon

Semi-Custom Test Chip: TCQ-P
(Test Chip for Qualification of Platform)

Parts similar to product

+ Parts for low level analysis

Qualification - not just verification

TCQP - Test Chip for Qualification of Platform
Memories, Testchips Must be Designed for Analyzability

- Probe Points
- Bitmap capabilities
- Programmable Timing Control (Read Margin)
- S/H Measurements possible
- etc.

- Rapid analysis and yield ramp-up depend on
  - Robust design
  - Design-for-Analysis techniques
  - Tight Cooperation between Design, Manufacturing and Analysis

Manufacturing: High Yield & Low Cost => Redundancy

- Definition: Introduction of spare elements to increase the circuit yield after production at the expense of overhead in area, power consumption or performance.

Cost: NRE, Area, Repair & Retest

Hard vs. Soft Redundancy: Fuses, NVM, Register storage

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Hard vs. Soft Redundancy: Fuses, NVM, Register storage

Word-based Redundancy

- Advantages:
  - Good yield improvement, low area overhead
  - 128 kbit: 2.5%
  - 256 kbit: 1.3%
  - from 1 Mbit on: <1%
  - Flexible sizes
  - One wrapper can handle multiple memories

- Disadvantage:
  - Not robust to specific fault patterns (word-/bitline faults)
Choice of Redundancy Solutions Required for Overall Optimum

A high-quality Embedded Memory ...

- meets requirements specifications
- can be manufactured with high yield at low cost
- can be tested economically
  - BIST vs. Memory Tester
  - Test algorithm: coverage vs. effort
  - TDR functionality (Test, Diagnosis, Repair)
- meets reliability criteria
- enables timely product design

Productivity Gain (8kx32 macros)

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Radiation induced Soft Error Rate in embedded SRAMs

1 FIT = 1 failure / 10^9 hours
What is radiation induced SER?

A soft error is a non-destructive error caused by alpha particles or cosmic rays.

Ionizing radiation generates a current peak
⇒ flips a bit without physical damage
⇒ significantly delays a signal

Memories and logic circuits are effected, depending on critical charge.

Measures for Radiation Hard Systems

- fault tolerant architectures
- system simulations
- increase of critical charge
- no dynamic logic
- parity bits / check sums
- error correction codes etc.
- low alpha packages
- low alpha solder bumps
- B11 enriched BPSG
- SOI etc.

Choice of Memory Technology Depends on Many Factors

- Wafer Yield
- License Cost
- NRE (memory; process)
- Test cost (Burn-In?)
- Performance
- Operating Conditions
- Memory Granularity
- Availability

Additional Decision Factors

- Test cost (Burn-In?)
- Performance
- Operating Conditions
- Memory Granularity
- Availability
Choice of Memory Technology Depends on Many Factors

Alternatives: SoC vs. SiP
- MCM
- Face-to-Face
=> Directly Utilize Yield Learning of Commodity DRAM manufacturing

A high-quality Embedded Memory ...
- meets requirements specifications
- can be manufactured with high yield at low cost
- can be tested economically
- meets reliability criteria
- enables timely product design
  - memories tightly integrated into the design flow
  - information about tradeoffs rapidly available
  - limited number of updates
  - concise information about changes for updates (tech. parameters!)

Excellent Quality Assurance - escorting the entire Development

Verification of Library Views for Design Flow

Discrete quality levels
- Single library regression test
- Regular reviews
- Q-Level 1

Multi library regression test
- Single cell in single tool test
- Regular reviews
- Q-Level 2
- Q-Level 3

Continuous quality improvement
- Macro TCs
- Production chip
- MemLib
- Excellent Quality Assurance

Focus Topics:
- Automation of QA
- Install a separate QA team
- Ensure corner case coverage
- Replicate designer behavior

Library Verification on Silicon
Memory Explorer

- Fast generation of datasheets for evaluations
- Easy comparison of memory configurations

Summary

- Memory Dominance on SoCs continues to increase
- UDSM effects force changes in embedded memory design

- Memory Designers:
  - Work very closely with SoC Designers and TD / Fab people
  - Design for robustness, manufacturability, analyzability

- SoC Designers:
  - Perform reviews (concept; architecture; design)
  - Insist on detailed silicon reports
  - Ensure that manufacturability is addressed