TUTORIALS
San Carlos/San Juan

TUTORIAL I
Monday, March 27, 2006
9:00am-12:30pm

Emerging Technologies for VLSI Design

Chair & Moderator:
Anirudh Devgan, *Magma Design Automation*

Presenters:
Andre DeHon, *California Institute of Technology, Pasadena, CA*
Kaustav Banerjee, *University of California, Santa Barbara, CA*
Rajiv Joshi, *Research Staff Member, IBM T J Watson Research Center, NY*

SUMMARY:
This tutorial discusses emerging technologies. We will focus on three major components:

Computing with Nanowires
Chemists can now construct wires which are a few atoms in diameter; these wires can be selectively field-effect gated, and wire crossings can act as programmable diodes. The tiny feature sizes offer a path to economically scale to atomic dimensions. However, the associated bottom-up synthesis techniques only produce highly regular structures and have high defect rates and minimal assembly control. In this tutorial, I review architectural techniques to bridge between lithographic and atomic-scale dimensions, build circuits from these nanowire building blocks, and tolerate defective and stochastic assembly.

Emerging Interconnect Technologies based on Carbon Nanotubes
Carbon nanotube (CNT) interconnects have recently aroused a lot of interest as a promising candidate to meet the challenges faced by copper interconnects. This section of the tutorial will start with an overview of the key challenges in the domain of scaled copper interconnects and highlight their limitations arising due to a number of nanometer scale effects. Specifically, it will illustrate how combined effects of increasing copper resistivity, decreasing thermal conductivity of ILD materials and rising current densities in on-chip wires result in significant rise in interconnect temperatures that significantly degrades electromigration reliability and can limit their current carrying capacity in the near future. State-of-the-art CNT interconnects will be examined including their electrical, mechanical, and thermal properties as well as their fabrication issues. A comprehensive evaluation of CNT bundle interconnects vis-à-vis Cu will be presented and their impact on all aspects of VLSI circuits - performance, power dissipation and reliability - will be quantified, while accounting for practical limitations of the technology. Finally, hybridization of CNT and Cu interconnects will be discussed as a very attractive alternative for deep nanometer scale VLSI technologies.

Nanometer Technologies
To continue scaling of the CMOS devices deep into sub-65nm technologies, fully depleted SOI, strained-Si on SiGe, FinFETs with double gate, and even further, three-dimensional circuits will be utilized to design high-performance circuits. We will discuss unique design aspects and issues resulting from this scaling such as gate-to-body tunneling, self-heating, reliability issues, and process variations. As the scaling approaches various physical limits, new design issues such as Vt modulation due to leakage, low-voltage impact ionization, and higher Vt,lin to maintain adequate Vt,sat, continue to surface. Circuit examples using SRAM are illustrated with the impact of technology. In case of FinFETs, impact of quantization and thermal impact on multi-finger devices is brought out. In this part of the tutorial, we will discuss these emerging trends and design issues related to aggressive device scaling.

TUTORIAL II
Monday, March 27, 2006
1:30pm-5:00pm

Variability and Its Impact on Design

Chair & Moderator:
Anirudh Devgan, *Magma Design Automation*

Presenters:
Keith Bowman, *Intel Corporation*
Michael Orshansky, *University of Texas-Austin*
Sachin S. Sapatnekar, *University of Minnesota*

Summary:
As digital designs scale down into the sub-100nm regime, the effects of variations are seen to dramatically affect the behavior of the circuit. These may arise from:

1. Fluctuations attributed to the manufacturing process (e.g., drifts in channel length, oxide thickness, threshold voltage, or doping concentration), which affect the circuit yield.

2. Variations in the environmental operating conditions (e.g., supply voltage, temperature, or particle strikes that lead to soft errors) after the circuit is manufactured, which affect the correctness of the behavior of the design.

These variations have been observed at the 90nm technology node, and trends show that this will be even more significant from the 65nm node onwards. Some of these variations are entirely deterministic (metal fill density, etc.), while others are random, as their cause is either unknown, unattributable, or too difficult to model. Either way, it is imperative to analyze their effects and design circuits to be tolerant to variations. Circuit performance, in terms of both timing and power, is shown to vary significantly under process and environmental variations. While timing can vary by unacceptably large amounts, a second important factor is the leakage power (which is becoming a major fraction of the total power): its exponential dependence on process parameters can lead to large swings in the power dissipation from die to die after manufacturing. Therefore, variation-tolerant design is imperative for the design of next-generation digital integrated circuits. Traditional circuit design techniques tackle this by using several design corners, but they are insufficient under the magnitude and scale of these variations for several reasons: first, they are incapable of accurately predicting parametric yield, and second, they lead to the run-time explosion due to the increasing number of corner cases that need to be considered. While variation-tolerant design has been practice in the analog world for many years, the scale of digital problems, where circuits may have a billion transistors or more, renders those techniques inadequate. The past few years have seen a great deal of work on robust design techniques for digital circuits, ranging from employing statistical methods for analysis and optimization at the design phase, to building in compensatory techniques to recover performance (timing and power) after the circuit is manufactured. The objective of this tutorial is to present an overview of the state of the art in variation-tolerant design, while highlighting important unsolved research problems for the future.
The tutorial will consist of the following segments:

Sources of variation and impact of variations on circuits
A good understanding of the sources and nature of process variation is key to accurately simulating their impact design. As the need for better modeling of variation margins arises, so does the need to understand and model the systematic sources of variation and incorporate them in the design flow. This portion of the tutorial will introduce the various sources of variation, focusing on their impact on design and how to mitigate their effects. The impact of process, voltage and temperature (PVT) variations on performance and power, and on circuit robustness will be discussed. Scaling trends of these variations and their impacts will be presented. Promising design and circuit techniques that can mitigate variation impacts and make designs variation-tolerant will be described. Furthermore, models and measurement methodologies of key systematic and random process-related variations, needed to enable robust designs, will be presented.

Analysis of timing and power under variability
In the second section of the tutorial the speaker will discuss analysis and optimization strategies for design in the presence of variability. He will cover the recent work in statistical static timing analysis (SSTA), and discuss the algorithmic approaches to efficient SSTA, including block-based algorithms suitable for incremental analysis and useful within the optimization loops, as well as the sign-off quality path-based algorithms.

Design optimization techniques to overcome variations
The speaker in this section will then cover the growing body of work on the fully statistical optimization methods, which optimize the performance of a digital circuit under random variations, using techniques such as transistor and gate sizing, and statistical dual-Vth optimization, and promising significant advantages in terms of timing and leakage power parametric yields. He will also address the techniques for dealing with systematic sources of variability.

Session EP1
Panel Discussion & Dinner

Donner Pass Room
6:30pm - 8:30pm

Power management and optimization challenges for sub 90nm CMOS designs
- What is the real cost of long battery life?

Panel Organizer: ***Pallab Chatterjee**, SiliconMap*
Panel Moderator: ***Mike Santarini,** EDN magazine*

The recent migration to DSM process geometries and very large gate count, has created a need for low power design and multi-voltage designs as standard rather than the exception. The variety of power optimization and power planning tools has resulted in ad-hock modification to existing design flows to accommodate the new requirements. This has given rise to wide variation in the QOR of the silicon that incorporates these design features. The

panel will review and discuss places in the design flow where power planning and optimization are beneficial to improving QOR and also some of the analysis and signoff limitations to the automation that is available and directed at this task.

Panelists:
Dennis Heller, *CEO of Golden Gate Technology*
Adam Traidman, *CEO of GigaScale IC*
James Spoto, *CEO Applied Wave Research*
John Goodenough*, ARM*
Aurangzeb Khan*, Corporate VP Cadence*

Plenary Session 1P

Donner Pass Room

8:30AM - 10:15AM

Co-Chairs: ***Andrew Kahng***
UC San Diego, and Blaze DFM

Kris Verma
Silicon Valley Technical Institute

8:30am
Introduction & Announcements

8:45am
1P.1

Modular service-oriented platform architecture - a key enabler to SoC design quality

Dr. Risto Suoranta
Principal scientist and Research Fellow
Nokia

In the digital convergence era, new products are created at ever faster pace by combining and integrating existing and new technologies in innovative ways. Designers of these products are already facing immense productivity and quality demands. We need new architectural thinking to address the demands of the future. We need to achieve very high-level of reuse and at the same time manage the system complexity. Platformization and modularity are the key to do this. The key to true system modularity is an architectural model where the functional and physical architecture are aligned. One solution is a uniformed interconnect based device architecture consisting of sub-systems with services and applications. Reuse takes place in multiple levels from requirements, through service specifications, and interconnect nodes to sub-systems. Design flow provides verified formal sub-system requirements to be used in internal and/or external purchasing. Finite energy, device heating and peak-power limitations call for a well defined EPM architecture. This solution gives: Ease system integration, Scalability from device to SoC implementations, Allow efficient horizontalization, Match performance with requirements, Speed-up innovations-to-product cycle, while still taking into account the fact we are operation in energy - power - heat limited world.

9:15am
1P.2

Deep sub-100 nm Design Challenges

Dr. T. Furuyama
GM, SoC Research center
Toshiba

Moore's law and the scaling theory have been the guiding principle for the semiconductor industry to accomplish its rapid progress and persistent growth. Semiconductor chips had been continuously benefited from the device scaling by simultaneously achieving higher density, higher performance and lower power consumption until they reached the 100 nm technology node. However, once the silicon technology exceeded this point, i.e. in sub-100 nm nodes, some important device parameters have started to diverge from the scaling theory, such as threshold voltages and leakage currents. As a result, we are able to enjoy only higher density from the device scaling, but neither higher performance nor lower power any longer especially at the deep sub-100 nm nodes. In addition, the increase in device density has created various new problems. A single LSI chip can accommodate more number of gates than the engineers can properly design and integrate in a reasonable time period. This gap causes a serious design efficiency problem. Another problem is the large power consumption of the chip and the power density, which reaches the range of a nuclear reactor. Not only how to efficiently cool the chip but

also how to properly pour the huge current into the chip is getting extremely difficult. Even though the LSI design and initial development are successful, highly integrated chips will face yield problems in the fabrication line often at the beginning of the volume production. Yield learning and the quick yield ramp are crucial especially when the product life time is short, which is usually the case for digital media related SoC's (System on Chip). This presentation will introduce and discuss several approaches to counteract these problems, such as high-level language and platform based design flow, various low power technologies from devices, circuits to architectures, and DFM (Design for Manufacturing) related technologies.

9:45am

1P.3

Successful IP Business Models

Dr. Di Ma
Vice President, Field Technical Support
TSMC

The onward march of Moore's Law obviously brings with it a host of challenges, not the least of which is how to design to the space that is now available on an average leading edge semiconductor device. With millions of available transistors and a variety of technology options to choose from, it's small wonder that IP providers have managed to continue to build a viable industry. But that industry is changing, with numerous business models and sources of IP emerging. How will the interaction between IP providers and semiconductor manufacturers change? How will the industry benefit, in terms of quality and availability of IP? Dr. Di Ma will present a foundry perspective, including interesting statistics on IP usage and how the future interplay of foundry and IP provider might develop.

SESSION 1A

Tuesday March 28

10.30AM - 12.00noon

Variation Aware Timing

Chair: **Murat Becer**, CLK Design Automation
CoChair: **Peng Li**, Texas A&M University

Summary:
Variations in IC manufacturing processes are expected to pose significant challenges to design optimization and yield maximization in future nanoscale technologies. This session focuses on the statistical methods for analysis, optimization and design while accounting for process variations. The first two and the last paper directly address variation aware design and optimization. The first paper presents an efficient technique to generate interconnect timing models in terms of the random variables that represent the interconnect variations. The second paper presents a way of optimizing the leakage of SRAM cells, accounting for the process variations. The third paper focuses on an important circuit design technique for reducing the active and standby power Domino logic. The third paper presents novel and efficient way of constructing a current based model library. The last paper presents a technique for adding connections between sub-networks of a clock network to reduce the variability in the clock skews.

10.30AM

1A.1

Variational Interconnect Delay Metrics for Statistical Timing Analysis

Praveen Ghanta, Sarma Vrudhula, Arizona State University

11.00AM

1A.2

Statistically Aware SRAM Memory Array Design

Evelyn Grossar[12], Michele Stucchi[2], Karen Maex[12], Wim Dehaene[1], [1]KUL, [2]IMEC

11.15AM

1A.3

Robust Dynamic Node Low Voltage Swing Domino Logic with Multiple Threshold Voltages

Zhiyu Liu, Volkan Kursun, University of Wisconsin at Madison

11.30AM

1A.4

Constructing Current-Based Gate Models Based on Existing Timing Library

Andrew Kahng, Bao Liu, Xu Xu, University of California at San Diego

11.45AM
1A.5
Efficient Model Update for General Link-Insertion Networks
Zhuo Feng, Peng Li, Jiang Hu, Texas A&M University

SESSION 1B

Tuesday March 28
10.30AM - 12.00noon

High-level Design Verification

Chair: **Tao Feng**, Cadence
CoChair: **Li-C. Wang**, University of California Santa Barbara

Summary:
This session covers design verification techniques at the high level. The first paper discusses the use of abstraction to reduce the complexity of verification so that formal verification can be efficiently applied on pipelined processors. The second paper applies a refined EFSM-based approach to implement an effective functional ATPG. The third paper conducts extensive study to assess the difficulty of formal verification. The fourth paper discusses verification in high-level synthesis.

10.30AM
1B.1
Using Abstraction for Efficient Formal Verification of Pipelined Processors with Value Prediction
Miroslav N. Velev, Consultant

11.00AM
1B.2
EFSM Manipulation to Increase High-Level ATPG Effectiveness
Giuseppe Di Guglielmo, Franco Fummi, Cristina Marconcini, Graziano Pravadelli, University of Verona

11.30AM
1B.3
A Technique for Estimating the Difficulty of a Formal Verification Problem
Indradeep Ghosh, Mukul Prasad, Fujitsu Labs. of America

11.45AM
1B.4
A Formal Verification Method of Scheduling in High-level Synthesis
Chandan Karfa[1], Chittaranjan Mandal[1], Dipankar Sarkar[1], Satyam R Pentakota[1], Chris Reade[2], [1]Indian Institute of Technology, Kharagpur, [2]Kingston University

SESSION 1C

Tuesday March 28
10.30AM - 12.00noon

Physical Planning

Chair: **Lei Wang**, University of Connecticut
CoChair: **Eli Bozorgzadeh**, University of California Irvine

Summary:
The first two papers in this session focus on clock distribution. The first paper proposes a fast scheme for inserting crosslinks in a clock tree to reduce skew variability. The second paper presents a quantitative comparison of different clock architectures. The last two papers are on physical synthesis: one is about post-layout gate sizing using game theory and the other one is on thermal-aware floor planning for 3D microprocessors.

10.30AM
1C.1
Fast Incremental Link Insertion in Clock Networks for Skew Variability Reduction *Anand Rajaram, David Z. Pan, University of Texas at Austin*

11.00AM
1C.2
Clock Distribution Architectures: A Comparative Study
Chao-Yang Yeh[1], Gustavo R. Wilke[2], Hongyu Chen[1], Subodh M. Reddy[3], Hoa-van Nguyen[3], Takashi Miyoshi[3], William W. Walker[3], Rajeev Murgai[3], [1]University of California, [2]UFRGS, [3]Fujitsu Laboratories of America, Inc.

11.30AM
1C.3
Post-Layout Gate Sizing for Interconnect Delay and Crosstalk Noise Optimization *Narender Hanchate, Nagarajan Ranganathan, Univ. of South Florida*

11.45AM
1C.4
Interconnect and Thermal-aware Floorplanning for 3D Microprocessors
W.-L. Hung, G. M. Link, Yuan Xie, Vijay Narayanan, M. J. Irwin, Pennsylvania State University

ISQED Luncheon Awards & Speech
Sponsored by Synopsys
Donner Pass Room
12:00pm-1:30pm

Chairs: ***Ali Iranmanesh,*** *Silicon Valley Technical Institute*
Tanay Karnik, *Intel*

12:05pm
Committee Recognition Awards
Best Paper Awards (Sponsored By Magma Design Automation, and Synopsys)

12:30pm
Luncheon Speech:

Simplicity and Executability: Cornerstones of Quality
Michael Keating
Synopsys Inc.

SESSION 2A
Tuesday March 28
1.30PM - 3.30PM

Robust Device and Circuit Design

Chair: **Sheldon Tan**, University of California Riverside
CoChair: **Kevin Cao**, Arizona State University

Summary:
This session addresses the circuit modeling for special purpose transistors such as VDMOS, FinFET, and SOI techniques. Robust circuit design techniques such as Electro-Thermal and transient error will also be addressed.

1.30PM
2A.1
A Compact DC and AC Model for Circuit Simulation of High Voltage VDMOS Transistor
Y. S. Chauhan, C. Anghel, F. Krummenacher, C. Maier, R. Gillon, A. Baguenier, B. Desoete, S. Frere, A. M. Ionescu, M. Declercq, EPFL

2.00PM
2A.2
A Complete Carrier-Based Non-Charge-Sheet Analytic Theory for Nano-Scale Undoped Surrounding-Gate MOSFETs
Jin He, Xing Zhang, Mansun Chan, Yangyuan Wang, Peking University

2.30PM
2A.3
METS: A Metric for Electro-Thermal Sensitivity, and Its Application to FinFETs *Brian Swahn, Soha Hassoun, Tufts University*

3.00PM
2A.4
A Carrier-Based Analytic Model for Undoped (Lightly Doped) Ultra-Thin-Body Silicon-on-Insulator (UTB-SOI) MOSFETs
Jin He, Xing Zhang, Mansun Chan, Yangyuan Wang, Peking University

3.15PM
2A.5
Improving Transient Error Tolerance of Digital VLSI Circuits Using RObustness COmpiler (ROCO)
Chong Zhao, Sujit Dey, University of California at San Diego

SESSION 2B
San Juan Room
Tuesday March 28
1.30PM - 3.30PM

Power, Noise and Timing issues in DSM designs

Chair: **Vamsi Srikantam**, Agilent
CoChair: **Tom Chen,** Colorado State University

Summary:
With increase in process variations and design complexity, meeting power, noise, and timing targets has become increasingly difficult. Statistical timing analysis and budgeting can provide designers with more accurate information about timing robustness. Efficient noise analysis and noise modeling can improve overall design quality. The papers in this session address these critical issues in deep submicron design.

1.30PM
2B.1
Probabilistic Delay Budgeting for Soft Realtime Applications
Soheil Ghiasi, Po-Kuan Huang, UC-Davis

2.00PM
2B.2
TBNM - Transistor-Level Boundary Model for Fast Gate-Level Noise Analysis of Macro Blocks
Jindrich Zejda, Li Ding, Synopsys, Inc.

2.30PM
2B.3
Fast Sequential Cell Noise Immunity Characterization Using Meta-Stable Point of Feedback Loop
Nahmsuk Oh, Li Ding, Alireza Kasnavi, Synopsys, Inc.

2.45PM
2B.4
Pessimism Reduction In Static Timing Analysis Using Interdependent Setup and Hold Times
Emre Salman[1], Ali Dasdan[2], Feroze Taraporevala[2], Kayhan Küçükçakar[2], Eby G. Friedman[1], [1]University of Rochester, [2]Synopsys, Inc.

3.00PM
2B.5
Power Islands: A High-Level Technique for Counteracting Leakage in Deep Sub-Micron
Deniz Dal, Adrian Nunez, Nazanin Mansouri, Syracuse University

3.15PM
2B.6
Simultaneous Statistical Delay and Slew Optimization for Interconnect Pipelines
Andrew Havlir[1], David Pan[2], [1]AMD, [2]University of Texas at Austin

SESSION 2C
Monterey Room
Tuesday March 28
1.30PM - 3.30PM

Memory Analysis

Chair: **Dr. Kanak Agarwal,** IBM
CoChair: **Peter Wright**, Synopsys

Summary:
Since memories are generally designed using the most aggressive design rules, memory designers have developed many techniques to assess the quality of these designs. This session presents 5 papers that address yield and statistical analysis of memories.

1.30PM
2C.1
System-Level SRAM Yield Enhancement
Fadi Kurdahi[1], Ahmed M. Eltawil[1], Rouwaida N. Kanj[2], Young-Hwan Park[1], Sani Nassif[2], [1]UC Irvine, [2]IBM

2.00PM
2C.2
Sensing Margin Analysis of MLC Flash Memories Using a Novel Unified Statistical Model
Young-Gu Kim, Sang-Hoon Lee, Dae-Han Kim, Jae-Woo Im, Ji-Seong Doh, Sung-Eun Yu, Dae-Wook Kim, Young-Kwan Park, Jeong-Taek Kong, CAE

2.30PM
2C.3
The Statistics of Device Variations and Its Impact on SRAM Bitcell Performance, Leakage and Stability
Ramnath Venkatraman, Ruggero Castagnetti, Shiva Ramesh, LSI Logic Corporation

2.45PM
2C.4
A simulation-based soft error estimation methodology for computer systems
Makoto Sugihara[1], Tohru Ishihara[2], Koji Hashimoto[3], Masanori Muroyama[2], [1]ISIT, [2]Kyushu Univ., [3]Fukuoka Univ.

3.00PM
2C.5
SRAM Local Bit line Access Failure Analyses
Praveen Elakkumanan[1], Jente B Kuang[2], Kevin Nowka[2], Ramalingam Sridhar[1], Rouwaida Kanj[2], Sani Nassif[2], [1]University at Buffalo (SUNY), [2]IBM

3.15PM
2C.6
Impact of NBTI on SRAM Read Stability and Design for Reliability
Sanjay V. Kumar, Chris H. Kim, Sachin S. Sapatnekar, University of Minnesota

SESSION 2D

Siskiyou-Cascade
Tuesday March 28
1.00PM - 5.30PM

Poster Session

Chair: **Tanay Karnik**, Intel
CoChair: **Charlie Chung Ping Chen**, University of Wisconsin-Madison

Track: EDA

2D.1
Minimizing FPGA Reconfiguration Data at Logic Level
Krishna Raghuraman, Haibo Wang, Spyros Tragoudas, Southern Illinois University Carbondale

2D.2
Structure Synthesis of Analog and Mixed-Signal Circuits using Partition Techniques
Kaiping Zeng, Sorin A. Huss, Integrated Circuits and Systems Laboratory

2D.3
Language-Based High Level Transaction Extraction on On-chip Buses
Yi-Le Huang[1], Chun-Yao Wang[1], Richard Yeh[2], Shih-Chieh Chang[1], Yung-Chih Chen[1], [1]National Tsing Hua University, [2]SPRINGSOFT, INC.

Track: DFMQ

2D.4
Clock Skew Scheduling Under Process Variations
Xinjie Wei, Yici Cai, Xianlong Hong, Tsinghua University

2D.5
A CMOS Thermal Sensor and Its Applications in Temperature Adaptive Design
Qikai Chen, Mesut Meterelliyoz, Kaushik Roy, Purdue University

2D.6
Monte Carlo-Alternative Probabilistic Simulations for Analog Systems
Rasit Onur Topaloglu, UC San Diego

2D.7
Critical Path Analysis Considering Temperature, Power Supply Variations and Temperature Induced Leakage
Peng Li, Texas A&M University

2D.8
Process Window and Device Variations Evaluation using Array-Based Characterization Circuits
C. Tabery, M. Craig, G. Burbach, B. Wagner, S. McGowan, P. Etter, S. Roling, C. Haidinyak, E. Ehrichs, AMD

Track: PDI

2D.9
Novel Decoupling Capacitor Designs for sub- 90nm CMOS Technology
Xiongfei Meng[1], Karim Arabi[2], Resve Saleh[1], [1]University of British Columbia, [2]PMC-Sierra

2D.10
Localized On-Chip Power Delivery Network Optimization via Sequence of Linear Programming
Jeffrey Fan[1], I-Fan Liao[1], Sheldon X.-D. Tan[1], Yici Cai[2], Xianlong Hong[2], [1]University of California, Riverside,[2]Tsinghua University, Beijing, China

2D.11
Non-Physical Pseudo-Wave-Based Modal Decoupling Technique of Multi-Coupled Co-Planar Transmission Lines with Homogeneous Dielectric Media
Seongkyun Shin, Yungseon Eo, Hanyang University, Ansan

2D.12
Enhancement of Signal Integrity and Power Integrity with Embedded Capacitors in High-Speed Packages
K. Srinivasan, P. Muthana, R. Mandrekar, E. Engin, J. Choi, M. Swaminathan, Georgia Institute of Technology

2D.13
An Improved AMG-based Method for Fast Power Grid Analysis
Cheng Zhuo[1], Jiang Hu[2], Kangsheng Chen[1], [1]Zhejiang University, [2]Texas A&M University

Track: DFVT

2D.14
Formal Verification of Pipelined Microprocessors with Delayed Branches
Miroslav N. Velev, Consultant

2D.15
Power-Aware Test Pattern Generation for Improved Concurrency at the Core Level *Arkan Abdulrahman, Spyros Tragoudas, Southern Illinois University*

Track: RDIC

2D.16
Advances in Computation of the Maximum of a Set of Random Variables
Debjit Sinha[1], Hai Zhou[1], Narendra V Shenoy[2], [1]Northwestern University, [2]Synopsys

2D.17
A Low-Leakage High-Speed Monotonic Static CMOS 64b Adder in a Dual Gate Oxide 65-nm CMOS Technology
Ali Bastani, Charles A. Zukowski, Columbia University

2D.18
Leakage Biased Sleep Switch Domino Logic
Zhiyu Liu, Volkan Kursun, University of Wisconsin at Madison

Track: TRD

2D.19
Improvements to CBCM (Charge Based Capacitance Measurement) for Deep Submicron CMOS Technology
Randy Bach, Bob Davis, Rich Laubhan, LSI Logic

2D.20
Design of a Single Event Upset (SEU) Mitigation Technique for Programmable Devices
S. Baloch, T. Arslan, A. Storca, Edinburgh University

Track: PDM

2D.21
Area Efficient Temporal Coding Schemes for Reducing Crosstalk Effects
Jean-Marc Philippe, Sébastien Pillement, Olivier Sentieys, IRISA/University of Rennes

2D.22
Processing Rate Optimization by Sequential System Floorplanning
Jia Wang[1], Ping-Chih Wu[2], Hai Zhou[1], [1]Northwestern University, [2]Cadence Design Systems

Track: SDM

2D.23
Fast Pattern Matching with Don't Cares
Zile Wei, Donald Chai, Andreas Kuehlmann, A. Richard Newton, UC Berkeley

2D.24
A Methodology for Layout Aware Design and Optimization of Custom Network-on-Chip Architectures
Krishnan Srinivasan, Karam S. Chatha, Arizona State University

2D.25
Core Network Interface Architecture and Latency Constrained On-Chip Communication
Praveen S. Bhojwani, Rabi N. Mahapatra, Texas A&M University

2D.26
Design Space Exploration of RTL Datapaths Using Rent Parameter based Stochastic Wirelength Estimation
Vyas Krishnan, Srinivas Katkoori, University of South Florida

2D.27
Equivalence Checking of C Programs by Locally Performing Symbolic Simulation on Dependence Graphs
Takeshi Matsumoto[1], Hiroshi Saito[2], Masahiro Fujita[1], [1]University of Tokyo, [2]University of Aizu

2D.28
System-level process variability compensation on memory organizations of dynamic applications: a case study
Concepcion Sanz Pineda[1], Antonis Papanikolaou[2], Manuel Prieto Matias[1], Miguel Miranda[2], Francky Catthoor[2], [1]Complutense University, [2]IMEC

2D.29
A Low Input, Low-Power Dissipation CMOS ADC
Biye Wang, Lili He, and Morris Jones, San Jose State University

2D.30
Constant Impedance Scaling Paradigm for Scaling LC transmission lines
J.Balachandran[1], S.Brebels[1], G.Carchon[1], M.Kuijk[2], W.De Raedt[1], B.Nauwelaers[3], E.Beyne[1], [1]IMEC, [2]Vrije Universiteit Brussel, [3]Katholieke Universiteit Leuven

2D.31
Quasi-One-Step Gauss-Jacobi Method for Large-Scale Interconnect Analysis via RLCG-MNA Formulation
Yuichi Tanji[1], Takayuki Watanabe[2], Hidemasa Kubota[3], Hideki Asai[3], [1]Kagawa University, [2]University of Shizuoka, [3]Shizuoka University

SESSION 3A

San Carlos Room
Tuesday March 28
3.45PM - 5.45PM

Interconnect Analysis and Optimization

Chair: **Farzan Fallah**, Fujitsu Labs
CoChair: **Sarma Vrudhula**, University of Arizona

Summary:
This session presents new techniques for low power signal prorogation by pulse signaling for global buses and for new encoding scheme for power efficient serial link bus. An efficient model order reduction technique for multiple-port interconnects, interconnects transmission capacity estimation method and a new signal integrity analysis method for coupled RLC interconnects are also addressed.

3.45PM
3A.1
Analysis of Pulse Signaling for Low-Power On-Chip Global Bus Design
Min Chen, Yu Cao, Arizona State University

4.15PM
3A.2
Information Theoretic Capacity of Long On-chip Interconnects in the Presence of Crosstalk
Rohit Singhal, Gwan Choi, Rabi N. Mahapatra, Texas A&M University

4.45PM
3A.3
Compact Reduced Order Modeling for Multiple-Port Interconnects
Pu Liu[1], Sheldon X. -D. Tan[1], Bruce McGaughy[2], Lifeng Wu[2], [1]University of California, Riverside; [2]Cadence Design Systems

5.15PM
3A.4
Efficient Signal Integrity Verification Method of Multi-Coupled RLC Interconnect Lines with Asynchronous Circuit Switching
Teayong Je, Yungseon Eo, Hanyang University

5.30PM
3A.5
Reducing the Data Switching Activity on Serial Link Buses
Maged Ghoneima[1], Yehea Ismail[1], Muhammad Khellah[2], Vivek De[2], [1]Northwestern University, [2]Intel

SESSION 3B
San Juan Room
Tuesday March 28
3.45PM - 5.45PM

Digital Test and Diagnosis Techniques

Chair: **Sreejit Chakravarty**, Intel
CoChair: **Miroslav Velev**, Carnegie Mellon University

Summary:
This session is devoted to techniques that deal with digital test issues. The first paper proposes a new test set embedding method with reseeding for scan-based testing and a cost metric for assessing the quality of the test results. The second paper presents two new fault collapsing methods for single stuck-at fault collapsing to reduce the number of tests required for fault diagnosis. The third paper discusses the potential of applying Integer Linear Programming to optimize N-detect test set. The fourth paper present an approach to simultaneously minimizing power and routing cost in scan chain reordering after cell placement and formulates problem as a Traveling Salesman Problem. The fifth paper demonstrates the use of linear dependency relationships among path delay faults as an effective way to determine circuit-timing characteristics. The last paper presents a novel approach to perform delay-fault diagnosis for robust as well as non-robust tests.

3.45PM
3B.1
Efficient Multiphase Test Set Embedding for Scan-based Testing
E. Kalligeros[1], X. Kavousianos[2], D. Nikolos[1], [1]University of Patras, [2]University of Ioannina

4.15PM
3B.2
Evaluation of Collapsing Methods for Fault Diagnosis
Rajsekhar Adapa[1], Spyros Tragoudas[1], Maria K. Michael[2], [1]Southern Illinois University, [2]University of Cyprus

4.45PM
3B.3
On N-Detect Pattern Set Optimization
Yu Huang, Mentor Graphics Co.

5.00PM
3B.4
On Optimizing Scan Testing Power and Routing Cost in Scan Chain Design
Li-Chung Hsu, Hung-Ming Chen, National Chiao Tung University, Hsinchu, Taiwan

5.15PM
3B.5
An Improved Method for Identifying Linear Dependencies in Path Delay Faults
E. Flanigan, T. Haniotakis, S. Tragoudas, Southern Illinois University at Carbondale

5.30PM
3B.6
Delay Fault Diagnosis for Non-Robust Test
Vishal J. Mehta[1], Zhuiyan Wang[2], Malgorzata Marek-Sadowska[1], Kun-Hans Tsai[3], Janusz Rajski[3], [1]UC Santa Barbara, [2]Cisco, [3]Mentor Graphics

SESSION 3C
Monterey Room
Tuesday March 28
3.45PM - 5.45PM

Back of Line DFM

Chair: **Rajendran Panda**, Freescale Semiconductor
CoChair: **Enrico Malavasi**, PDF Solutions

Summary:
This session presents 5 papers addressing manufacturability metrics and yield enhancements in the layout of CMOS integrated circuits. As lithographical features scale down to the nanometer range, CMOS design needs to fit more and more complex requirements in order to be manufacturable with acceptable yields. Intellectual Property (IP) components require adequate characterization, and the design to process interaction needs to be modeled to represent adequately the impact of layout features and process variability on performance metrics.

3.45PM
3C.1
Yield Improvement by Local Wiring Redundancy
Jeanne Bickford[1], Markus Buehler[1], Jason Hibbeler[1], Juergen Koehl[1], Dirk Mueller[2], Sven Peyer[2], Christian Schulte[2], [1]IBM, [2]Bonn University

4.15PM
3C.2
Via Distribution Model for Yield Estimation
Takumi Uezono, Kenichi Okada, Kazuya Masu, Tokyo Institute of Technology

4.45PM
3C.3
The Use of the Manufacturing Sensitivity Model Forms to Comprehend Layout Manufacturing Robustness For Use During Device Design
Lawrence S. Melvin III, Daniel N. Zhang, Kirk J. Strozewski, Skye Wolfer, Synopsys

5.00PM
3C.4
DFM Metrics for Standard Cells
Robert Aitken, ARM

5.15PM
3C.5
Yield Enhancement Methodology for CMOS Standard Cells
Arnaud Epinat[1], N.Vijayaraghavan[2], Matthieu Sautier[1], Olivier Callen[1], Sebastien Fabre[3], Ryan Ross[4], Paul Simon[3], Robin Wilson1, [1]ST Microelectronics, Crolles, France; [2]ST Microelectronics, Noida, India; [3]Phillips Semiconductor, Crolles, France; [4]Freescale Semiconductor, Crolles, France

5.30PM
3C.6
Dummy-Gate Structure to Improve ESD Robustness in a Fully-Salicided 130-nm CMOS Technology without Using Extra Salicide-Blocking Mask
Hsin-Chyh Hsu[1], Ming-Dou Ker[2], [1]Industrial Technology Research Institute, [2]National Chiao-Tung University

Session EP2
Panel Discussion & Dinner
Sponsored By Mentor Graphics & LSI Logic*

Donner Pass Room
6:30 -8:30PM

Soft IP Quality:
Who is really responsible for quality throughout the design process?

Panel Organizer: ***David Overhauser***
Panel Moderator: ***Ron Wilson,*** *EDN Magazine*

From development through manufacturing an IP core undergoes many different stages that can affect the overall quality and characteristics of the core. When a project is slowed or halted because of a problem with the IP core then who is responsible? Is it the IP provider who provided a core that worked at delivery, the integrator that made changes as necessary or perhaps the manufacturer? This panel will explore the many possible causes of problems with an IP core, but more importantly it will examine what is being done to minimize the risk associated with third party IP and who is responsible.

Panelists:
Gary Delp*, LSI Logic Distinguished Engineer; VSIA, CTO*
Bill Martin*, Mentor Graphics Corporation - General Manager, Intellectual Property Division*
Naveed Sherwani*, President, Open-Silicon*
Guri Stark*, VP of Marketing, Solutions Group, Synopsys*
John Goodenough*, Director of Design Technology, ARM*

* *With special thanks to Hillary Cain, Cain Communications*

Plenary Session 2P
Donner Pass Room
Wednesday March 29
8:30AM - 10:15AM

Co-Chairs:
Lech Jozwiak
Eindhoven University of Technology, The Netherlands

George Alexiou
University of Patras and Computer Technology Institute, Patras, Greece

8:30am
Introduction & Announcements

8:45am
2P.1
Adding Manufacturability to the Quality of Results

Dr. Raul Camposano
Sr. VP, GM and CTO
Synopsys

Quality has many definitions. Conformance to specifications; Customer Satisfaction; Delivery divided by Expectations; etc. EDA's sense of quality is determined by what it's customers want. Do we have a virtuous cycle in the quality relationship between EDA and its customers? EDA is also the quality tools supplier to help the Electronics Systems and semiconductor companies to produce quality products on time. The speaker will examine both aspects of the quality issue from an EDA perspective.

9:15am
2P.2
Future Memory Technology Trends and Challenges

Dr. Changhyun Kim
Fellow
Samsung

As memory market enters the Gigabit and GHz range with consumers demanding ever higher performance and diversified applications, new types of devices are being developed in order to keep up with the scaling requirements for cost reduction. Among these devices are well-known ones such as the recessed channel transistors, but also FinFET and vertically stacked transistors for DRAM and charge trap devices for Flash memory. The latter ones are still not at a manufacturable stage yet. Even more exotic memories implement new materials and stacked architectures on the cell, chip and package level. On the performance side, increasing speeds require higher time resolutions. The future difficulties of process control by far exceed those of conventional planar devices. Therefore device characteristics are expected to show ever increasing PVT variations. As these variations become more and more inevitable, especially as dimensions approach the atomic scale, negative effects on circuit and device performances have to be prevented by new, appropriate methods of 3D device modeling and circuit design which consider the mentioned parameter variations. In this talk such challenges will be discussed as well as some approaches to overcome them. An outlook will also be given about the memory technology trends in the next decades.

9:45am
2P.3
Device and Technology Challenges for Nanoscale CMOS

Dr. H.-S. Philip Wong
Center for Integrated Systems and Department of Electrical Engineering
Stanford University

With the introduction of 90 nm node technology, silicon CMOS is already at the nanoscale. There is no doubt that the semiconductor industry desires to stay on the historical rate of cost/performance/density improvement as exemplified by the International Technology Roadmap for Semiconductors (ITRS). The challenges for continued device scaling are daunting. At the highest level, the challenges are: (1) delivering cost/performance improvement while at the same time containing power consumption/dissipation, (2) control of device variations, and (3) device/circuit/system co-design and integration. New devices and new materials offer new opportunities for solving the challenges of continued improvement. In this talk, we give an overview of the device options being considered for CMOS logic technologies from 45 nm to 22 nm and beyond. Technology options include the use of device structures (multi-gate FET) and transport-enhanced channel materials (strained Si, Ge). Beyond the 22 nm node, research are underway to explore even more adventurous options such as III-V compound semiconductors as channel materials, metal Schottky source/drain. Beyond that time horizon, there is the question of whether new materials and fabrication methods such as carbon nanotubes, semiconductor nanowires and self-assembly techniques will make an impact in nanoscale CMOS technologies. We survey the state-of-the-art of these emerging devices and technologies and discuss the research opportunities going forward. We conclude with a discussion of the interaction between device design and the circuit/system architecture and how this interaction will change the landscape of technology development in the future.

SESSION 4A
San Carlos Room
Wednesday March 29
10.30AM - 12.30PM

Analog Test and Self-Checking Design

Chair: **George Alexiou**, University of Patras
CoChair: **Spyros Tragoudas**, Southern Illinois University

Summary:
This session focuses on analog and mixed-signal test as well as on self-checking design techniques. The first paper proposes a self-checking design architecture to implement advanced encryption standard. The second paper applies time lag correlation to extract various kinds of jitter for bit error rate estimation. The third paper investigates the impact of window comparator threshold variations on the performance of integrator-based programmable capacitor array testing circuits. The fourth paper presents the results of an intensive investigation of a new so-called polynomial fitting method for built-in ADC testing. The last paper is an exploratory study on the ability of Oscillation-Based Test for testing continuous-time low-pass ladder filters.

10.30AM
4A.1
A Totally Self-Checking S-box Architecture for the Advanced Encryption Standard *Adam K. Matthews, Parag K. Lala, University of Arkansas*

11.00AM
4A.2
Jitter Decomposition by Time Lag Correlation
Qingqi Dou, Jacob A. Abraham, University of Texas at Austin

11.30AM
4A.3
Design of Window Comparators for Integrator-Based Capacitor Array Testing Circuits
Amit Laknaur, Haibo Wang, Southern Illinois University

12.00noon
4A.4
Analysis and experimental results of an FPGA-based strategy for fast production test of high resolution ADCs
Daniela De Venuto, Leonardo Reyneri, Politecnico di Bari, Italy

12.15PM
4A.5
Exploring the Ability of Oscillation Based Test for Testing Continuous -Time Ladder Filters
J.L Catalano[1], G. Peretti[1], E. Romero[1], C. Marqués[2], [1]Universidad Tecnológica Nacional Fac. Reg. Villa María, [2]Universidad Nacional de Córdoba, Facultad de Matemática, Astronomía y Física

SESSION 4B

San Juan Room

Wednesday March 29
10.30AM - 12.30PM

Power Aware Designs and Memory Management

Chair: **Lech Jozwiak**, Eindhoven University of Technology
CoChair: **Artur Chojnacki**, PDF Solutions

Summary:
The recent spectacular progress in modern microelectronics that enabled implementation of a complete complex system on a single chip created new important opportunities, but also new serious difficulties due to unusual silicon and system complexity. In particular, huge numbers, high density and small dimensions of devices and interconnections, as well as, huge length of interconnections result in power and energy crisis, increased leakage power, and fluctuations in the on-chip power density distribution. This session reports recent work on important aspects of the system-level power aware design and memory management. It discusses such important issues as parameterizable architecture-level SRAM power model, data replication in DRAMs for reducing energy, scratch-pad memory space management, various techniques for gate leakage reduction, and compiler-directed power density reduction in NoC-based multi-core designs.

10.30AM
4B.1
Data Replication in Banked DRAMs for Reducing Energy Consumption
Ozcan Ozturk, Mahmut Kandemir, Pennsylvania State University

11.00AM
4B.2
Parameterizable Architecture-Level SRAM Power Model Using Circuit-Simulation Backend for Leakage Calibration
Minh Q. Do, Mindaugas Drazdziulis, Per Larsson-Edefors, Lars Bengtsson, Chalmers University of Technology

11.30AM
4B.3
Dual-K Versus Dual-T Technique for Gate Leakage Reduction: A Comparative Perspective
Saraju P. Mohanty, Ramakrishna Velagapudi, Elias Kougianos, University of North Texas

12noon
4B.4
Compiler-Directed Power Density Reduction in NoC-Based Multi-Core Designs
Sri Hari Krishna Narayanan, Mahmut Kandemir, Ozcan Ozturk, Pennsylvania State University

12.15PM
4B.5
Shared Scratch-Pad Memory Space Management
Ozcan Ozturk[1], Mahmut Kandemir[1], Ibrahim Kolcu[2], [1]Pennsylvania State University, [2]UMIST

SESSION 4C
Monterey Room
Wednesday March 29
10.30AM - 12.30PM

Technologies for Robust Design

Chair: **Ming Dou Ker**, National Chiao Tung University
CoChair: **Paul Tong**, Pericom

Summary:
The papers selected in this Session report recent works on the Effect of Technology on IC Design, Performance, Reliability, and Yield. The first paper provides a predictive MOSFET model for circuit design in CMOS processes from 130nm to 32nm technology nodes. The second paper reports a scalable non-volatile embedded memory cell and technology with high reliability and high data retention. The third paper uses the long-pulse transmission line pulsing system to investigate the robustness of CMOS devices under cable discharge event. The fourth paper analyzes the effect of manufacturing process variations on the SRAM stability in the read operation. The fifth paper provides a flip flop sizing scheme to efficiently immunize combinational logic circuits from the effects of radiation induced single event transients (SET). The sixth paper presents a single event transients (SET) mitigation scheme for flip-flops based on the time redundancy principle.

10.30AM
4C.1
New Generation of Predictive Technology Model for Sub-45nm Design Exploration *Wei Zhao, Yu Cao, Arizona State University*

11.00AM
4C.2
A Non-volatile Embedded Memory for high temperature Automotive and High-Retention applications
Mammen Thomas[1], Jagdish Pathak[1], Jim Payne[1], Friedrich Leisenberger[2], Ewald Wachmann[2], Gregor Schatzberger[2], Andreas Wiesner[2], Martin Schrems[2], [1]MEMTEK, LLC., [2]austriamicrosystems AG

11.30AM
4C.3
Method to Evaluate Cable Discharge Event (CDE) Reliability of Integrated Circuits in CMOS Technology
Tai-Xiang Lai, Ming-Dou Ker, National Chiao-Tung University

11.45AM
4C.4
Analysis of Process Variation's Effect on SRAM's read stability
Chung-Kuan Tsai, Malgorzata Marek-Sadowska, UC Santa Barbara

12noon
4C.5
Logic SER Reduction through Flipflop Redesign
Vivek Joshi[1], Rajeev R. Rao[2], David Blaauw[2], Dennis Sylvester[2], [1]Indian Institute of Technology, Kanpur, India; [2]University of Michigan, Ann Arbor, MI

12.15PM
4C.6
Time Redundancy Based Scan Flip-Flop Reuse To Reduce SER Of Combinational Logic *Praveen Elakkumanan, Kishan Prasad, Ramalingam Sridhar, University at Buffalo (SUNY)*

SESSION 5A
San Carlos Room
Wednesday March 29
1.45PM - 3.15PM

IC-Package Design Challenges

Chair: **Lalitha Immaneni**, Intel
Co-Chair: **Jaijeet Roychowdhury**, University of Minnesota

Summary:
The papers in this session report recent work on important aspects of power delivery and thermal management. The first paper provides an overview of thermal issues in nanoscale technologies. The second paper extends moment matching methods for fast power grid analysis to handle stochastic variations. The third paper provides a thermal analysis method for materials with nonlinear thermal conductivities. The fourth paper proposes a switched-capacitor-based voltage regulator for power grids that, together with external capacitors, result in considerable improvements in power quality. Forth paper proposes a switched-capacitor-based voltage regulator for power grids that, together with external capacitors, result in considerable improvements in power quality. The final paper proposes a novel methodology for optimizing power savings that uses partial sleep states to smoothly trade off wake-up power penalty against leakage power.

1.45PM
5A.1
Thermal Trends in Emerging Technologies
G. M. Link, N. Vijaykrishnan, Pennsylvania State University

2.15PM
5A.2
Power Gating with Multiple Sleep Modes
Kanak Agarwal[1], Harmander Deogun[2], Dennis Sylvester[2], Kevin Nowka[1], [1]IBM, [2]University of Michigan

2.30PM
5A.3
SMM: Scalable Analysis of Power Delivery Networks by Stochastic Moment Matching *Andrew Kahng, Bao Liu, Sheldon Tan, UC San Diego*

2.45PM
5A.4
Accurate Thermal Analysis Considering Nonlinear Thermal Conductivity
Anand Ramalingam[1], Frank Liu[2], Sani R. Nassif[3], David Z. Pan[1], [1]University of Texas at Austin, [2]ARL, [3]IBM

3.00PM
5A.5
Minimizing Ohmic Loss in Future Processor IR Events
Mark Budnik, Kaushik Roy, Purdue University

SESSION 5B
San Juan Room
Wednesday March 29
1.45PM - 3.15PM

IP, Interoperability: design Optimization

Chair: **James Lei**, Altera
CoChair: **Tom Chen**, Colorado State University

Summary:
Interoperability among EDA tools has become a critical productivity issue. Many standards have been created to address this critical issue. Some aspects of these standards also facilitate IP protection. Three papers in this session deal with using standards for improving productivity and IP protection. The other two papers address design optimization techniques for complex cell design.

1.45PM
5B.1
GmTest: An Industry-Wide Database of Layouts for Quality Control
Anand P Kulkarni, Thomas J Grebinski; OASIS Tooling, Alamo, California

2.15PM
5B.2
ConvexSmooth: A simultaneous convex fitting and smoothing algorithm for convex optimization problems
Sanghamitra Roy, Charlie Chung-Ping Chen, University of Wisconsin at Madison

2.30PM
5B.3
A Watermarking System for IP Protection by Buffer Insertion Technique
Guangyu Sun, Zhiqiang Gao, Yi Xu, Tsinghua University

2.45PM
5B.4
Partial Selective Encryption: An Improved System for Protecting VLSI Design Data in the OASIS format
Anand P Kulkarni, Thomas J Grebinski, OASIS Tooling, Alamo, California

3.00PM
5B.5
Transistor-Level Optimization of Supergates
Dimitris Kagaris, Themistoklis Haniotakis, Southern Illinois University

SESSION 5C
Monterey Room
Wednesday March 29
1.45PM - 3.15PM

DSM Interconnect Challenges

Chair: **Hardy Leung**, Magma Design Automation
CoChair: **Rajeev Murgai**, Fujitsu Labs of America

Summary:
This session addresses some challenging problems pertaining to interconnect in deep sub-micron (DSM) technologies. The first paper studies the impact of floating fills on interconnect capacitance. The second paper presents challenges related with parasitic extraction in DSM technologies. The last two papers describe novel methods for inductance estimation and extraction respectively.

1.45PM
5C.1
Study of Floating Fill Impact on Interconnect Capacitance
Andrew B. Kahng, Kambiz Samadi, Puneet Sharma, UC San Diego

2.15PM
5C.2
The Challenges of Parasitic Extraction at 65 nm
Karen Chow, Mentor Graphics Co.

2.45PM
5C.3
Pre-Layout Inductive Corners for Advanced Digital Design Interconnect: Modeling and Silicon Validation
Lauréline David[1], Stéphane Martin[1], Corinne Crégut[1], Eric Balossier[1], Fabrice Huret[2], Frédéric Nyer[1], [1]STMicroelectronics, [2]LEST

3.00PM
5C.4
A Mixed Boundary Element Method for Extracting Frequency-Dependent Inductances of 3D Interconnects
Changhao Yan, Wenjian Yu, Zeyi Wang, Tsinghua University, Beijing

SESSION 6A

San Carlos Room

Wednesday March 29
3.30PM - 5.30PM

Leakage Analysis and Optimization

Chair: **Syed Alam**, Freescale Semiconductor
CoChair: **Volkan Kursun**, University of Wisconsin - Madison

Summary:
This session presents various methods for reducing the leakage powers of deep sub-micro chips. The proposed techniques range from leakage reduction under process variations, efficient sleep transistor insertion method during placement, low leakage SRAM design exploiting timing delays, low leakage FPGA architecture use dual-Vt logics, optimization method to reduce the impacts of sleep transistors, and analysis of gate-length basing effects for better threshold voltage selection.

3.30PM
6A.1
LOTUS: Leakage Optimization under Timing Uncertainty for Standard-cell designs *Sarvesh Bhardwaj, Sarma Vrudhula, Yu Cao, Arizona State University*

4.00PM
6A.2
Simultaneous Fine-grain Sleep Transistor Placement and Sizing for Leakage Optimization
Wang Yu, Lin Hai, Yang Huazhong, Luo Rong, Wang Hui, Tsinghua University

4.30PM
6A.3
Low-leakage SRAM Design with Dual Vt Transistors
Behnam Amelifard[1], Farzan Fallah[2], Massoud Pedram[1], [1]University of Southern California, [2]Fujitsu Labs of America

4.45PM
6A.4
Dual-Vt Design of FPGAs for Subthreshold Leakage Tolerance
Akhilesh Kumar, Mohab Anis, University of Waterloo

5.00PM
6A.5
Gate Sizing and Replication to Minimize the Effects of Virtual Ground Parasitic Resistances in MTCMOS Designs
Chanseok Hwang, Changwoo Kang, Massoud Pedram, University of Southern California

5.15PM
6A.6
Impact of Gate-Length Biasing on Threshold-Voltage Selection
Andrew B. Kahng, Swamy Muddu, Puneet Sharma, UC San Diego

SESSION 6B

San Juan Room

Wednesday March 29

3.30PM - 5.30PM

System Level Designs and Reliability Models

Chair: **Lech Jozwiak**, Eindhoven University of Technology
CoChair: **Antonio Nunez**, University of Las Palmas GC

Summary:
Due to the rapidly growing silicon and system complexity, both the hardware and software of the future chips tends inherently to be less reliable and more sensitive to noise and interferences with the environment. However, we certainly cannot tolerate that the future systems will be less reliable, because our life is to a higher and higher degree dependent on their adequate operation. In consequence, the system responsiveness, robustness and dependability are becoming more and more critical. This session reports recent important work on the system-level reliability models and design methodology. It discusses such important issues as error susceptibility modeling and analysis, diagnosis and design for diagnosability, system-level design methodologies enabling quality and predictability.

3.30PM
6B.1
FASER: Fast Analysis of Soft Error Susceptibility for Cell-Based Designs
Bin Zhang, Wei-shen Wang, Michael Orshansky, University of Texas at Austin

4.00PM
6B.2
Diagnosis and Design for Diagnosability for Internet Routers
Lee Barford, Agilent Laboratories

4.30PM
6B.3
Enabling Quality and Schedule Predictability in SoC Design using HandoffQC
Bhaskar J. Karmakar, V. Kalyana Chakravarty, R. Venkatraman, Jagdish C. Rao, Texas Instruments

5.00PM
6B.4
Transaction Level Error Susceptibility Model for Bus-Based SoC Architectures
Ing-Chao Lin, Suresh Srinivasan, Vijay Narayanan, Pennsylvania State University

5.15PM
6B.5
System-Level Design Methodology with Direct Execution For Multiprocessors on SoPC
Riad Benmouhoub, Omar Hammami, ENSTA

SESSION 6C

Monterey Room

Wednesday March 29

3.30PM - 5.30PM

Modeling for DFM

Chair: **Dave Overhauser**, Cadence
CoChair: **Kanak Agarwal**, IBM

Summary:
Design for Manufacturing (DFM) relies heavily on a deep understanding of technology variability and its impact on circuit performance. The papers in this session represent a variety of approaches for the generation, use, and quality evaluation of DFM related models. The models range from physical level models for device stress and lithography, through back end issues such as via variations and the impact of layout variation on cross-talk, and finally at the highest levels where basic methodological questions are asked.

3.30PM
6C.1
Question: DRC or DfM ? Answer: FMEA and ROI
Artur Balasinski, Cypress Semiconductor

4.00PM
6C.2
Statistical Analysis of Capacitance Coupling Effects on Delay and Noise
Usha Narasimha, Texas Instruments

4.30PM
6C.3
Bringing Manufacturing into Design via Process-Dependent SPICE Models
Sridhar Tirumala, Yuri Mahotin, Xi-Wei Lin, Victor Moroz, Lee Smith, S. Krishnamurthy, Li Benhaldt, Dipu Pramanik, Synopsys Inc

5.00PM
6C.4
Stress-Aware Design Methodology
Victor Moroz, Lee Smith, Xi-Wei Lin, Dipu Pramanik, Greg Rollins, Synopsys

5.15PM
6C.5
A DFM Methodology to Evaluate the Impact of Lithography Conditions on the Speed of Critical Paths in a VLSI Circuit
Peter Wright, Minghui Fan, Synopsys