ISQED'07 Tutorials

TUTORIAL I
Monday, March 26, 2007
9:00am-12:30pm

Sub-45nm Technology and design challenges

Chair & Moderator:
Rajiv Joshi, *IBM T J Watson Research Center, NY*

Presenters:
Gerhard Knoblinger, *Infineon Technologies*
James W. Tschanz, *Intel*
Marcal Pol, *IMEC*

Multi-Gate MOSFET Design

Presenter:
Gerhard Knoblinger, *Infineon Technologies*

Multi-Gate Field Effect Transistors (MuGFET) such as FinFETs and Triple-Gate FETs are the most promising device structures for sub-45nm CMOS technology nodes.The superior control of the channel due to multiple gates reduces short-channel effects and leakage currents.This opens the opportunity for further down scaling of the threshold and supply voltages and device performance improvements. Circuit performance also benefits from novel gate stack materials, reduced parasitic capacitances, and hole mobility improvement. For future SoC solutions in these advanced technologies, the ability to realize also analog building blocks is of utmost importance. In this tutorial, circuit design issues of emerging multi-gate field effect transistors will be discussed with special emphasis on the link between circuit design and technology.The tutorial will start with CMOS scaling trends, followed by an example for a typical MuGFET technology and an overview of the available devices. Reliable and accurate compact models for MuGFET devices, including new device specific effects are an important prerequisite for successful circuit design. So the second part will cover compact modeling of MuGFET devices with special emphasis on self heating effects. We will then discuss the impact of different technology options on the performance of digital circuits.The influence of novel midgap gate electrode materials on digital circuits will be presented.To compare different technology options, ring oscillator circuits are first realized with double gate devices using conventional body doping and n+/p+ poly-Si gates to define the nMOS/pMOS threshold voltages.To meet the requirements of future low power technologies, these circuits are then fabricated with triple gate devices and single-midgap gate electrodes allowing for enhancement-type devices with undoped bodies. Furthermore the influence of new device specific effects on analog circuits, like self heating or output conductance improvement due to undoped body are discussed and the first analog building blocks realized with MuGFET devices are presented. In addition RF and ESD issues will be discussed and RF circuits realized with MuGFET devices and the most important issues of ESD robustness will be covered.

Sub 45nm Low Power Design Challenges

Presenter:
James W. Tschanz, *Intel*

The ever-increasing use of mobile devices and the constant desire for energy efficiency and long battery life have made low power design more important than ever. At the same time, continued technology scaling results in more devices per die, higher leakage current and power densities, and increased process variations. Advanced low-power design techniques are therefore necessary in order to deal with these challenges and to allow Moore's Law to continue below the 45nm technology node. In order to produce the most energy-efficient design, power must be considered at all stages of the product: in the design of the circuits themselves, after fabrication of the design, and during the actual operation of the part. In this tutorial, we examine low-power design techniques applicable to each of these phases:

- Circuit design: Leakage currents and variations become worse as technology continues to scale. Thus, leakage-tolerant and variation-tolerant circuits are essential for robust operation. We describe several circuit techniques that allow energy-efficient operation in the presence of leakage and variations.

- Post-silicon techniques: Due to process variations, the power consumption and performance of a design can vary widely after fabrication. We will describe post-silicon techniques such as adaptive body bias and adaptive supply voltage which can be used to reduce this variation and improve the parametric yield of the design.

- Dynamic techniques: During normal operation of the design, temperature, voltage, and activity factor can vary based on environmental conditions and the workload of the part. Simply guardbanding these dynamic variations results in a non-optimal design which sacrifices performance, energy, or both. We will describe techniques for sensing these variations and dynamically responding to them, reducing the guardbands required and improving energy efficiency of the part.

Self-adaptive systems to drive out the nano-scale devil

Presenter:
Marcal Pol, *IMEC*

Within 15 years we will reach the ultimate scaling of CMOS. This will enable the billion transistor chips needed for ever more complex ambient intelligent systems providing sense and simplicity to daily life at low cost. Realizing these systems requires coping with the accumulation of nano-scale physical phenomena disturbing the digital abstraction needed for complexity management. In face of these nano-scale challenges, the entire design flow should be re-considered to build energy-efficient systems with performance/throughput guarantees. Rather than taking conservative margins (by worst-case or statistical design techniques), a better approach is to go for design techniques that allow systems to safely operate under uncertainties and that are as energy-delay optimal as possible. We will discuss the issues in building such uncertainty-resilient systems from both a circuit and architectural viewpoint.

TUTORIAL II

1:30pm-5:00pm

Quality driven manufacturing and SOC designs

Chair & Moderator:
Rajiv Joshi, *IBM T J Watson Research Center, NY*

Presenters:
Srikanth Venkataraman, *Intel*
Nagesh Tamarapalli , *AMD*
Dr. Lech Jozwiak, *Eindhoven University of Technology*

DFM, DFY, Debug and Diagnosis: The loop to ensure yield

Presenter:
Srikanth Venkataraman, *Intel*

Semiconductor yield has traditionally been limited by random particle-defect based issues. However, as the feature sizes reduce, systematic mechanism-limited yield loss is a substantial component of yield loss. A key factor is the interaction between design and manufacturing. Yield losses in the newer processes include functional defects, parametric defects and issues with testing. Each of these sources of yield loss needs to be analyzed and understood by designers and tool developers. In addition, new techniques and methods must be devised to minimize the impact of these yield loss mechanisms. After an introduction of the issues involved, Design-for-Manufacturing (DFM) techniques to analyze the design content, flag areas of design that could limit yield, and make changes to improve yield are covered. Test presents an opportunity to close the loop by analyzing silicon failures through diagnosis to determine the features that are actually causing yield loss and their relative impact. The application of statistical diagnosis techniques to determine the features that are actually causing yield loss and their relative impact are covered.

DFT and Test: Ensuring product quality

Presenter:
Nagesh Tamarapalli , *AMD*

In order to be able to diagnose the yield limiting defects it is first necessary to detect them through high quality test patterns. In this part, basics such as scan techniques, Built-In Self-Test (BIST) for random logic and memories, as well as fault modeling that is used to abstract the defects will be covered. Traditionally, tests have been created using the static stuck-at fault model. However, with the increasing occurrence of newer defect mechanisms at current technologies, insuring product quality requires that these traditional stuck-at tests be augmented with at-speed tests. In addition, ways to link DFM techniques to identify the defect-prone regions and actively target them during test pattern generation need to be explored. While the addition of these newer tests result in better quality, the test cost also increases due to the increased tester memory and time required to deliver them. A variety of on-chip hardware based compression techniques that have recently been proposed to insure product quality while maintaining the test cost will also be discussed.

Quality-driven Architecture Synthesis and Power Aware Design of Embedded SoCs

Presenter:
Dr. Lech Jozwiak, *Eindhoven University of Technology*

The recent spectacular progress in modern microelectronics has created ability to implement a complex system on a single chip, and facilitated common global networking and wireless communication. This way, it has generated a strong stimulus for further development of the embedded system area, and specifically, of the embedded SoCs. Many new sorts of highly integrated wireless, mobile and networked systems for known and new important applications are now feasible and affordable. These systems have important applications in virtually all areas of human activity, and can be embedded inside of medical devices, robots, machines, planes, cars etc. or even implanted in human or animal bodies. On the other hand, application of the system-on-a-chip technology means however that different mixtures of non-programmable and programmable (re-configurable) processors, various sorts of memories and communication circuitry, as well as various digital and/or analog circuits are implemented together on a single chip. It also results in more and more severe power and energy problems, and an increasing influence of various physical phenomena on the system's behavior and performance parameters with the progressing miniaturization. Embedded systems are especially difficult to design. In addition to the above listed issues: their design is highly innovative, they must continuously communicate with their surroundings and appropriately react in real-time to the signals from the surrounding when guaranteeing continuous service within the time constraints. They have to satisfy various application-specific constraints and objectives, and many of them are used in critical applications that impose extremely high quality requirements. The main aims of this tutorial are the following:

- to analyze the nature of the modern embedded SoC design problems, and to show which system, design and design automation concepts seem to be adequate to solve the problems,
- to consider the application of these promising concepts to the system-level design of embedded SoCs, when focusing on the quality-driven system-level design exploration, system architecture design, and hardware/software co-design of the heterogeneous hard real-time embedded multi-processor SoCs, and on the EDA-tools supporting these complex design tasks,
- to discusses new quality-driven model-based automatic architecture synthesis methods and corre sponding EDA-tools that enable effective and efficient multi-objective optimal architecture synthe sis for complex hard real-time embedded heterogeneous multi-processor SoCs,
- to overview the power and energy issues in embedded SoCs and techniques to reduce power and energy.