

# The Changing IC Devices

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May 4, 2011 Exclusive News

# The New York Times Front Page

- Intel will use 3D FinFET at 22nm
- Most radical change in 4 decades
- There is a competing SOI technology

The New York Times

Science

WORLD U.S. N.Y. / REGION BUSINESS TECHNOLOGY SCIENCE HEALTH SPORTS OPINION

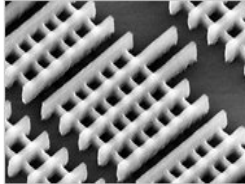
ENVIRONMENT SPACE & COSMOS

## Intel Increases Transistor Speed by Building Upward

By JOHN MARKOFF  
Published: May 4, 2011

HILLSBORO, Ore. — Intel announced on Wednesday that it had again found a way to make computer chips that could process information more quickly and with less power in less space.

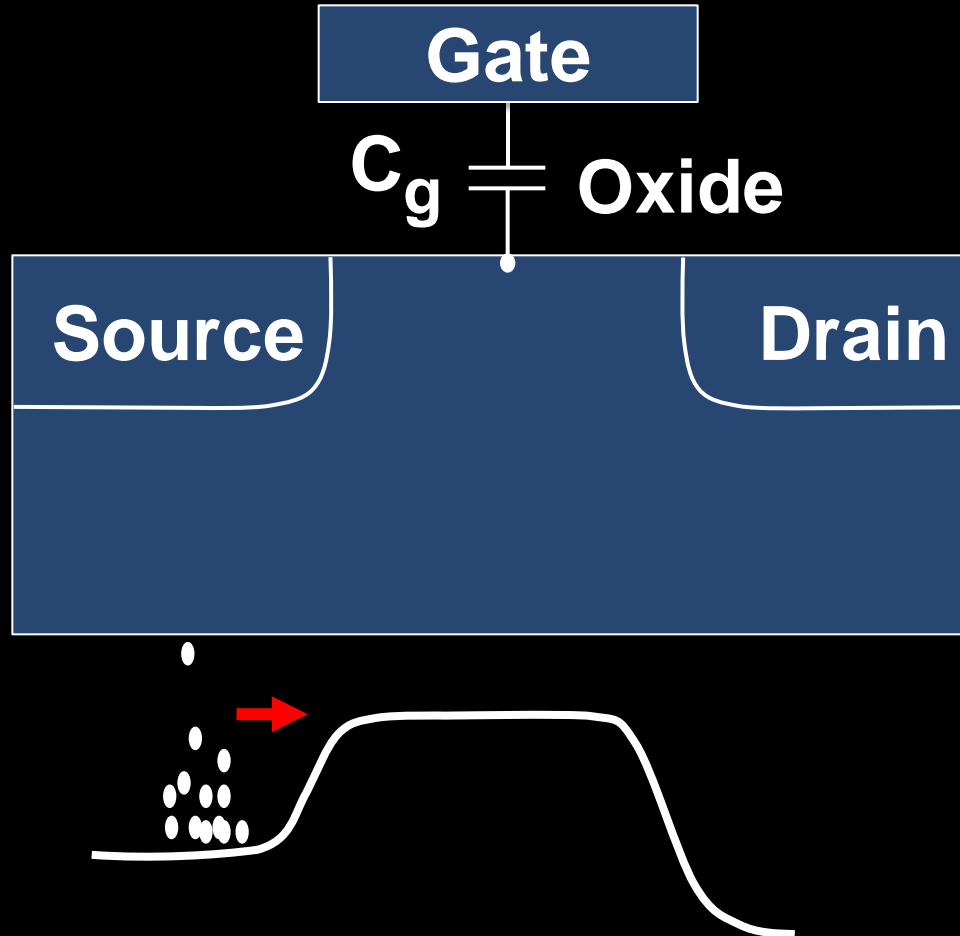
[Enlarge This Image](#)



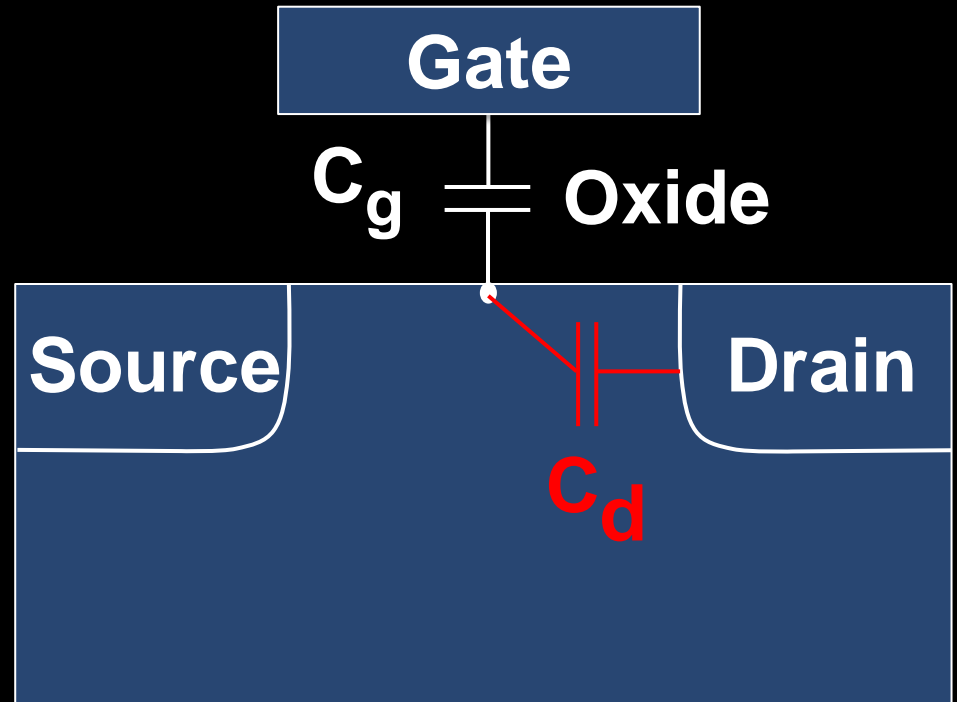
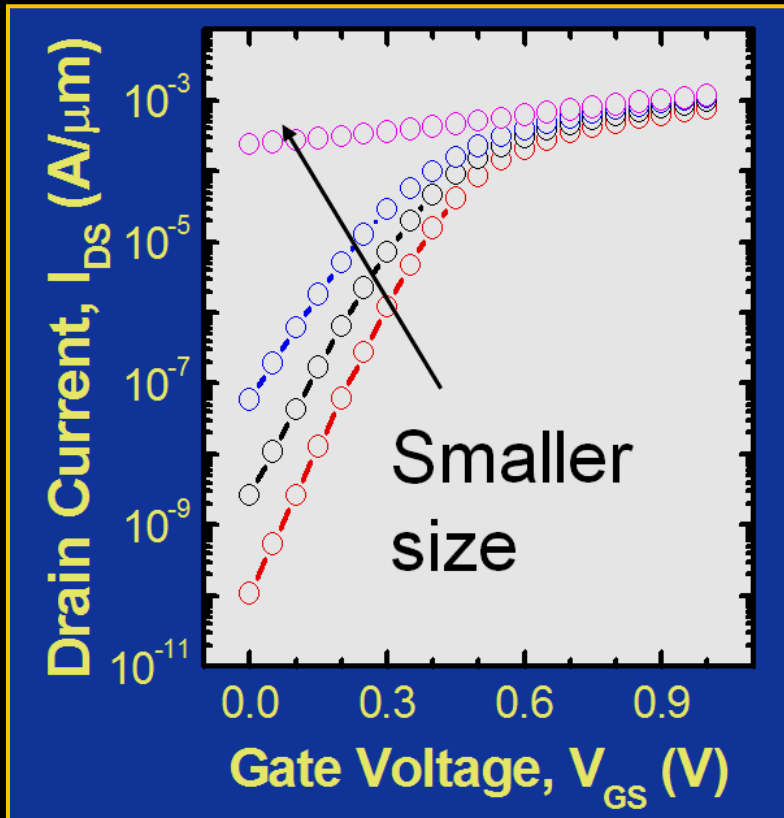
Intel's new transistors have tiny pillars, or fins, that rise above the chip's surface.

The transistors on computer chips — whether for PC's or smartphones — have been designed in essentially the same way since 1959 when Robert Noyce, Intel's co-founder, and Jack Kilby of [Texas Instruments](#) independently invented the first integrated circuits that became the basic building block of electronic devices in the information age.

# Long Channel Transistor

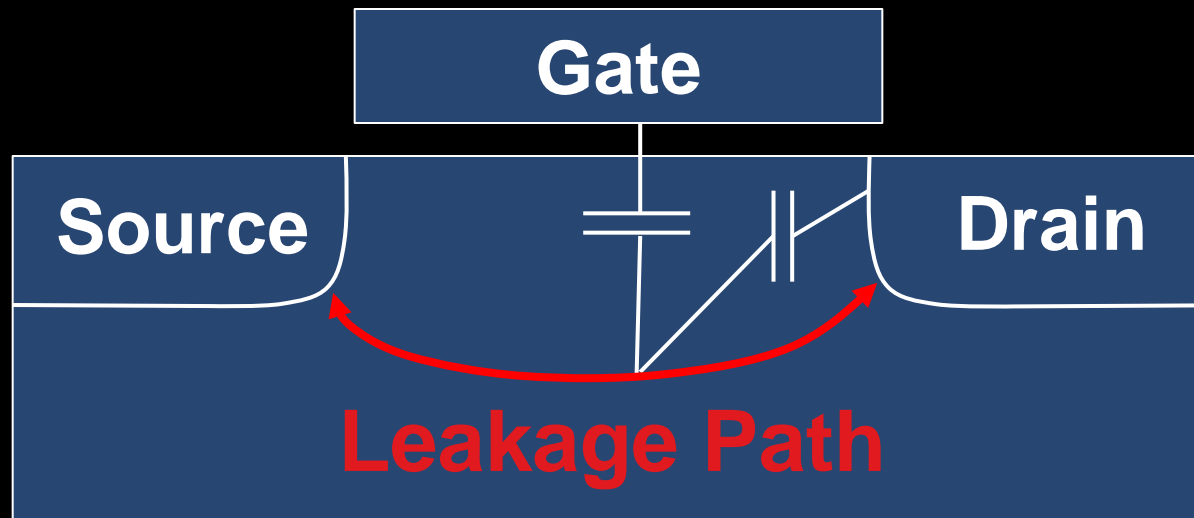


# Short Channel – Problem



**MOSFET becomes “resistor” at small L.**

# Making Oxide Thin is Not Enough

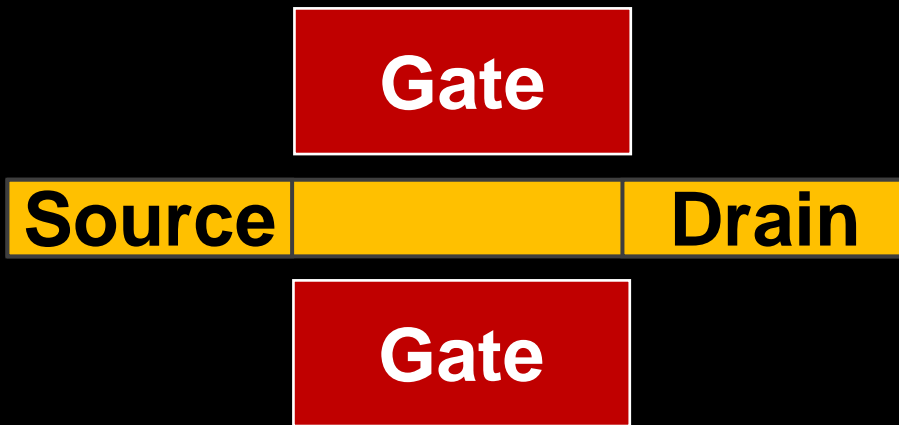


Gate cannot control the leakage current paths that are **far from the gate.**

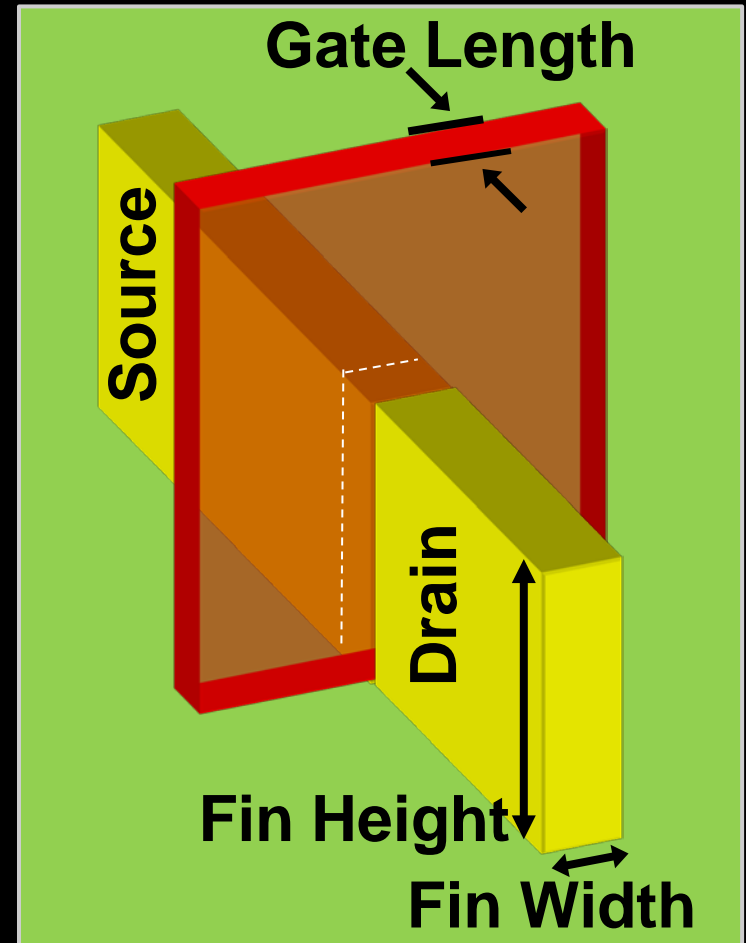
C.Hu, "Modern Semicon. Devices for ICs" 2010, Pearson

# A Structure without Si Far from Gate

**Thin** body controlled by multiple gates.



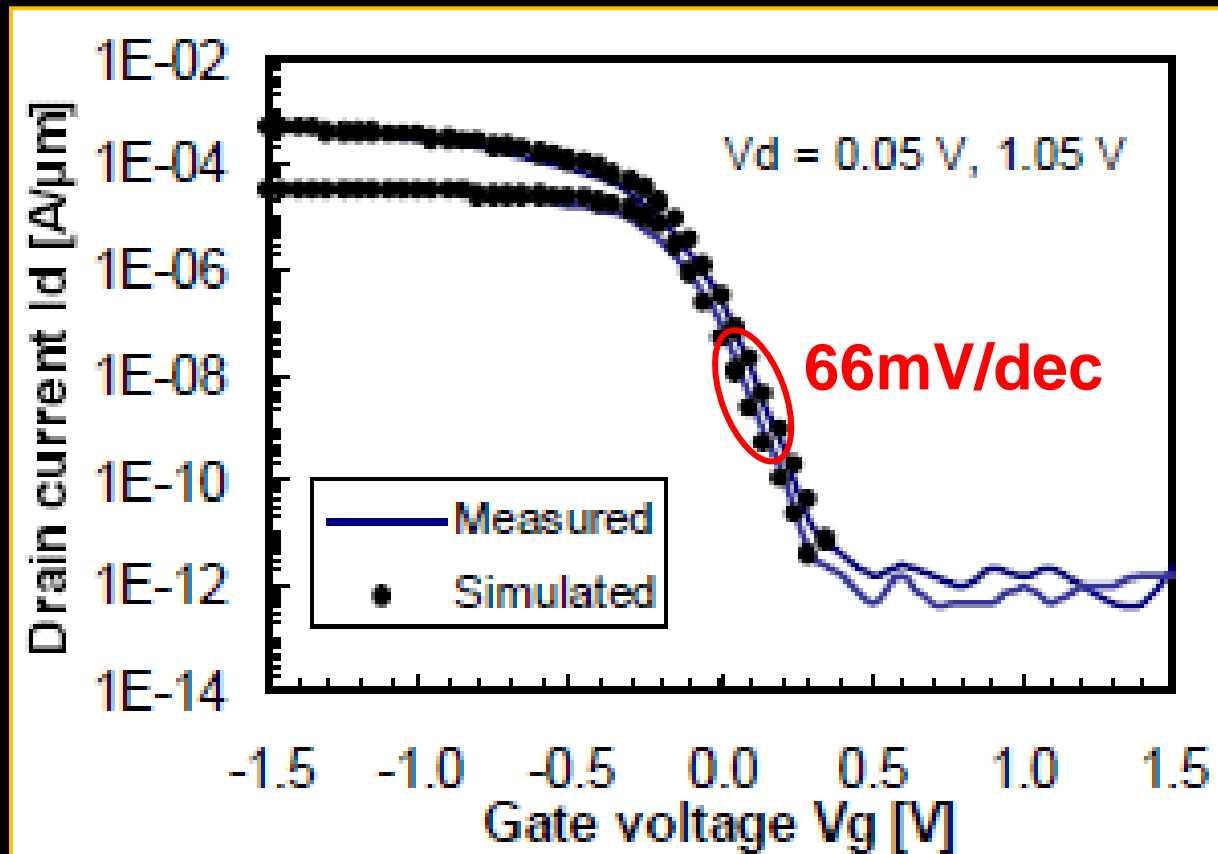
**FinFET** body is a thin Fin. →



N. Lindert et al., DRC paper II.A.6, 2001

# 40nm FinFET – 1999

30nm Fin allows 2.7nm SiO<sub>2</sub> & undoped body ridding random dopant fluctuation.

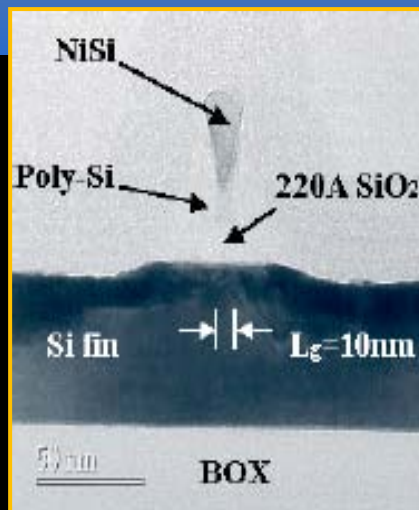


# Introduced a New Scaling Rule

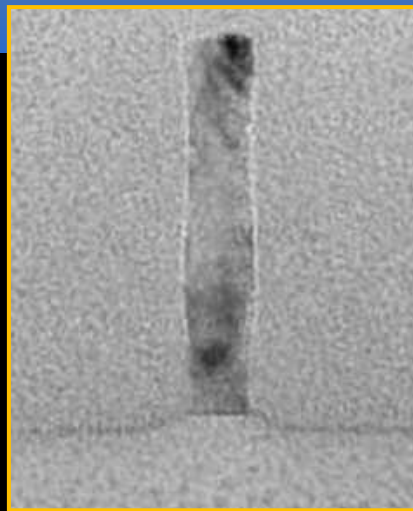
Leakage is well suppressed if

**Fin thickness  $< L_g$**

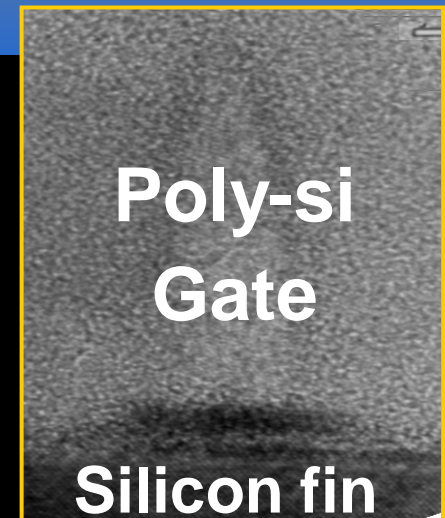
**10nm  $L_g$   
AMD  
2002 IEDM**



**5nm  $L_g$   
TSMC  
2004 VLSI**



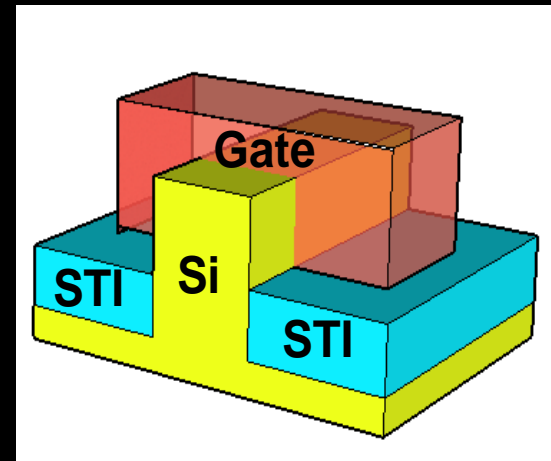
**3nm  $L_g$   
KAIST  
2006 VLSI**



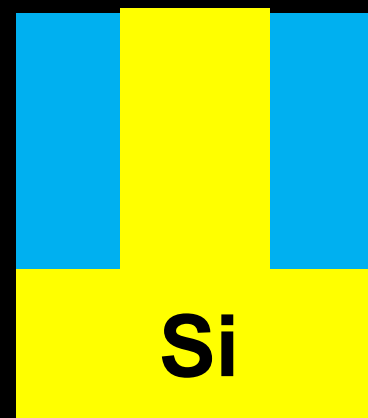


# Two Improvements Since 1999

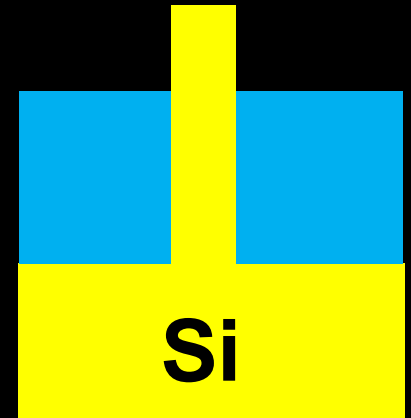
- **2002** FinFET with thin oxide on fin top.  
F.L.Yang et al. (TSMC)  
2002 IEDM, p. 225.
- **2003** FinFET on bulk substrate.  
T. Park et al. (Samsung)  
2003 VLSI Symp. p. 135.



Planar FET



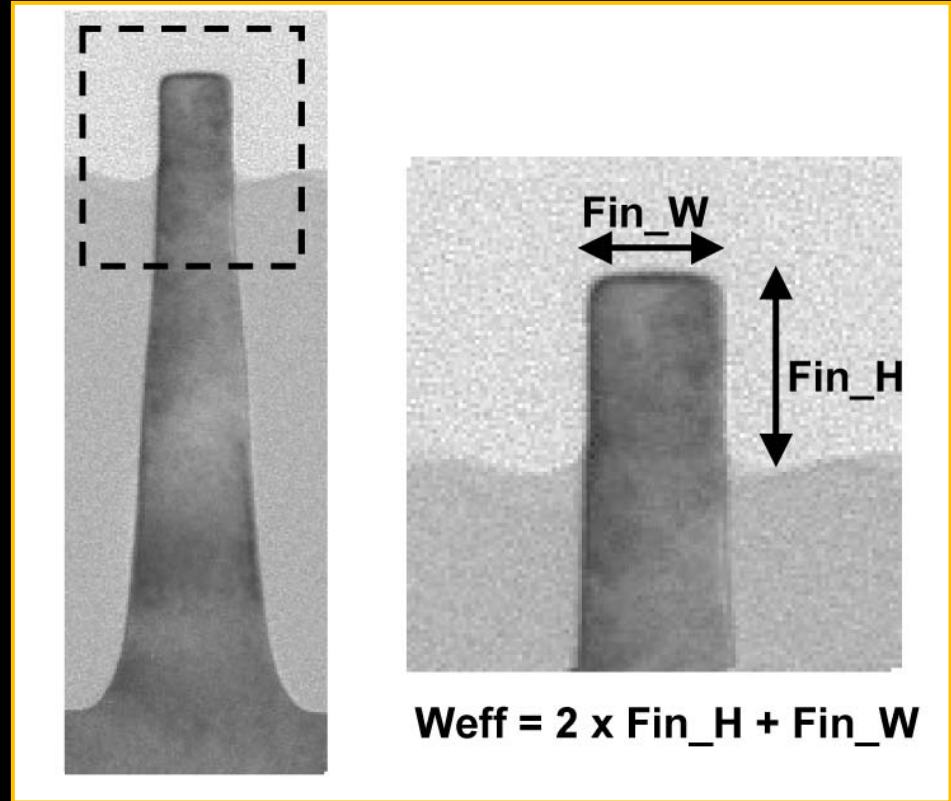
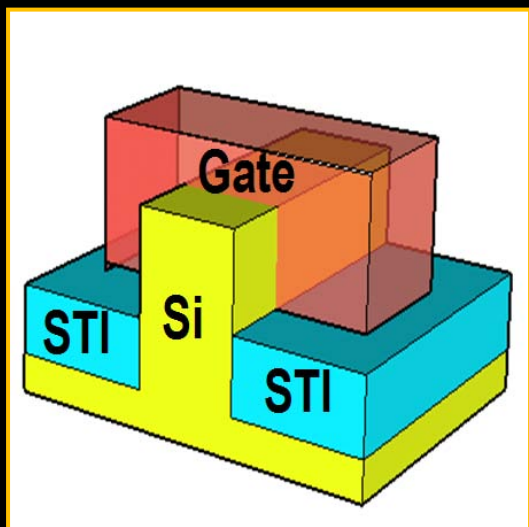
FinFET



# 20nm FinFET

Planar FET

FinFET



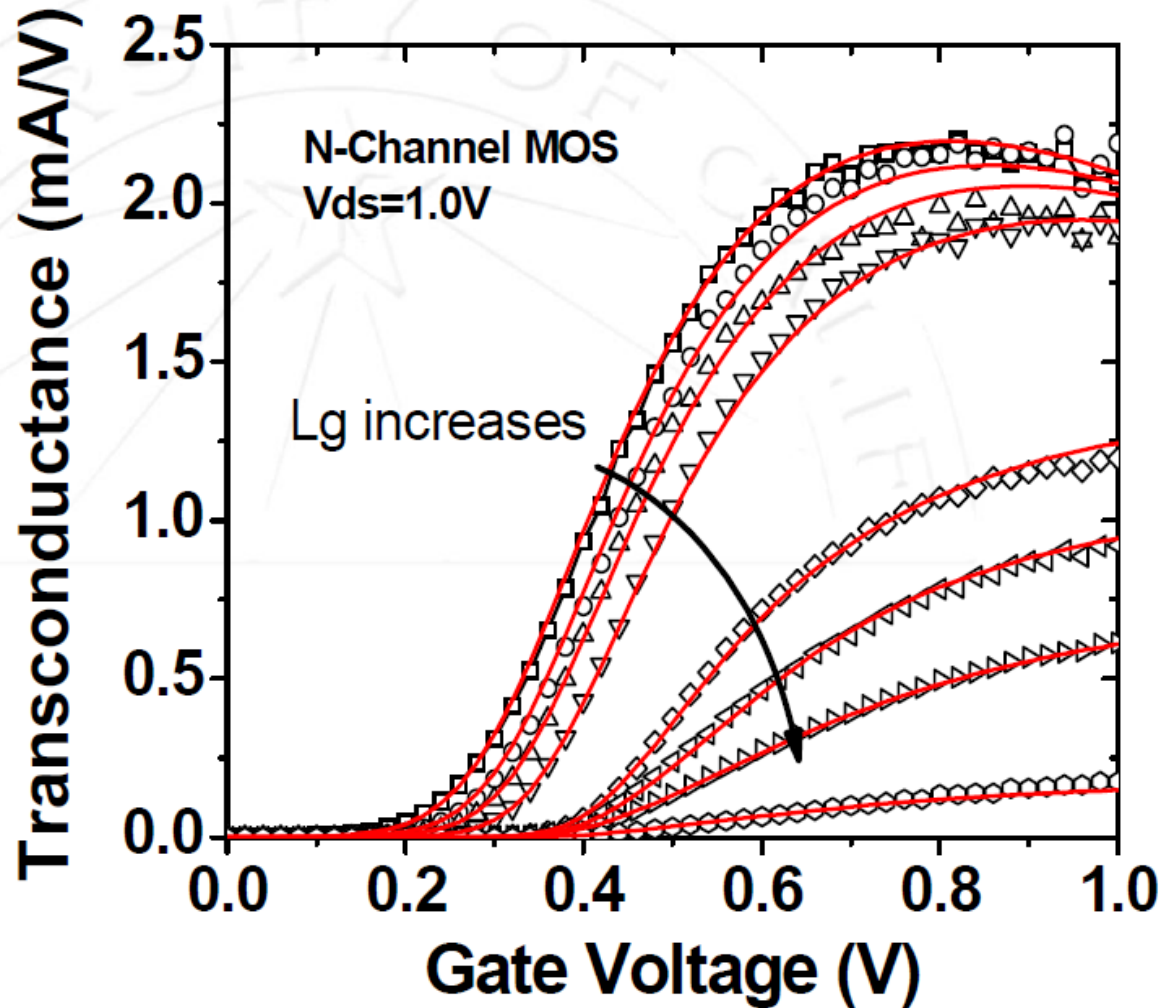
C.C. Wu et al., 2010 IEDM

# BSIM

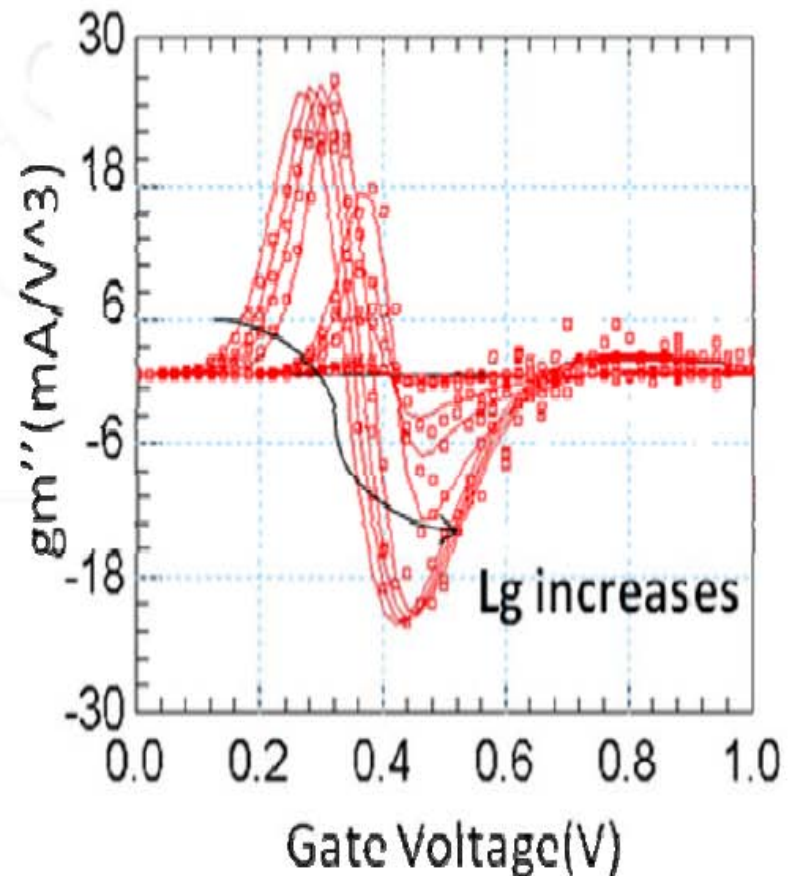
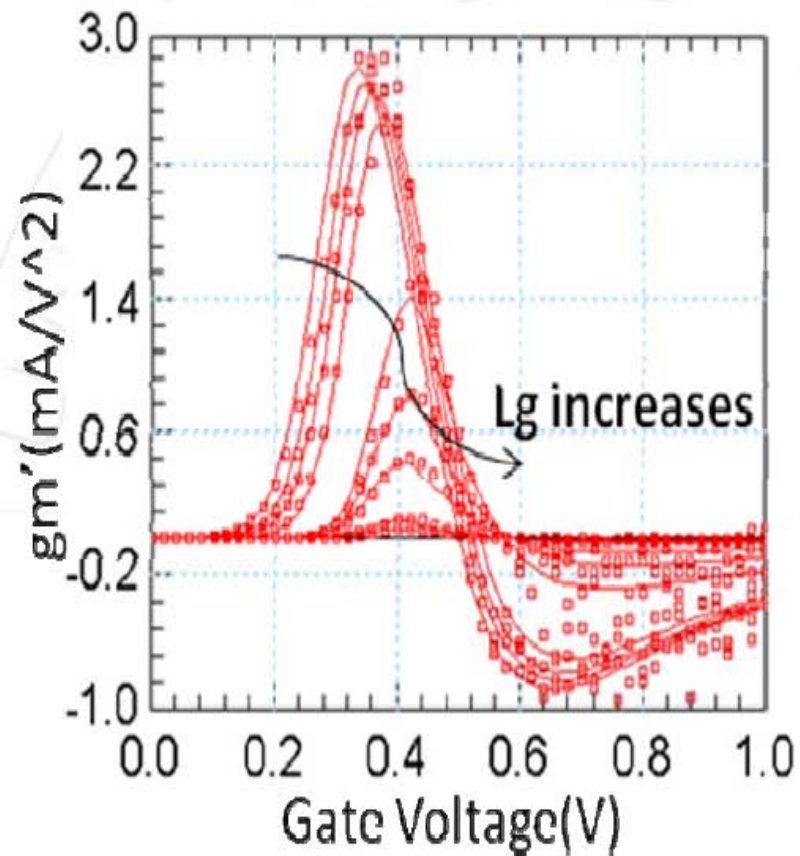
- **Berkeley Short-channel IGFET Model**
- **First industry standard SPICE model for IC simulation**
- **Used by hundreds of companies for IC design since 1997**
- **BSIM FinFET model became industry standard in March 2012**



# Global fitting with 30nm-10um FinFETs



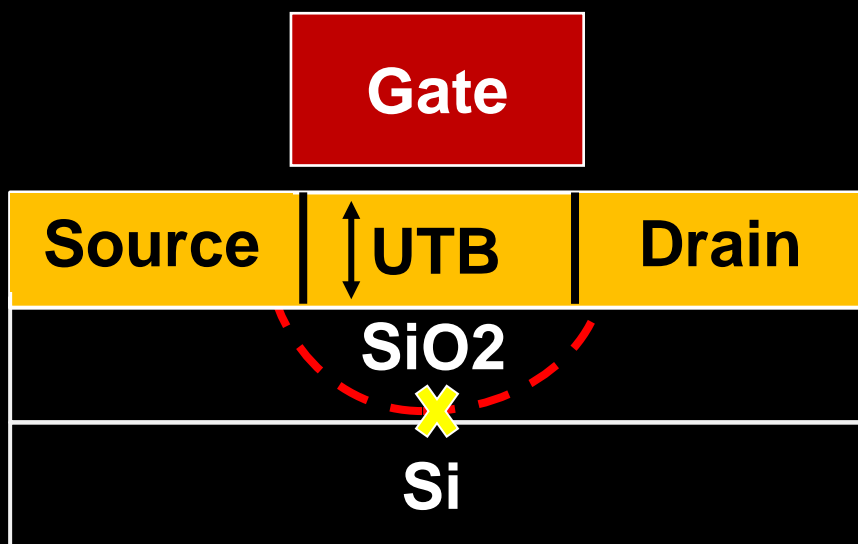
# Global fitting with 30nm-10um FinFETs



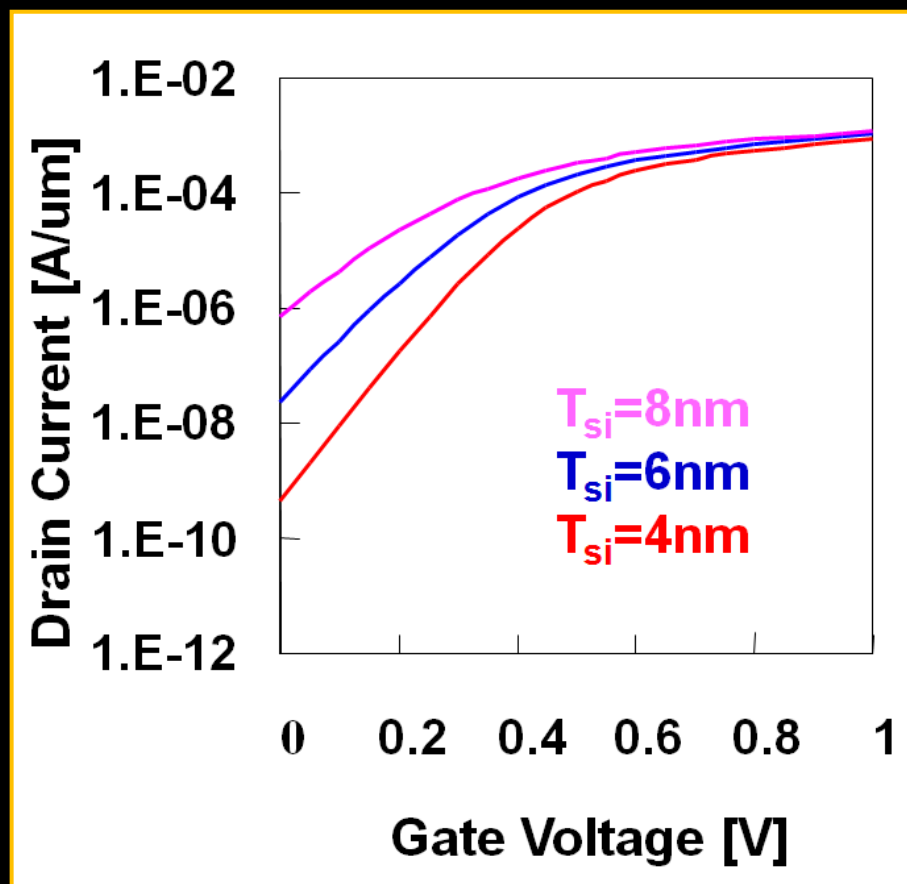
# Another Structure

with no Si far from the gate

## Ultra-Thin-Body FET (UTB-FET)

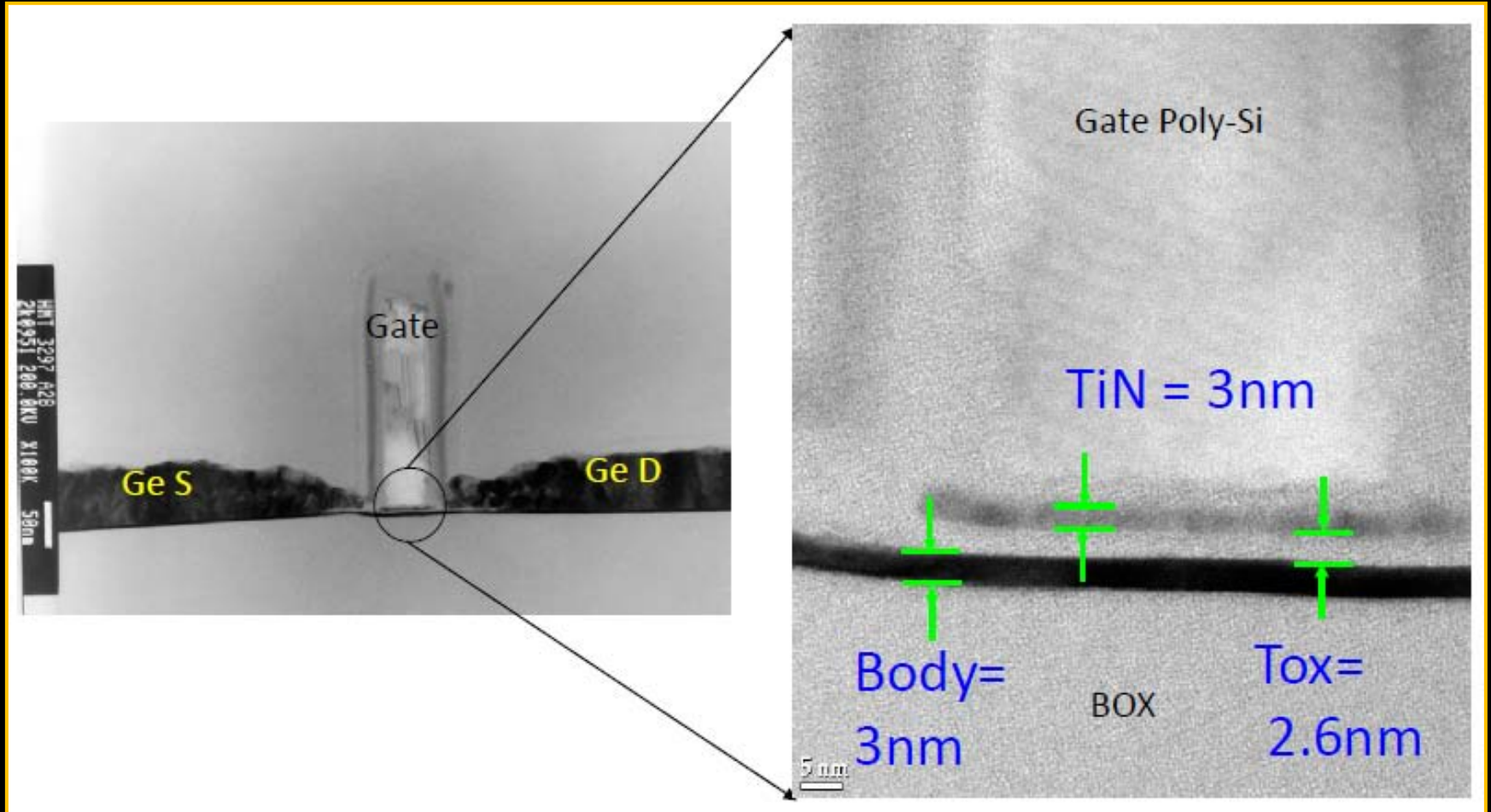


Y-K. Choi, IEEE EDL, p. 254, 2000



# 2001 UTB-FET

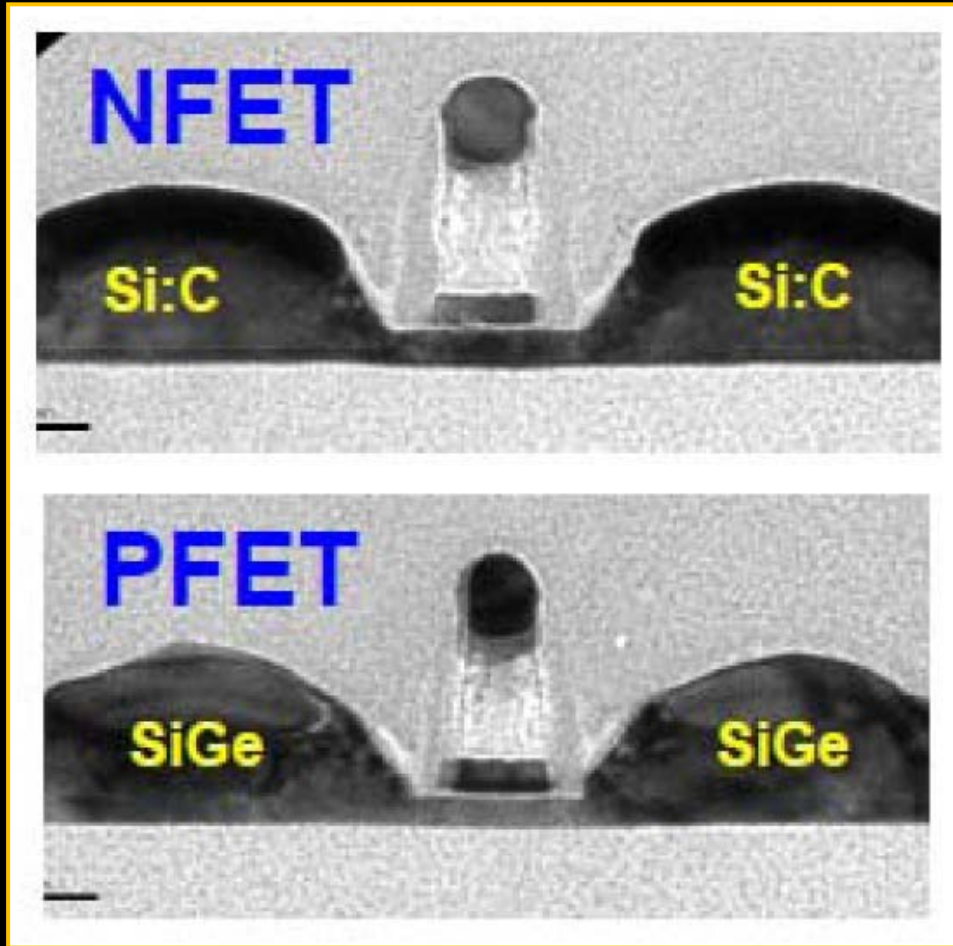
## 3nm Silicon Body, Raised S/D



Y-K. Choi et al, VLSI Tech. Symposium, p. 19, 2001



# 2009 20nm UTB-FET using 5nm-Body



K. Cheng et al, IEDM, 2009

Other Names:

- FDSOI
- UTBB



# Outlook

## FinFET

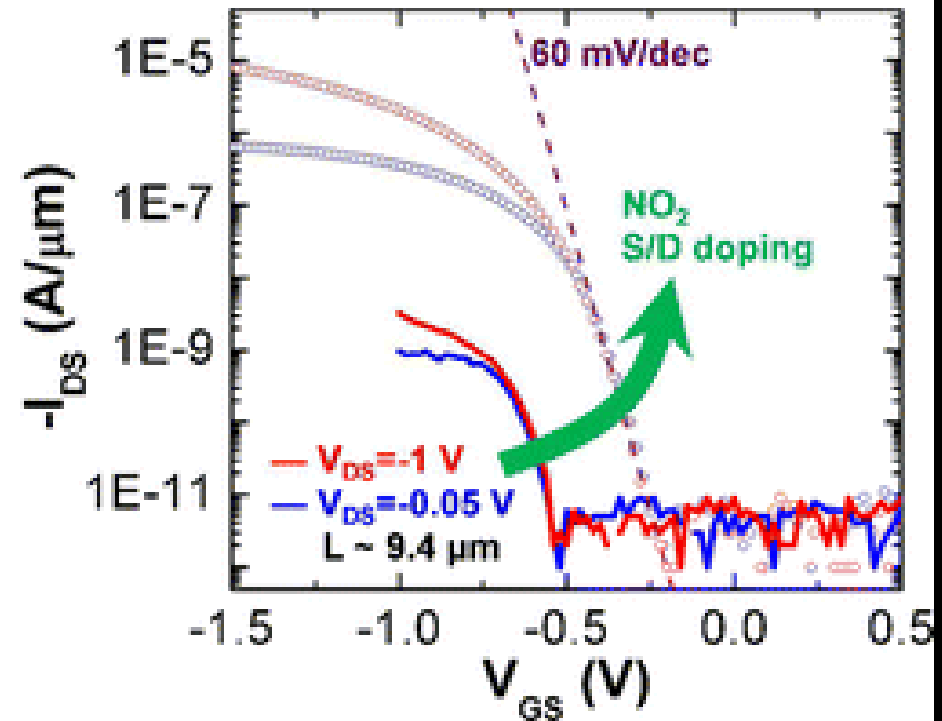
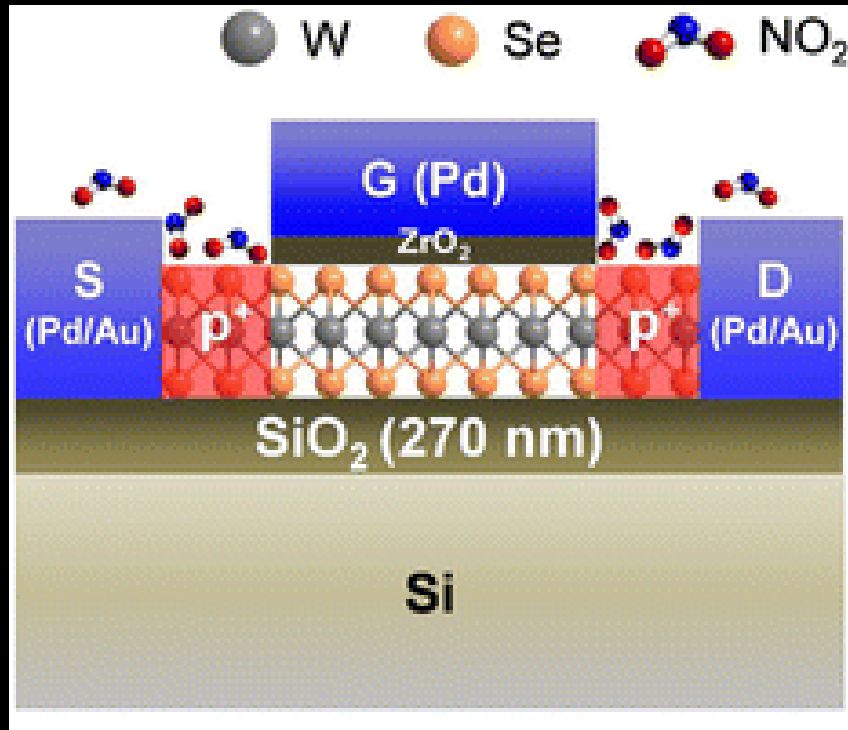
Intel uses it at 22nm and foundries at 14nm or sooner

## UTB-FET

ST uses **UTB-FET** at 28nm, 20nm... against regular CMOS

**Competition will bring out the best of both.**

# WSe<sub>2</sub> UTB-FET



60mV/decade experimentally demonstrated

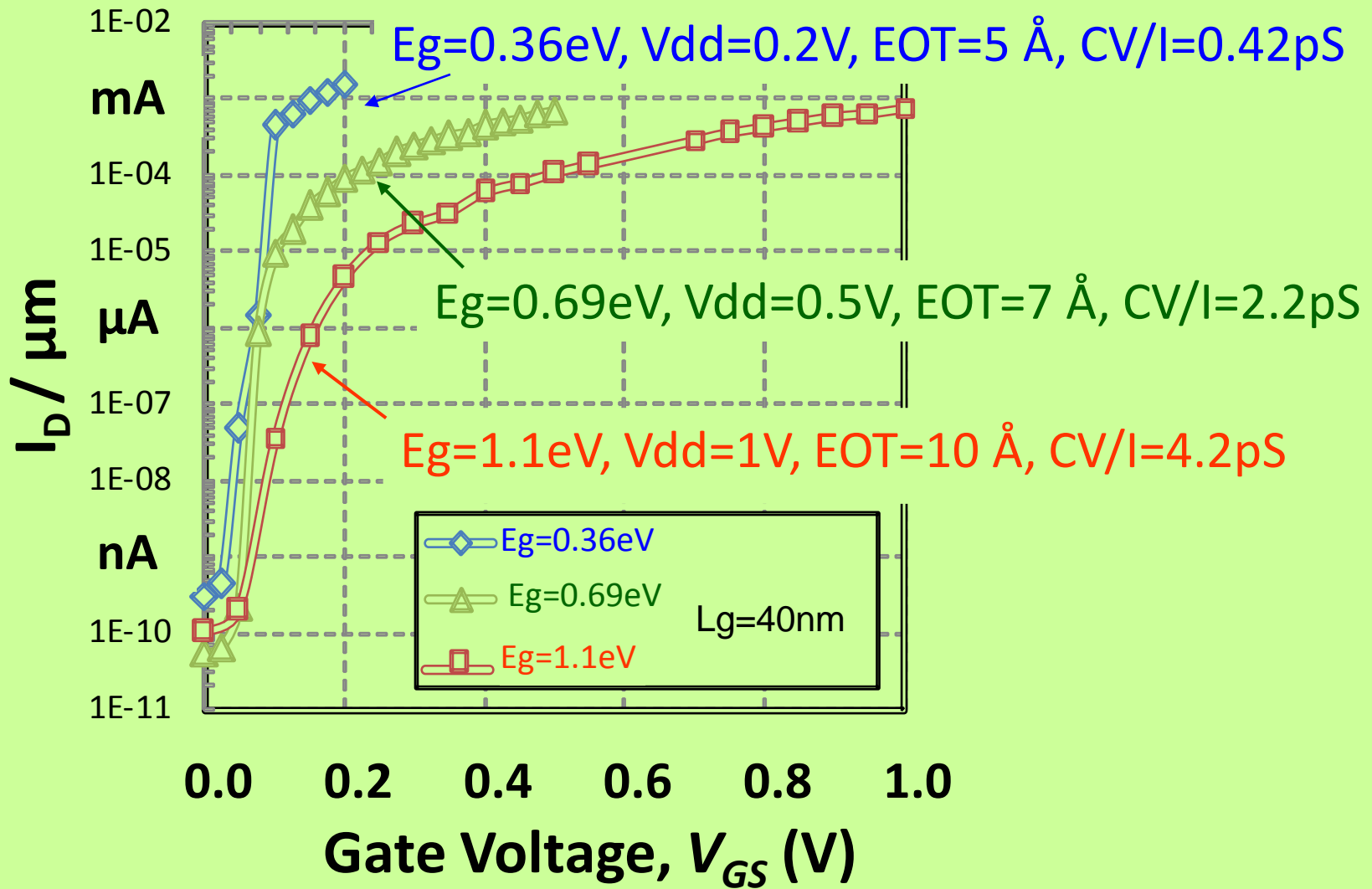
H. Fang et al., *Nano Lett.*, Vol 12, 3788 (2012)

$$P = f C V^2$$

- How to reduce  $V_{dd}$  to 0.1V?
- Need a **new transistor** turning on/off with 0.1V change in  $V_g$ .

**e.g. Tunneling Transistor**

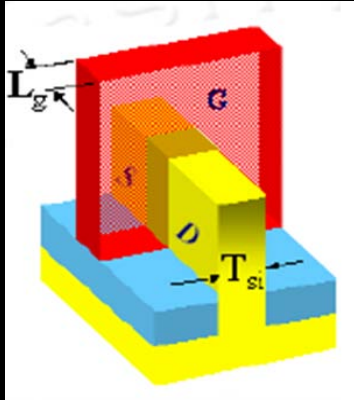
# Scale Vdd by Scaling Eg - Simulation



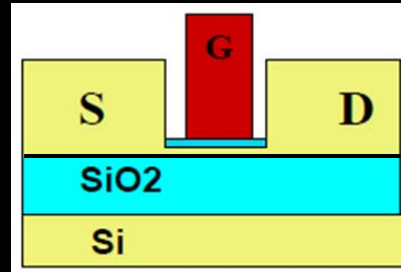
C. Hu, 2008 VLSI-TSA, p.14, April, 2008

**Must:** Thin body thickness/diameter  $< \alpha L_g$

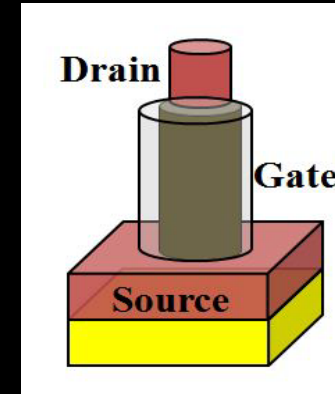
FinFET



UTB



Pillar/nano-Wire



**Want:** High mobility + low contact resistance

**Future Must:** 2D-crystal semiconductor for 3D IC,  
e.g., graphene, MoS<sub>2</sub>, WSe<sub>2</sub>...

(WSe<sub>2</sub> UTB with 60mV/dec: Fang, Javey,.., *Nanolett.*, 2012)

**Future Must:** 100mV V<sub>dd</sub>, e.g., TFET, Negative  
Capacitance FET (Salahudin,..,*Nanolett.*, 2008) ,...

# Gradually Add New Technologies

1. FinFET, UTB, Pillar structure
2. 1 + **SiGe/III-V**
3. 2 + 0.1V **TFET**
4. 3 + 2D-crystal materials for true **3D ICs**  
using deposited stacks of  
semiconductor, dielectric, metal, e.g.,  
MoS<sub>2</sub>/BN/graphene

# Summary

- **Ultra thin body** allows device scaling beyond 10nm.
- **2D-crystal** semiconductors are the ultimate **UTB-FET** materials, great for 3D IC.
- A new transistor will enable 0.1V IC in the 2020's.