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Preliminary Call for Papers

ISQED 2017
18th International Symposium & Exhibits on
QUALITY ELECTRONIC DESIGN

March 2017 - Santa Clara, CA

Paper Submission Deadline: Sept. 9 2016
Acceptance Notifications: Dec. 5, 2016
Final Camera-Ready paper: Jan. 10, 2017

A pioneer and leading interdisciplinary electronic design and semiconductor conference, ISQED accepts and promotes papers in following areas:

- Hardware and System Security
- Smart Sensors & IoT - Design and Technology
- System-level Design and Methodologies
- Package and Three-Dimensional Integration
- Integrated Circuit Design
- EDA Methodologies & IP Cores; Interoperability, Security, and Reuse
- Design Verification and Design for Testability
- Physical Design, Methodologies & Tools
- Emerging Process & Device Technologies and Design Issues
- Design Technology Co-Optimization; Designing at the Manufacturing Frontier
- Cognitive Computing in Hardware

Papers from past ISQED events have been published in ISQED proceedings and IEEE Xplore.
For more information please visit:

www.ISQED.org
On behalf of the ISQED 2015 conference and technical committees, we are pleased to welcome you to the 17th International Symposium on Quality Electronic Design, ISQED 2016. The 17th International Symposium on Quality Electronic Design (ISQED 2016) is the premier interdisciplinary and multidisciplinary Electronic Design conference—bridges the gap among Electronic/Semiconductor ecosystem members providing electronic design tools, integrated circuit technologies, semiconductor technology, packaging, assembly & test to achieve design quality. ISQED is held with the technical sponsorship of IEEE CASS, IEEE EDS, and IEEE Reliability Society.

ISQED continues to provide and foster a unique opportunity to participants to interact and engage themselves in cutting edge tutorials, presentations, and panel and plenary sessions. We are happy to report a number of initiatives this year. The conference is organized around the theme ‘IoT, Smart Sensors and Security’. And we have invited 2 distinguished keynote speakers from industry to focus on these topics.

Additionally four tutorials provide a holistic approach, from devices to circuits to systems, while covering in-depth studies and state-of-the-art in each of the topics impacting the quality of electronic design. The two-day technical program with three parallel sessions pack over 100 papers highlighting the latest trends in electronic circuit and system design & automation, test, verifications, and semiconductor technologies. ISQED 2016 also features a panel discussion titled “Industry Panel on Hardware and System Security” on Tuesday March 15th.

All the technical presentations, plenary sessions, panel discussions, tutorials and related events will take place on March 15-16 at the Santa Clara Convention Center in Santa Clara, CA. Please refer to the conference booklet and/or ISQED website for program details. Welcome to another stellar year of ISQED! It couldn't have happened without your support and participation.

Brian Cline  
TPC Co-Chair

Saibal Mukhopadhyay  
TPC Co-Chair

Peter J. Wright  
General Chair

Hai (Helen) Li  
Tutorial Chair

Vinod Viswanath  
Tutorial Co-Chair

Paul Wesling  
Publication Chair

Gang Qu  
Plenary Chair

Ali A. Iranmanesh  
Founder & President
1A.1

Sizing-Priority Based Low-Power Embedded Memory for Mobile Video Applications

Seyed Alireza Pourbakhsh, Xiaowei Chen, Dongliang Chen, Xin Wang, Na Gong, Jinhui Wang
North Dakota State University

2A.2

Process Variation Aware Crosstalk Mitigation for DWDM based Photonic NoC Architectures

Sai Vineel Reddy Chittamuru, Ishan Thakkar, Sudeep Pasricha
Colorado State University

2C.1

Exploring the Use of Volatile STT-RAM for Energy Efficient Video Processing

Hengyu Zhao¹, Hongbin Sun¹, Qiang Yang², Tai Min¹, Nanning Zheng¹
¹Xi’an Jiaotong University, ²Changhong Electric Co., Ltd

5A.1

Reliability and Energy-aware Cache Reconfiguration for Embedded Systems

Yuanwen Huang and Prabhat Mishra
University of Florida

5B.1

Digital IP Protection Using Threshold Voltage Control

Joseph Davis, Niranjan Kulkarni, Jinghua Yang, Aykut Dengi, Sarma Vrudhula
Arizona State University

5B.5

On Testing Physically Unclonable Functions for Uniqueness

Arunkumar Vijayakumar, Vinay Patil, Sandip Kundu
University of Massachusetts Amherst

6A.1

Impact of Interconnect Variability on Circuit Performance in Advanced Technology Nodes

Divya Madapusi Srinivas Prasad, Chenyun Pan, Azad Naeemi
Georgia Institute of Technology

6B.4

AFD-Based Method for Signal Line EM Reliability Evaluation

Zhong Guan, Malgorzata Marek-Sadowska
University of California, Santa Barbara
Best Papers

5A.1
Reliability and Energy-aware Cache Reconfiguration for Embedded Systems
Yuanwen Huang and Prabhat Mishra
University of Florida

5B.1
Digital IP Protection Using Threshold Voltage Control
Joseph Davis, Niranjan Kulkarni, Jinghua Yang, Aykut Dengi, Sarma Vrudhula
Arizona State University

* Authors of best papers are honored during the luncheon on Tuesday March 15
## ISQED 2016 Organizing Committee

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<th>Position</th>
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<tr>
<td>General Chair</td>
<td>Peter J. Wright</td>
<td>Synopsys</td>
</tr>
<tr>
<td>Plenary Chair</td>
<td>Ali Iranmanesh</td>
<td>Silicon Valley Polytechnic</td>
</tr>
<tr>
<td>Panel Chair</td>
<td>Gang Qu</td>
<td>University of Maryland</td>
</tr>
<tr>
<td>Japan Chair</td>
<td>Masahiro Fujita</td>
<td>University of Tokyo</td>
</tr>
<tr>
<td>Taiwan Chair</td>
<td>Shih-Hsu Huang</td>
<td>Chung Yuan Christian University</td>
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<tr>
<td>Brazil &amp; South America Chair</td>
<td>Fabiano Passuelo Hessel</td>
<td>Pontificia Universidade Catolica do Rio Grande do Sul, Brazil</td>
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<tr>
<td>TPC Co-Chair</td>
<td>Saibal Mukhopadhyay</td>
<td>Georgia Institute of Technology</td>
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<tr>
<td>TPC Co-Chair</td>
<td>Brian Cline</td>
<td>ARM</td>
</tr>
<tr>
<td>Tutorials Chair</td>
<td>Hai (Helen) Li</td>
<td>University of Pittsburgh</td>
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<tr>
<td>Tutorials Co-Chair</td>
<td>Vinod Viswanath</td>
<td>Real Intent</td>
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<tr>
<td>Publication Chair</td>
<td>Paul Wesling</td>
<td>IEEE</td>
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<tr>
<td>Europe Chair</td>
<td>George P. Alexiou</td>
<td>University of Patras and RA-CTI, Patras, Greece</td>
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<tr>
<td>China Chair</td>
<td>Gaofeng Wang</td>
<td>Hangzhou Dianzi University</td>
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</table>
TECHNICAL PROGRAM COMMITTEES

**Cognitive Computing in Hardware (CCH)**

Yiran Chen, University of Pittsburgh (Chair)
Vikas Chandra, ARM (Co-Chair)

**Committee Members:**
- Yu Cao - Arizona State University
- Abishai Daniel - Intel
- Miao Hu - HP labs
- Hao Jiang - San Francisco State University
- Yang Yi - University of Kansas

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Bao Liu, University of Texas at San Antonio (Co-Chair)

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- Domenic Forte - University of Florida
- Ken Mai - Carnegie Mellon University
- Seetharam Narasimhan - Intel Corp
- Nicolas Sklavos - Computer Engineering & Informatics Department, University of Patras
- Xuehui Zhang - Oracle

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Rajan Beera, Pall Corporation (Co-Chair)

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- Vivek Joshi - GLOBALFOUNDRIES
- Murari Mani - AMD
- Jimson Mathew - University of Bristol
- Mustafa Berke Yelten - Istanbul Technical University
- Vladimir Zolotov - IBM
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Ping Gao - Aries Design Automation
Abhilash Goyal - IEEE Member
Michael Hsiao - Virginia Tech
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Vamsi Srikantam (Co-Chair)

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Rung-Bin Lin - Yuan Ze University
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Rajeev Murgai - Synopsys India Pvt. Ltd.
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Jia Wang - Illinois Institute of Technology
Hua Xiang - IBM Research
Guo Yu - Oracle
Min Zhao - oracle
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Qiang Cui - Qorvo Inc.
Jayita Das - Sr. Technology and Design Integration Engineer
Nikos Konofaos - AUTH
Chun-Yu Lin - National Taiwan Normal University
Guofu Niu - guofu.niu
Renato ribas - UFRGS
Swatilekha Saha - Cypress Semiconductor Corporation
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Rasit Onur Topaloglu - IBM
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Steve Heinrich-Barna, Texas Instruments, Inc (Co-Chair)

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Plamen Asenov - Gold Standard Simulations
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Paulo Butzen - Universidade Federal do Rio Grande - FURG
subho chatterjee - intel corporation
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Kurt Schwartz - Texas Instruments
Jeremy Tolbert - Samsung Austin R&D Center
Haibo Wang - Texas A&M International University
Cheng Zhuo - Intel Corp.Cheng Zhuo - Intel

Smart Sensors for IoT – Design & Technology (SSDT)

Xiaoning Qi (Chair)
Vijay Raghunathan, Purdue University (Co-Chair)

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Kamesh Gadepally - GigaCom Semiconductor
Michel Maharbiz - U.C. Berkeley
Libor Rufer - University of Grenoble
Thilo Sauter - Danube University Krems
System-level Design and Methodologies (SDM)

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Shiyan Hu, Michigan Technological University (Co-Chair)

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Rosilde Corvino - Intel
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Hana Kubatova - CTU in Prague
Hai (Helen) Li - University of Pittsburgh
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Vivek Nandakumar - Synopsys
Gabriela Nicolescu - Ecole Polytechnique de Montréal
Antonio Nunez - University of Las Palmas GC
Sudeep Pasricha - Colorado State University
Shana-Jang Ruan - National Taiwan University of Sci. and Tech.
Tuna Tarim - Texas Instrument, Inc.
Tianyi Wang - Florida International University
Yu Wang - Auburn University, ECE department
Bei Yu - The Chinese University of Hong Kong

3 Dimensional Integration & Adv. Packaging (TDIP)

Sung Kyu Lim, Georgia Tech (Chair)
Kambiz Samadi, Qualcomm Technologies, Inc. (Co-Chair)

Committee Members:
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Nauman Khan - Intel Corporation
Dae Hyun Kim - Washington State University
Manuel Luschas - Broadcom
Shreepad Panth - Altera Corporation
Yiyu Shi - University of Notre Dame
Saurabh Sinha - ARM Inc.
Jianyong Xie - Intel
HL Yiu - Hong Kong Science and Technology Parks
Hirokazu Yonezawa - Panasonic Corporation
Payman Zarkesh-Ha - University of New Mexico
Ehrenfried Zschech - Fraunhofer IKTS
**Embedded Tutorials**

**Chair:** Hai (Helen) Li - University of Pittsburgh

**Co-Chair:** Vinod Viswanath - Real Intent

**On-Chip Nonvolatile Memory Designs for Energy-Efficient IoT**

Prof. Meng-Fan (Marvin) Chang  
National Tsing Hua University (NTHU), Taiwan

**Pattern Recognition and Learning with Neuromorphic Cognitive Systems**

Prof. Giacomo Indiveri  
University of Zurich, Switzerland

**Low Power SoC System Design**  
A Systems Approach to Power Management Techniques, Power and Performance Optimizations, Thermal and Energy Management of Systems-on-Chip

Rajiv Muralidhar  
Senior Platform Architect, Intel Corporation

---

**KEYNOTE SPEECHES**

**New Frontiers in Hardware Security & Trust**

Prof. Mark M. Tehranipoor  
Charles E. Young Professor in Cybersecurity  
ECE Department  
University of Florida

**Avoiding The Dark Side Of The Cloud Using Secure And Reliable IoT Devices**

Navraj Nandra  
Sr. Director of Marketing  
DesignWare Interface and Analog IP  
Synopsys

**Luncheon Panel Discussion**  
Hardware and System Security in IoT Era

**Chair & Moderator**  
Prof. Gang Qu - University of Maryland

**Panelists:**  
Dr. Seetharam Narasimhan - Intel  
Prof. Mark M. Tehranipoor - Florida Institute for Cybersecurity  
Tom Katsioulas - Mentor Graphics  
Michele D. Guel - Cisco Systems  
Mohit Arora - NXP Semiconductors  
Dr. Pim Tuyls - Intrinsic-ID
GENERAL INFORMATION

ISQED LUNCH & AWARDS CEREMONY

Tuesday, March 15, 12:00PM-12:35PM
Great America Ballroom

ISQED Best Paper Awards
Recipients of the ISQED 2016 Best Paper Award will be recognized during the ISQED luncheon on Tuesday. List of best papers is shown in Page 2 of this document.

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TECHNICAL SESSIONS
There are a total of 16 paper sessions held on Tuesday and Wednesday. Technical sessions are held in the format of three parallel tracks in Great America Meeting Rooms 1-3.

Poster Papers & Mixer
Poster display will take place on Tuesday afternoon 5:30PM-7:00PM in the Atrium area outside of Great America Meeting Rooms 1-3. Authors will be available to discuss their works and to answer questions. Refreshments will be served.

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ON-SITE REGISTRATION
Tentative time schedule of on-site registration is as follows:

Tuesday, March 15  8:00AM-5:00PM
Wednesday, March 16  8:00AM-1:00PM

Registration desk location will be alternate between the location beside Great America meeting rooms 1-3, and the location right outside Great America Ballrooms.

Co-located Events

IoT Summit
March 17-18
Great America Ballrooms
www.IoT-Summit.org
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<td>TUESDAY 3/15/2016</td>
<td>9:00AM-10:00AM</td>
<td>PLENARY SESSION 1P</td>
<td>KEYNOTE SPEECHES BY: PROF. MARK M. TEHRANIPOOR - UNIVERSITY OF FLORIDA, NAVRAJ NANDRA - SYNOPSYS</td>
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<td>10:00AM-10:30AM</td>
<td>MORNING BREAK</td>
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<td></td>
<td>10:30AM-11:50AM</td>
<td>SESSION 1A - LOW POWER MEMORY &amp; LOGIC DESIGN</td>
<td>GREAT AMERICA MEETING ROOM 1</td>
<td>GREAT AMERICA MEETING ROOM 2</td>
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<td>12:00PM-1:45PM</td>
<td>ISQED PANEL &amp; LUNCHEON</td>
<td>GREAT AMERICA MEETING ROOM 3</td>
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<td></td>
<td>MORNING BREAK</td>
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<td>2:00PM-3:20PM</td>
<td>SESSION 2A - NETWORK ON A CHIP</td>
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<td>3:20PM-3:40PM</td>
<td>AFTERNOON BREAK</td>
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<td>WEDNESDAY 3/16/2016</td>
<td>8:30AM-9:50AM</td>
<td>SESSION 4A - POWERING IOT</td>
<td>GREAT AMERICA MEETING ROOM 1</td>
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<td></td>
<td>9:50AM-10:00AM</td>
<td>MORNING BREAK</td>
<td></td>
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<td></td>
<td>10:00AM-11:00AM</td>
<td>EMBEDDED TUTORIAL 3 - LOW POWER SOC SYSTEM DESIGN - A SYSTEMS APPROACH TO POWER MANAGEMENT TECHNIQUES, POWER AND PERFORMANCE OPTIMIZATIONS, THERMAL AND ENERGY MANAGEMENT OF SYSTEMS-ON-CHIP</td>
<td>GREAT AMERICA MEETING ROOM 3</td>
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<td></td>
<td>11:00AM-12:00PM</td>
<td>EMBEDDED TUTORIAL 4 - BUILDING NEUROMORPHIC COMPUTING SYSTEMS WITH EMERGING DEVICE TECHNOLOGIES</td>
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<td>12:00PM-1:00PM</td>
<td>LUNCH BREAK</td>
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<td>1:00PM-2:20PM</td>
<td>EMBEDDED SYSTEMS</td>
<td>GREAT AMERICA MEETING ROOM 1</td>
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<tr>
<td></td>
<td>2:20PM-2:40PM</td>
<td>AFTERNOON BREAK</td>
<td></td>
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<tr>
<td></td>
<td>2:40PM-4:20PM</td>
<td>DESIGN OPTIMIZATION FOR PERFORMANCE, RELIABILITY, AND YIELD</td>
<td>GREAT AMERICA MEETING ROOM 1</td>
<td>GREAT AMERICA MEETING ROOM 2</td>
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</tbody>
</table>
New Frontiers in Hardware Security and Trust

Hardware security domain has received significant attention from researchers in academia, industry, and government due mainly to the globalized design, fabrication, and assembly of integrated circuits and systems. The complexity of today’s electronic components and systems supply chain has made it increasingly vulnerable to malicious activities, security attacks, and counterfeiting activities. In this talk, we will first analyze these vulnerabilities and threats. We will then present challenges dealing with emerging attacks and threats and present potential solutions to addressing them. Finally, we will present opportunities that securing hardware can provide at different application domains, different levels of abstraction, and from nano-device to systems.

About Mark M. Tehranipoor

Mark Tehranipoor is currently the Intel Charles E. Young Professor in Cybersecurity at the ECE Department, University of Florida. His current research interests include: hardware security and trust, counterfeit electronics detection and prevention, supply chain risk management, and reliable and testable circuit design. Dr. Tehranipoor has published over 250 journal articles and refereed conference papers and has given more than 150 invited talks and keynote addresses since 2006. He has published six books and ten book chapters. He is a recipient of several best paper awards as well as the 2008 IEEE Computer Society (CS) Meritorious Service Award, the 2012 IEEE CS Outstanding Contribution, the 2009 NSF CAREER Award, and the 2014 MURI award. His projects are sponsored by both the industry (Semiconductor Research Corporation (SRC), Texas Instruments, Freescale, Comcast, Honeywell, LSI, Avago, Mentor Graphics, R3Logic, Cisco, Qualcomm, MediaTeck, etc.) and Government (NSF, ARO, MDA, DOD, AFOSR, DOE, etc.). He serves on the program committee of more than a dozen leading conferences and workshops. He served as Program and General Chairs of several leading conferences and workshops. Prior to joining UF, Dr. Tehranipoor was the founding director of CHASE and CSI centers at the University of Connecticut. He co-founded a new symposium called IEEE International Symposium on Hardware-Oriented Security and Trust (HOST) and served as HOST-2008 and HOST-2009 General Chair. He is currently serving as HOST’s Chair of Steering Committee. He is also the co-founder of Trust-Hub (www.trust-hub.org). He served as an Associate EIC for IEEE Design & Test, an IEEE Distinguished Speaker, and an ACM Distinguished Speaker from 2010 to 2014. He is currently serving as an Associate Editor for JETTA, JOLPE, Transactions on VLSI (TVLSI), and Transactions on Design Automation for Electronic Systems (TODAES). Dr. Tehranipoor is a Senior Member and Golden Core Member of the IEEE and Member of ACM and ACM SIGDA.
Avoiding The Dark Side Of The Cloud Using Secure And Reliable IoT Devices

Keeping the enormous amounts of data being generated by billions of smart connected devices ultimately stored in the cloud – secure - is a hotly debated topic. The number of connected devices is expected to reach 50 billion by the end of this decade. Today, it is estimated that 70% of IoT devices contain serious security vulnerabilities, 100 car models are affected with security flaws. This presentation will provide proposals for integrated silicon solutions that help prevent a wide range of evolving security threats in connected devices such as theft, tampering, side channels attacks, malware and data breaches.

About Navraj Nandra

Navraj Nandra is the Sr. Director of Marketing for the DesignWare Interface and Analog IP at Synopsys. He has worked in the semiconductor industry since the mid 80’s as an analog/mixed signal IC designer for Philips Semiconductors, Austria Micro Systems, (San Jose & Austria) and EM-Marin (Switzerland). He has been responsible for the complete design of a number of analog front ends in application areas such as digital audio, RFID and automotive. He joined Synopsys from Barcelona Design where he was Director of Application Engineering. During his four years at Barcelona he was responsible for pre- and post-sales support for Barcelona’s analog synthesis technology. Navraj holds a masters degree in Microelectronics, majoring in analog IC design, from Brunel University and a post-graduate diploma in Process Technology from Middlesex University. He has presented at numerous technical conferences on mixed-signal design, analog IP and analog synthesis/EDA.
SESSION 1A

Tuesday March 15

Low Power Memory & Logic Design

Chair: Kurt Schwartz, Texas Instruments
Co-Chair: Charles Augustine, Intel

10:30AM

1A.1
Sizing-Priority Based Low-Power Embedded Memory for Mobile Video Applications
Seyed Alireza Pourbakhsh, Xiaowei Chen, Dongliang Chen, Xin Wang, Na Gong, Jinhui Wang
North Dakota State University

10:50AM

1A.2
Bit-Upset Vulnerability Factor for eDRAM Last Level Cache Immunity Analysis
Navid Khoshavi, Xunchao Chen, Jun Wang, Ronald F. DeMara
University of Central Florida

11:10AM

1A.3
Optimizing SRAM Bitcell Reliability and Energy for IoT Applications
Harsh Patel, Farah Yahya, Benton Calhoun
University of Virginia

11:30AM

1A.4
Variability- and Correlation-Aware Logical Effort for Near-Threshold Circuit Design
Jun Shiomi, Tohru Ishihara, Hidetoshi Onodera
Kyoto University

SESSION 1B

Tuesday March 15

Advanced Three-Dimensional Integrated Circuits

Chair: Payman Zarkesh-Ha, University of New Mexico

10:30AM

1B.1
Design Challenges and Methodologies in 3D Integration for Neuromorphic Computing Systems
M. Amimul Ehsan\(^1\), Hongyu An\(^1\), Zhen Zhou\(^2\), Yang Yi\(^1\)
\(^1\)University of Kansas, \(^2\)Intel
10:50AM
1B.2
Optimization of Dynamic Power Consumption in Multi-Tier Gate-Level Monolithic 3D ICs
Sheng-En(David) Lin, Partha Pande, Dae Hyun Kim
Washington State University

11:10AM
1B.3
Electromigration-Aware Placement for 3D-ICs
Tiantao Lu¹, Zhiyuan Yang², Ankur Srivastava¹
¹ECE Department, University of Maryland, ²University of Maryland, College Park

11:30AM
1B.4
Monolithic 3D IC Design: Power, Performance, and Area Impact at 7nm
Kartik Acharya¹, Kyungwook Chang¹, Bon Woong Ku¹, Shreepad Panth¹, Saurabh Sinha², Brian Cline², Greg Yeric², Sung Kyu Lim¹
¹Georgia Institute of Technology, ²ARM Inc, ³Georgia Tech

SESSION 1C

Tuesday March 15
Technology beyond CMOS

Chair: Brian Cline, ARM
Co-Chair: Rajan Beera, Pall Corporation

10:30AM
1C.1
Nanodevices to Nanosystems: Carbon Nanotube Digital VLSI
Gage Hills¹, Max Shulaker², Chi-Shuen Lee², H.-S. Philip Wong², Subhasish Mitra²
¹Department of Electrical Engineering, Stanford University, ²Stanford University

10:50AM
1C.2
Negative Capacitance for Low Power Computing
Asif Khan and S Salahuddin
University of California, Berkeley

11:10AM
1C.3
Tunnel-FET: The Prospects and Challenges Ahead
Uygar Avci, Daniel Morris, Ian Young
Intel
Beyond Moore’s Law: It's More than Just Transistors
Saurabh Sinha, Greg Yeric, Lucian Shifren, Brian Cline
ARM Inc.

SESSION 2A
Tuesday March 15
Network on a Chip

Chair: Hai (Helen) Li, University of Pittsburgh
Co-Chair: Rajesh Berigei, Texas Instruments

2:00PM
2A.1
Maximizing the Performance of NoC-based MPSoCs under Total Power and Power Density Constraints
Alireza Shafran Bejestan¹, Yanzhi Wang¹, Lizhong Chen², Shuang Chen¹, Massoud Pedram³
¹University of Southern California, ²Oregon State University, ³USC

2:20PM
2A.2
Process Variation Aware Crosstalk Mitigation for DWDM based Photonic NoC Architectures
SAI VINEEL REDDY CHITTAMURU, Ishan Thakkar, Sudeep Pasricha
Colorado State University

2:40PM
2A.3
Memory-Aware Circuit Overlay NoCs for Latency Optimized GPGPU Architectures
Venkata Yaswath Raparti¹ and Sudeep Pasricha²
¹Colorado State University, Fort Collins, ²Colorado State University

3:00PM
2A.4
Design Guidelines for Embedded NoCs on FPGAs
Noha Gamal¹, Hossam Fahmy², Yehea Ismail³, Hassan Mostafa²
¹Mentor Graphics, ²Cairo University, ³CND at Zewail city and AUC

3:20PM
2A.5
A Delay Variation and Floorplan Aware High-level Synthesis Algorithm with Body Biasing
Koki Igawa, Youhua Shi, Masao Yanagisawa, Nozomu Togawa
Waseda University
SESSION 2B

Tuesday March 15

IoT Design Concepts

Chair: Stephan Heinrich-Barnes, Texas Instruments
Co-Chair: Charles Augustine, Intel

2:00PM
2B.1
IoT Memory Trends
Rashmi Sachan
Texas Instruments

2:20PM
2B.2
NVM Memory Requirements for a Secure IoT Ecosystem
Jim Lipman
Sidense Corp

2:40PM
2B.3
Challenges and Trends in Switched Capacitor Power Converters in an IoT World
Mervin John and Yogesh Ramadass
Texas Instruments

3:00PM
2B.4
Embedded Integrated Microdevices for the Internet of Things
Mark Bachman
University of California, Irvine

3:20PM
2B.5
Designing for Security in SoC-driven Supply Chains
Tom Katsioulas
Mentor Graphics
SESSION 2C

Tuesday March 15

Circuits and Architecture for Emerging Logic and Memory Technologies

Chair: Paul Tong, Pericom Semiconductor
Co-Chair: Swaroop Ghosh, University of South Florida

2:00PM
2C.1
Exploring the Use of Volatile STT-RAM for Energy Efficient Video Processing
Hengyu Zhao¹, Hongbin Sun¹, Qiang Yang², Tai Min¹, Nanning Zheng¹
¹Xi'an Jiaotong University, ²Changhong Electric Co., Ltd

2:20PM
2C.2
Low Power Data-Aware STT-RAM based Hybrid Cache Architecture
Mohsen Imani¹, Shruti Patil¹, Tajana Rosing²
¹University of California San Diego, ²UCSD

2:40PM
2C.3
Yield estimation and statistical design of memristor cross-point memory systems
Jizhe Zhang¹ and Sandeep Gupta²
¹Electrical Engineering Department, University of Southern California, ²University of Southern California (USC)

3:00PM
2C.4
ReMAM: Low Energy Resistive Multi-Stage Associative Memory for Energy Efficient Computing
Mohsen Imani¹, Pietro Mercati², Tajana Rosing²
¹University of California San Diego, ²UCSD

3:20PM
2C.5
Ultra-Low-Power Compact TFET Flip-Flop Design for High-Performance Low-Voltage Applications
Navneet Gupta¹, Adam Makosiej², Andrei Vladimirescu¹, Amara Amara¹, Costin Anghel³
¹Institut supérieur d'électronique de Paris, France; LETI, Commissariat à l’Energie Atomique et aux Energies Alternatives (CEA-LETI) France;, ²CEA-LETI, France, ³Institut supérieur d'électronique de Paris, France
SESSION T12

Tuesday March 15

Tutorial 1 & 2

Chair: Hai (Helen) Li, University of Pittsburgh
Co-Chair: Vinod Viswanth, Real Intent

3:40PM
T1
On-chip Nonvolatile Memory Designs for energy-efficient IoT
Meng-Fan (Marvin) Chang
National Tsing Hua University

4:40PM
T2
Pattern recognition and learning with neuromorphic cognitive systems
Giacomo Indiveri
University of Zurich

SESSION 3A

Tuesday March 15

On-Chip Machine Learning and Neuromorphic Computing

Chair: Rouwaida Kanj, American University of Beirut

3:40PM
3A.1
A Hardware Accelerator for Convolutional Neural Networks
Vinayak Gokhale and Eugenio Culurciello
Purdue University

4:00PM
3A.2
Sparsely Connected Neural Networks in FPGA for Handwritten Digit Recognition
Luca Saldanha and C Bobda
University of Arkansas
4:20PM
3A.3
Neuromorphic architectures with electronic synapses
S Burc Eryilmaz¹, Siddharth Joshi², Emre Neftci³, Weier Wan¹, Gert Cauwenberghs², H.-S. Wong¹
¹Stanford University, ²University of California, San Diego, ³Department of Cognitive Sciences, University of California Irvine

4:40PM
3A.4
Towards a Scalable Neuromorphic Hardware for Classification and Prediction with Stochastic No-Prop Algorithms
Dan Christiani, Cory Merkel, Dhireesha Kudithipudi
Rochester Institute of Technology

5:00PM
3A.5
High-Performance and Low-Power MPSoC Architectures for Advanced Mobile and Wearable IoT Systems
Lech Jozwiak
Eindhoven University of Technology

SESSION P
Tuesday March 15
Posters

Chair: Brian Cline, ARM
Co-Chair: Kamesh Gadepally, GigaCom Semiconductor

4:40PM
P1
Equivalence Checking between SLM and RTL Using Machine Learning Techniques
Jian Hu¹, Tun Li², Sikun Li²
¹National University of Defense Technology, College of Computer, ²National University of Defense Technology, School of Computer

4:40PM
P2
Very low supply voltage room temperature test to screen low temperature soft blown fuse fails which result in a resistive bridges
Peter Sarson
ams AG
On-Line Harmonic-Aware Partitioned Scheduling For Real-Time Multi-Core Systems Under RMS
Ming Fan¹, Rong Rong², Xinwei Niu³
¹Broadcom Corporation, ²Florida International University, ³Penn State Erie, The Behrend College

CovGen: A Framework for Automatic Extraction of Functional Coverage Models
Eman El Mandouh¹ and Amr G. Wassal²
¹Mentor Graphics Corporate, ²Computer Engineering Dept, Cairo University

In-situ Trojan Authentication for Invalidating Hardware-Trojan Functions
Masaru Oya, Youhua Shi, Masao Yanagisawa, Nozomu Togawa
Waseda University

A 1.3μW, 5pJ/cycle sub-threshold MSP430 processor in 90nm xLP FDSOI for energy-efficient IoT applications
Abhishek Roy¹, Peter Grossmann², Steven Vitale², Benton Calhoun³
¹University of Virginia, ²MIT Lincoln Laboratory, Lexington, MA USA, ³University of Virginia, Charlottesville, VA USA

Statistical Quality Modeling of Approximate Hardware
Seogoo Lee¹, Dongwook Lee², Kyungtae Han³, Emily Shriver¹, Lizy John², Andreas Gerstlauer²
¹The Univeristy of Texas at Austin, ²The University of Texas at Austin, ³Intel Corporation

Performance Evaluation of Stacked Gate-All-Around MOSFETs at 7 and 10 nm Technology Nodes
Meng-Yen Wu and Meng-Hsueh Chiang
National Cheng Kung University

Fast Stress Analysis for Runtime Reliability Enhancement of 3D IC Using Artificial Neural Network
Lang Zhang¹, Hai Wang¹, Sheldon Tan²
¹University of Electronic Science and Technology of China, ²University of California at Riverside

Detection of Malicious Hardware Components in Mobile Platforms
Fatih Karabacak¹, Umit Ogras¹, Sule Ozev²
¹Arizona State University, ²ASU
An Effective BIST Architecture for Power-Gating Mechanisms in Low-Power SRAMs
Alberto Bosio¹, Luigi Dilillo¹, Patrick Girard¹, Arnaud Virazel¹, Leonardo Zordan²
¹LIRMM, ²Intel Mobile Communication

Performance Evaluation Considering Mask Misalignment in Multiple Patterning Decomposition
Haitong Tian and Martin Wong
University of Illinois at Urbana Champaign

UM-BUS: An Online Fault-Tolerant Bus for Embedded Systems
Jiqin Zhou¹, Weigong Zhang², Keni Qiu², Xiaoyan Zhu²
¹Beijing Center for Mathematics and Information Interdisciplinary Sciences, ²College of Information Engineering, Capital Normal University

Low-Leakage and Process-Variation-Tolerant Write-Read Disturb-Free 9T SRAM Cell Using CMOS and FinFETs
Ayushparth Sharma and Kusum Lata
The LNM Institute of Information Technology

Ruggedness evaluation and design improvement of automotive power MOSFETs
Tianhong Ye and Kuan Chee
The University of Nottingham Ningbo China

Device/System Performance Modeling of Stacked Lateral NWFET Logic
Victor Huang¹, Chenyun Pan¹, Azad Naeemi¹, Dmitry Yakimets², Praveen Raghavan²
¹Georgia Institute of Technology, ²imec

Accelerating Physical Level Sub-Component Power Simulation by Online Power Partitioning
Siddharth S. Bhargav, Andrew Kolb, Young H. Cho
University of Southern California

Power Efficient Router Architecture for Wireless Network-on-Chip
Hemanta Kumar Mondal¹, Sri Harsha Gade², Raghav Kishore¹, Shashwat Kaushik¹, Sujay Deb¹
¹IIIT Delhi, ²iiitd.ac.in
4:40PM
P19
Preventing Integrated Circuit Piracy via Custom Encoding of Hardware Instruction Set
Vinay Patil\textsuperscript{1}, Arunkumar Vijayakumar\textsuperscript{2}, Sandip Kundu\textsuperscript{1}
\textsuperscript{1}Department of Electrical and Computer Engineering, University of Massachusetts Amherst, \textsuperscript{2}Department of Electrical and Computer Engineering, University of Massachusetts, Amherst

4:40PM
P20
Preventing Design Reverse Engineering with Recongurable Spin Transfer Torque LUT Gates
Ted Winograd\textsuperscript{1}, Hassan Salmani\textsuperscript{2}, Hamid Mahmoodi\textsuperscript{3}, Houman Homayoun\textsuperscript{1}
\textsuperscript{1}George Mason University, \textsuperscript{2}Howard University, \textsuperscript{3}San Francisco State University

4:40PM
P21
Portable Bio-sensor for Chronic Malaria Detection
Lalitha Sivaraj, nurul amziah md yunus, Mohamad Nazim Mohtar, samsuzana abd aziz, M iqbal saripan, Fakhrul Zaman Rokhani, Zurina Zainal Abidin
University Putra Malaysia

4:40PM
P22
Performance Modeling and Optimization for On-Chip Interconnects in 3D Memory Arrays
Javaneh Mohseni, Chenyun Pan, Azad Naeemi
Georgia Institute of Technology

4:40PM
P23
Near-threshold circuit variability in 14nm FinFETs for ultra-low power applications
Sriram Balasubramanian, Ninad Pimparkar, Mangesh Kushare, Vinayak Mahajan, Juhi Bansal, Takashi Shimizu, Vivek Joshi, Kun Qian, Arunima Dasgupta, Karthik Chandrasekaran, Chad Weintraub, Ali Icel
GLOBALFOUNDRIES

4:40PM
P24
An Efficient Timing Analysis Model for 6T FinFET SRAM using Current-Based Method
Tiansong Cui\textsuperscript{1}, Ji Li\textsuperscript{1}, Alireza Shafaei Bejestan\textsuperscript{1}, Shahin Nazarian\textsuperscript{1}, Massoud Pedram\textsuperscript{2}
\textsuperscript{1}University of Southern California, \textsuperscript{2}USC
SESSION 4A

Wednesday March 16

**Powering IoT**

Chair: Stephen Hienrich-Barna, Texas Instruments
Co-Chair: Charles Augustine, Intel

08:30AM

4A.1 **Energy Harvesting and Power Management Opportunities in IOT**  
*Harish Krishnamurthy, Jason Mix, Lilly Huang, Krishnan Ravichandran*  
Intel

08:50AM

4A.2 **Linear, Point-of-Load Regulators for Fine-Grained Power Management of Digital Circuits**  
*Saad Bin Nasir, Samantak Gangopadhyay, Arijit Raychowdhury*  
Georgia Institute of Technology

09:10AM

4A.3 **Multi-Ratio Switched-Capacitor DC-DC Converters for Power Management Applications**  
*Patrick Mercier and Loai Salem*  
University of California, San Diego

09:30AM

4A.4 **Low-Power Circuit Techniques for IoT Energy Harvesting**  
*Inhee Lee, Wanyeong Jung, Dennis Sylvester, David Blaauw*  
University of Michigan

SESSION 4B

Wednesday March 16

**Enabling 5nm Technology Node**

Chair: Brian Cline, ARM  
Co-Chair: Rajan Beera, Pall Corporation
08:30AM
4B.1
Nanowire Transistor Solutions for 5nm and Beyond
Asen Asenov\textsuperscript{1}, Y Wang\textsuperscript{2}, B Cheng\textsuperscript{1}, X Wang\textsuperscript{3}, P Asenov\textsuperscript{1}, T Al-Ameri\textsuperscript{1}, V. P. Georgiev\textsuperscript{3}
\textsuperscript{1}Gold Standard Simulations, \textsuperscript{2}Peking University, Beijing, \textsuperscript{3}University of Glasgow

08:50AM
4B.2
5nm: Has the Time for a Device Change Come?
Praveen Raghavan, Marie Garcia Bardon, Pieter Schuddinck, Doyoung Jang, Dmitry Yakimets, Rogier Baert, Peter Debacker, Diederik Verkest, Aaron Thean
imec

09:10AM
4B.3
Transistor Design for 5nm and Beyond: Slowing Down Electrons to Speed Up Transistors
Victor Moroz\textsuperscript{1}, Joanne Huang\textsuperscript{1}, Reza Arghavani\textsuperscript{2}
\textsuperscript{1}Synopsys, \textsuperscript{2}Lam Research

09:30AM
4B.4
Decomposition Technologies for Advanced Nodes
Fedor Pikus
Mentor Graphics, Inc

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SESSION 4C

Wednesday March 16

Advanced Testing Concepts

Chair: Vinod Viswanath, Real Intent
Co-Chair: Sreejit Chakravarty, Intel

08:30AM
4C.1
Low Capture Power Dictionary based Test Data Compression
Panagiotis Sismanoglou and Dimitris Nikolos
University of Patras

08:50AM
4C.2
Analysis of Setup & Hold Margins Inside Silicon for Advanced Technology Nodes
Deepak Kumar Arora\textsuperscript{1}, Darayus Adil Patel\textsuperscript{2}, Shahabuddin Qureshi\textsuperscript{1}, Sanjay Kumar\textsuperscript{1}, Navin Kumar Dayani\textsuperscript{1}, Balwant Singh\textsuperscript{1}, Sylvie Naudet\textsuperscript{1}, Arnaud Virazel\textsuperscript{1}, Alberto Bosio\textsuperscript{3}
\textsuperscript{1}STMicroelectronics, \textsuperscript{2}STMicroelectronics / LIRMM, \textsuperscript{3}LIRMM
09:10AM
4C.3
Protocol-Guided Analysis of Post-silicon Traces Under Limited Observability
Hao Zheng¹, Yuting Cao¹, Sandip Ray², Jin Yang²
¹University of South Florida, ²Intel

09:30AM
4C.4
Nonlinear Delay-Table Approach for Full-Chip NBTI Degradation Prediction
Song Bian, Michihiro Shintani, Shumpei Morita, Masayuki Hiromoto, Takashi Sato
Kyoto University

SESSION T34

Wednesday March 16

Tutorial 3 & 4

Chair: Hai (Helen) Li, University of Pittsburgh
Co-Chair: Vinod Viswanth, Real Intent

09:50AM
T3
Low Power SoC System Design – A Systems Approach to Power Management Techniques, Power and Performance Optimizations, Thermal and Energy Management of Systems-on-Chip
Rajiv Muralidhar
Intel

10:50AM
T4
Building neuromorphic computing systems with emerging device technologies
John Strachan
Hewlett Packard Laboratories

SESSION 5A

Wednesday March 16

Embedded Systems

Chair: Yang Yi, University of Kansas
Co-Chair: Rajesh Berigei, Texas Instruments
1:00PM
5A.1
Reliability and Energy-aware Cache Reconfiguration for Embedded Systems
Yuanwen Huang and Prabhat Mishra
University of Florida

1:20PM
5A.2
Architecting STT Last-Level-Cache for Performance and Energy Improvement
Fazal Hameed1 and Mehdi Tahoori2
1Chair of Dependable Nano Computing KIT - Karlsruhe Institute of Technology, 2Karlsruhe Institute of Technology

1:40PM
5A.3
Instruction Cache Aging Mitigation Through Instruction Set Encoding
Anteneh Gebregiorgis1, Fabian Oboril1, Mehdi B. Tahoori1, Said Hamdioui2
1Karlsruhe Institute of Technology, 2Delft University of Technology

2:00PM
5A.4
Nga Dang1, Zana Ghaderi2, Eli Bozorgzadeh1, Moonju Park4
1Google Inc., 2University of California, Irvine, 3Univ. of California, Irvine, 4Incheon National University, South Korea

2:20PM
5A.5
Negotiation-Based Resource Provisioning and Task Scheduling Algorithm for Cloud Systems
Ji Li1, Yanzhi Wang2, Xue Lin1, Shahin Nazarian1, Massoud Pedram3
1University of Southern California, 2Syracuse University, 3USC

SESSION 5B

Wednesday March 16

Hardware and System Security

Chair: Gang Qu, University of Maryland

1:00PM
5B.1
Digital IP Protection Using Threshold Voltage Control
Joseph Davis, Niranjan Kulkarni, Jinghua Yang, Aykut Dengi, Sarma Vrudhula
Arizona State University
1:20PM  
5B.2  
Trojan Detection in Digital Systems Using Current Sensing of Pulse Propagation in Logic Gates  
Sabyasachi Deyati¹, Abhijit Chatterjee², Barry Muldrey¹  
¹Georgia Institute of Technology, ²Georgia Tech

1:40PM  
5B.3  
Active Protection against PCB Physical Tampering  
Steven Paley¹, Tamzidul Hoque², Swarup Bhunia²  
¹Case Western Reserve University, ²University of Florida

2:00PM  
5B.4  
SVM-based Real-Time Hardware Trojan Detection for Many-Core Platform  
Amey Kulkarni¹, Youngok Pino², Tinoosh Mohsenin¹  
¹University of Maryland, Baltimore County, ²Information Sciences Institute, University of Southern California

2:20PM  
5B.5  
On Testing Physically Unclonable Functions for Uniqueness  
Arun Kumar Vijayakumar¹, Vinay Patil², Sandip Kundu¹  
¹Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, ²Department of Electrical and Computer Engineering, University of Massachusetts Amherst

SESSION 5C  
Wednesday March 16  
Analog Design  

Chair: Riaz Naseer, Intel  
Co-Chair: Stephen Hiernich-Barna, Texas Instruments

1:00PM  
5C.1  
Neuromorphic Computing with Resistive Synaptic Arrays: Devices, Circuits and Systems  
Yu Cao¹, Shimeng Yu¹, Yu Wang², Pai-Yu Chen¹, Lixue Xia², Huazhong Yang²  
¹Arizona State University, ²Tsinghua University

1:20PM  
5C.2  
Dot-Product Engine as Computing Memory to Accelerate Machine Learning Algorithms  
Miao Hu, John Paul Strachan, Zhiyong Li, R. Stanley Williams  
Hewlett Packard Labs
1:40PM
5C.3
0.5-V 50-mV-Swing 1.2-GHz 28-nm-FD-SOI 32-bit Dynamic Bus Architecture with Dummy Bus
Khaja Ahmad Shaik, Kiyoo Itoh, Amara Amara
Institut supérieur d'électronique de Paris (ISEP)

2:00PM
5C.4
Analysis and Design of a Triangular Active Charge Injection for Stabilizing Resonant Power Supply Noise
Masahiro Kano, Toru Nakura, Kunihiro Asada
The University of Tokyo

2:20PM
5C.5
An Ultra-fast and Low-power Design of Analog Circuit Network for DoG Pyramid Construction of SIFT Algorithm
Zheyu Liu, Fei Qiao, Qi Wei, Xinghua Yang, Yi Li, Huazhong Yang
Dept.of Electronic Engineering, Tsinghua University

SESSION 6A
Wednesday March 16

Design Optimization for Performance, Reliability, and Yield

Chair: Fedor Pikus, Mentor Graphics
Co-Chair: Vivek Joshi, GlobalFoundries

3:00PM
6A.1
Impact of Interconnect Variability on Circuit Performance in Advanced Technology Nodes
Divya Madapusi Srinivas Prasad, Chenyun Pan, Azad Naeemi
Georgia Institute of Technology

3:20PM
6A.2
Hotspot Detection using Machine Learning
Kareem Madkour¹, Sarah Mohamed¹, Dina Tantawy², Mohab Anis³
¹Mentor Graphics, ²Cairo Univeristy, ³American University in Cairo

3:40PM
6A.3
Efficient Analog Circuit Optimization Using Sparse Regression and Error Margining
Mohamed Baker Alawieh¹, Fa Wang², Rouwaida Kanj³, Xin Li³, Rajiv Joshi³
¹American University of Beirut, ²Carnegie Mellon University, ³IBM
4:00PM

6A.4
State Encoding based NBTI Optimization in Finite State Machines
Shilpa Pendyala and Srinivas Katkoori
University of South Florida Tampa

SESSION 6B

Wednesday March 16

EDA for Design Exploration & Analysis Beyond Moore's Law

Chair: Takashi Sato, Kyoto University
Co-Chair: Ofelya Manukyan, Synopsys

3:00PM

6B.1
Gate Movement for Timing Improvement on Row Based Dual-VDD Designs
Hua Xiang, Lakshmi Reddy, Haifeng Qian, Ching Zhou, Yu-Shiang Lin, Fanchieh Yee, Andrew Sullivan, Pong-Fei Lu
IBM Research

3:20PM

6B.2
Multiple Shift-vector Importance Sampling Method using Support Vector Machine and Clustering for High-Density DRAM Designs
Jinyoung Lee, Sunghee Yun, Jeongha Kim, Dongsoo Kang, Jeongyeol Kim, Sanghoon Lee
Samsung Electronics

3:40PM

6B.3
Fully Automated PLL Compiler Generating Final GDS from Specification
Toru Nakura and Kunihiro Asada
The University of Tokyo

4:00PM

6B.4
AFD-Based Method for Signal Line EM Reliability Evaluation
Zhong Guan\(^1\) and Malgorzata Marek-Sadowska\(^2\)
\(^1\)UC Santa Barbara, ECE department, \(^2\)University of California, Santa Barbara
SESSION 6C

Wednesday March 16

Sensors for IOT

Chair: Kamesh Gadepally, GigaCom Semiconductor
Co-Chair: Charles Augustine, Intel

3:00PM
6C.1
A Smart ECG Sensor with In-Situ Adaptive Motion-Artifact Compensation for Dry-Contact Wearable Healthcare Devices
Shuang Zhu, Jingyi Song, Balaji Chellappa, Ali Enteshari, Tuo Shan, Mengxun He, Yun Chiu
University of Texas at Dallas

3:20PM
6C.2
Making Unreliable Chem-FET Sensors Smart via Soft Calibration
Fatih Karabacak¹, Uwadiae Obahiagbon¹, Umit Ogras², Sule Ozev², Jennifer Blain Christen¹
¹Arizona State University, ²ASU

3:40PM
6C.3
Novel design of a silicon photodetector and its integration in a 4x4 CMOS pixel array
Hari Shanker Gupta¹, Satyajit Mohapatra², Nihar R. Mohapatra², D K Sharma³
¹Space Applications Centre, ²Department of Electrical Engineering, Indian Institute of Technology, Gandhinagar, Ahmedabad, India, ³Department of Electrical Engineering, Indian Institute of Technology, Bombay, Mumbai, India

4:00PM
6C.4
Time-Division Multiple Access Based Intra-body Communication for Wearable Health Tracker
Tan Chee Phang¹, Mohammad Harris Mokhtar², Mohd Nazim Mohtat¹, fakhruul zaman rokhani³
¹University Putra Malaysia, ²Telecom Research