Analysis and Design of a 5G Multi-Mode Power Amplifier using 130 nm CMOS technology

Marwa Mansour [1, 2], Abdelhalim Zekry [2], Mohammed K. Ali [3, 4], and Heba Shawkey [1].
[1]Microelectronics Department, Electronics Research Institute (ERI), Giza, Egypt
[2]Electronics and Communications Department, Faculty of Engineering, Ain shams University, Cairo, Egypt
[3]Electrical Engineering Department, Fayoum University, Fayoum, Egypt
[4]Institute of Electronic Devices and Circuits, University Ulm, Germany
[1]E-mail: marwa_mansour@eri.sci.eg

Abstract

This work proposes a dual-mode radio frequency (RF) power amplifier (PA) for the 4.8 GHz multi-standard applications using a 130 nm CMOS technology. The proposed RF power amplifier (PA) consists of two stages (driver and power). By changing the driver and the power stages bias voltages any mode of PA (class-AB\F) can be achieved. The class-AB or linear mode power amplifier design is appropriate for IoT, LTE, 5G, and multi-standard RF transmitters. Whereas the class-F or switching mode PA is suitable for IoT-LPWAN and Bluetooth applications. The class-AB mode has a saturated output power of 23 dBm at 4.8 GHz, a power-added efficiency (PAE) of 29.5 %, an output third-order intercept point (OIP3) equals 18 dBm, and for LTE 15MHz channel bandwidth the adjacent channel power ratio (ACPR) is -36 dBc. On the other hand, the maximum PAE is 28% and the output power equals 22.3 dBm for the class-F mode. The proposed power amplifier occupies 0.88 mm^2 of the chip area where the active area equals 0.53 mm^2. The power dissipation is 136 mW or 26 mW in the proposed class-AB or class-F PA modes, individually.

Keywords

Class-AB, Class-F, CMOS, Dual-mode, Multi-standard, Power Amplifier (PA), Radio frequency (RF), Reconfigurable, RF Transmitter, UWB.

1. Introduction

A telecommunication standard determines all of the specifics of how a communication system works, such as modulation techniques, bit rate, duplexing, multiple access, frequency band, and channel bandwidth. The modulation techniques are classified into a variable envelope and constant envelope modulation techniques. Systems[1] that use a non-constant envelope modulation scheme require linear power amplifiers [2],[3]. On the other hand, systems that use the constant envelope modulation technique need saturated or switching power amplifiers[3].

The design of dual-band RF front-ends is required for multifunction services and this must also consume low power and achieves good matching. There are several methods for power amplifier design. A 130nm CMOS parallel-cascod linear power amplifier was presented in [4]. It had a high power dissipation of 417.6 mW. A wide bandwidth; 3-5 GHz; linear Power Amplifier was implemented in [5]. It was a single-ended power amplifier, with low output power around 11.3dBm and very low PAE of 14% at 5GHz, and also it consumed low power dissipation of 30.6mW with occupied a large chip area of 1.65 mm2. In [6] a dual-band Power Amplifier was designed with low power added efficiency (PAE) of 10.7% at 9 GHz, dissipation power of 1.3 W, and it occupied a relatively high chip area. Furthermore, a 5.2 GHz push-pull power amplifier (PA) using two on-chip transformers was presented in [7] and achieved a low output power of 16 dBm.

In this work, a dual-mode Class-AB / Class-F radio frequency power amplifier with input and output matching and harmonic termination network is analyzed and designed for the 4.8 GHz frequency band. The harmonic termination networks include a second harmonic series resonant circuit and a third harmonic parallel resonant network. The parallel resonance circuit is used to improve the PAE of the proposed power amplifier. The circuit architecture of the suggested power amplifier is based on that of the class-F power amplifier topology. Moreover, by changing the driver, and power stages bias voltages, the linear or switching operations are selected.

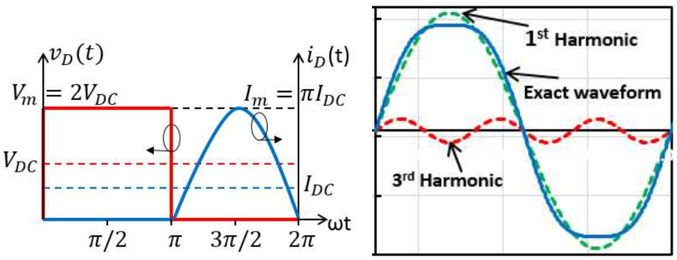
This paper is organized as follows; section 2 presents Class-AB/F background while the proposed Multi-mode RF Power Amplifier is introduced in section 3. Post-layout simulation results are covered in section 4. Finally, section 5 concludes the work.

2. Class AB/F Background

Power amplifiers are often categorized as either linear or switching power amplifiers. In the linear power amplifier, including class A, AB, and B, the current through the output device and the voltage across it have sinusoidal or partially sinusoidal waveforms [8]. Amplifiers in this category have relatively good linearity. But the linear amplifiers have poor efficiency, because of power loss resulting from the current-voltage overlap in the output transistor [9].

To solve the efficiency degradation problem of the amplifiers, nonlinear switching amplifiers are recommended. The switching results in sharp transitions that minimize the current-voltage overlap and hence rise the power efficiency [9]. One of the nonlinear amplifiers is a class F amplifier. The class F operation is specified when square wave voltage and half-rectified sine wave current at the active element output were present as illustrated in Figure 1(a). The voltage waveforms can be shaped into a square wave by managing the odd harmonics, as shown in

Figure 1(b). To appropriately flatten the voltage waveform, the third-harmonic voltage component must have the negative phase concerning the fundamental component as illustrated in Figure 1(b).



i. (b)

Figure 1: (a)Voltage and current waveforms of a Class-F power amplifier, and (b) Shaping of a square waveform by odd harmonic.

Figure 2 presents the normalized amplitudes of the drain current harmonic components at DC, f_o, and $3f_o$ as a function of the conduction angle Class F operation potential only if the device bias point is chosen in the range from device threshold to Class-A[10]. Biasing the device below threshold (Class-C) cannot lead to an appropriate Class-F mode due to in-phase voltage harmonic components. Class-B bias point cannot be selected for a Class-F due to the current waveform does not contain any odd harmonic components. For Class-F operation the conduction angle (α) must be a little above π and the device is biased just above the threshold voltage. For Class-AB operation the conduction angle (α) must be between π and 2π, and the device is biased as well above the threshold.

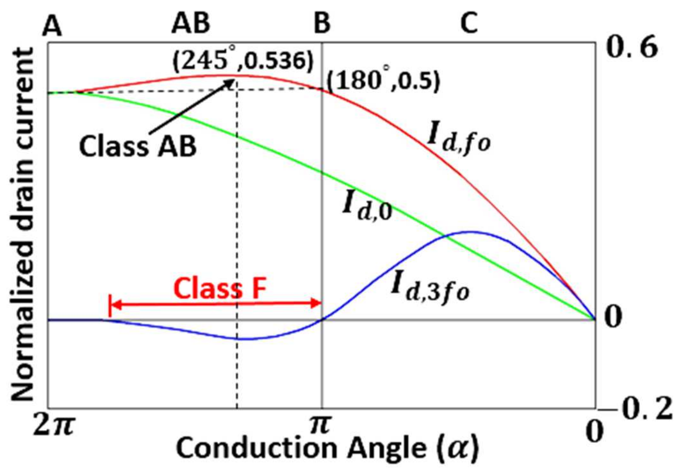


Figure 2: Drain current normalized amplitude harmonic components at DC, f_o , and $3f_o$ with the conduction angle (α).

3. Proposed Multi-mode RF Power Amplifier

The proposed RF power amplifier is cleared in Figure 3. It composes of two stages; driver, and power amplifier stages with input and output matching and harmonic controlling networks . The mode of operation is achieved by changing the driver and the power stages bias voltages of the proposed power amplifier, where $V_{cs} = 0.5\,V$, $V_{cg} = 1.9\,V$ for switching mode (Class-F operation), and $V_{cs} = 0.62\,V$, $V_{cg} = 1.8\,V$ for linear mode (Class-AB operation) as plotted in Figure. 3.

There are two control pins in the proposed power amplifier the first one is Vcg to bias the common gate transistors in the driver and power stages. The second control pin is Vcs to bias the common source transistors in the driver and power stages. Also, the quality factor of the inductors used in the proposed power amplifier is above 10. Table 1 illustrates the design values of the circuit components of the proposed multi-mode power amplifier shown in Figure 3.

Table 1: Design values of the circuit components of the proposed dual mode power amplifier displayed in Figure 3.

Comp.	Transistors ($\frac{W(\mu m)}{L(\mu m)}$)				
	M_1	M_2	M_3	M_4	
Value	$\frac{1536}{0.34}$	$\frac{800}{0.5}$	$\frac{768}{0.34}$	$\frac{1920}{0.5}$	
Comp.	L(nH)	L1(nH)	L2(nH)	L4(nH)	R_b(KΩ)
Value	0.4	0.2	0.15	0.65	15
Comp.	C2(pF)	L3(nH)	C3(pF)	Cs(pF)	C_b(pF)
Value	1.83	0.18	0.7	1.05	10

The Mu factor stability test is used to test the stability of the proposed PA. The stability condition (Mu factor) is calculated by equation (1)

$$Mu = \frac{1-|S_{11}|^2}{|S_{22}-S^*{}_{11}\cdot\Delta|+|S_{12}\cdot S_{21}|} > 1 \quad (1)$$

Where $\Delta = |S_{11}.S_{22} - S_{12}.S_{21}|$ and * means the complex conjugate. From equation (1), the stability of the PA relies on the S-parameters, input, and output matching.

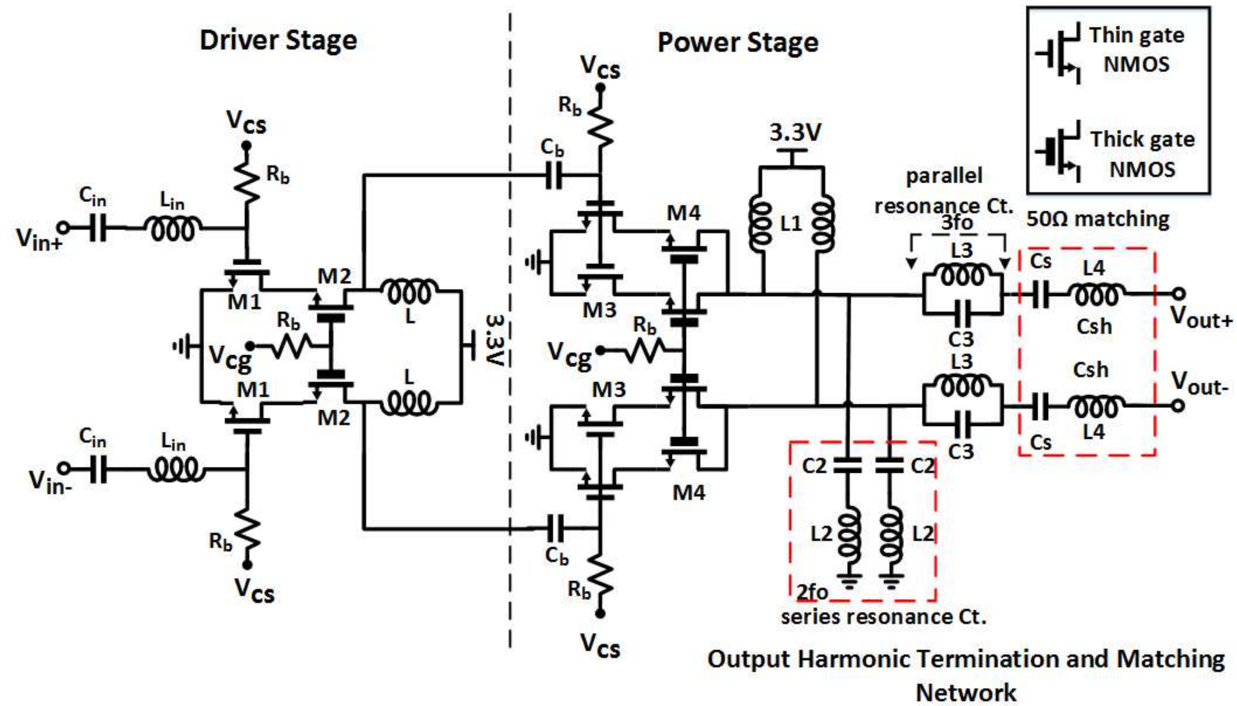


Figure 3: Schematic diagram of the proposed 4.8GHz dual mode Class-AB/Class-F power amplifier.

The simulated Mu stability test of the suggested Multi-mode PA is shown in Figure 4. The input matching is achieved by a series LC matching circuit, and the input return loss is less than -8 dB at 4.8GHz.

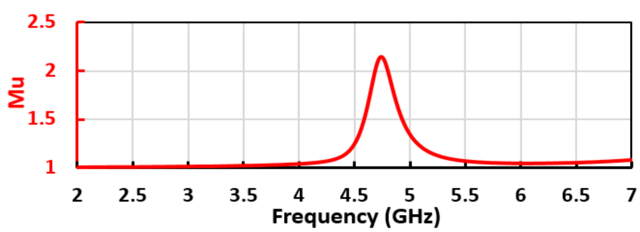


Figure 4: Stability test (Mu) of the proposed multi-mode PA with frequency.

The driver and power stages are cascode amplifier architecture as plotted in Figure 3. The common gate (CG) transistors are thick gate oxide to avoid breakdown issues whereas the common source transistor is a thin gate oxide with a minimum gate length to obtain high gain and excellent RF performance. The power stage is built based on Class-F topology with harmonic controlling and matching circuits, the harmonic termination network composed of series, and parallel resonant networks resonating at the second, and third harmonics, respectively, and an output LC matching network as depicted in Figure 3. The harmonic termination circuit is used to form the voltage waveforms at the drain in order to obtain a suitable ratio of voltage harmonics components [11] as follows: $Z_3 = \infty, Z_2 = 0$

$$C_2 = 1/((2\omega_o)^2\, L_2)\ , and\ C_3 = 1/((3\omega_o)^2\, L_3) \qquad (2)$$

where ω_o is the operating angular frequency.

Harmonic termination networks are used to improve the efficiency of the power amplifier without affecting the linearity of the Class-AB operation of the PA.

4. Post –layout Simulation Results

The proposed multi-mode power amplifier is designed using a 130 nm CMOS technology and simulated using Cadence Design Systems for circuit layout and physical verifications, and Advanced Design System (ADS) for circuit simulation. The layout of the proposed power amplifier is shown in Figure 5, the RF pad, and bypass capacitors at each dc source influence are taken into account for perfect simulation results. The layout is symmetric about its centerline and includes two stages driver, and power stage, where the area of the driver and power stages are 0.14, and 0.25 mm^2, respectively. The total chip area of the proposed power amplifier is 0.88 mm^2 including RF pads, DC pads, and a die area of 0.53 mm^2.

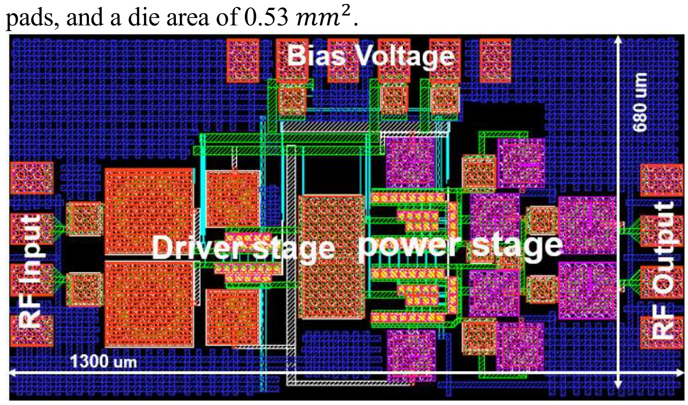


Figure 5: Radio frequency layout of the proposed 4.8 GHz multi-mode power amplifier.

Figure 6 explains a comparison between the suggested Class-AB and Class-F PA modes. The parallel resonance circuit at $3f_o$ (third harmonic open circuit) improves the PAE of the proposed Class-AB PA to be almost equal to the PAE of Class-F mode. Due to the lower bias, the gain of the proposed Class-F PA is lower than that of the proposed Class-AB PA. The proposed Class-AB power amplifier has an output power 0.7 dBm more than the proposed Class-F mode as illustrated in Figure 6.

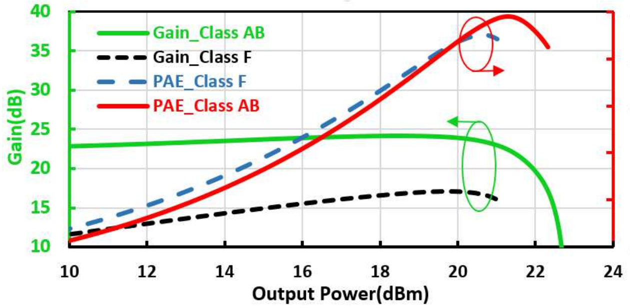
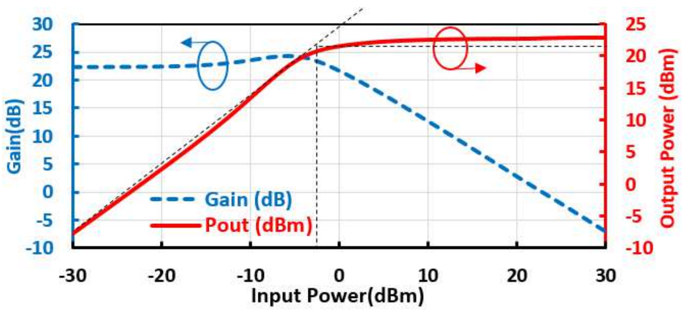
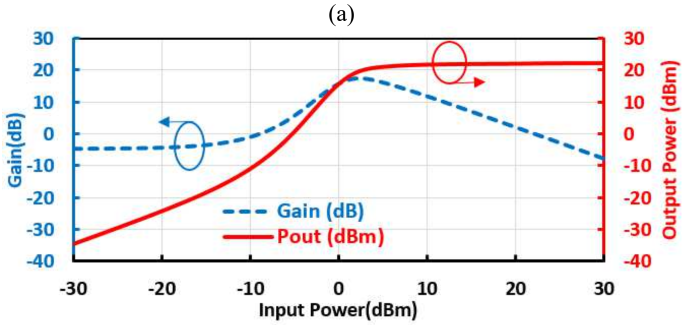


Figure 6: Simulation results of the dual-mode Class-AB/Class-F power amplifier, the gain and the PAE versus output power.

The output power and gain with an input power of the proposed Class-AB PA are shown in Figure 7(a). The proposed Class-AB power amplifier has an output 1-dB compression point (O1dB) of 20.9 dBm. The gain and output power against the input power of the suggested Class-F PA is displayed in Figure 7(b). The proposed Class-F switch from low output power to high output power at input power equals about 0 dBm as plotted in Figure 7(b).



(a)



(b)

Figure 7: Simulated gain and output power with input power for, (a) Suggested Class-AB PA, (b) Proposed Class-F power amplifier.

The linearity of the proposed class-AB power amplifier is depicted in Figure 8, where the output third-order intercept point (OIP3) of the class AB mode is 18 dBm at 4.8 GHz. While the transmitted output spectrum of the suggested Class-AB power amplifier at 4.8 GHz center frequency, and channel bandwidth 15 MHz is plotted in Figure 9, where the adjacent channel power ratio (ACPR) equals -36.036 dBc.

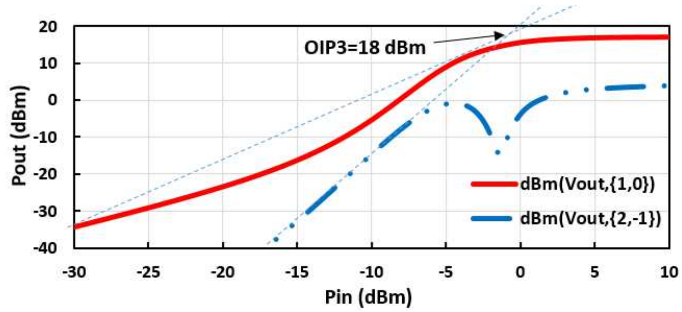


Figure 8: Simulated linearity test of the suggested Class-AB PA.

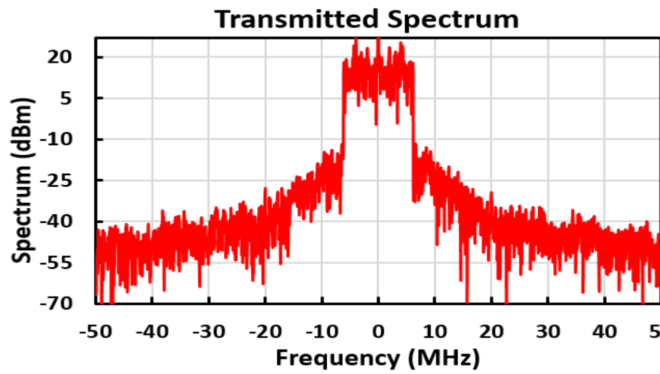


Figure 9: Transmitted output spectrum of the suggested Class-AB power amplifier at 4.8GHz frequency band for 15 MHz channel bandwidth of LTE.

Table 2 clarifies the harmonics power levels of the proposed Class-AB and Class-F PA. Because of using the harmonic termination networks (short circuit of the second harmonic component and open circuit of the third harmonic component), low harmonics power levels are presented in the proposed Class-AB and Class-F PA.

Table 2: Power levels of the harmonic components for the proposed power amplifier at 4.8 GHz.

Mode of operations	Pout (dBm)	@ $2f_o(dBc)$	@ $3f_o(dBc)$
Class F mode	22.25	-34.024	-26.24
Class AB mode	22.94	-45.33	-27.92

The proposed dual band PA shows comparable performances to the reported PAs implemented using CMOS technology concerning the mode of operation, output power, PAE, dissipated power, and area as illustrated in Table 3.

5. Conclusion

A multi-mode power amplifier in 130nm CMOS technology with input, output matching, and harmonic termination network at 4.8GHz is proposed. The proposed PA operates in the linear mode or switching mode, by changing the biasing voltage of the driver and the output stages. The input matching is implemented by the series LC matching. In the linear operation, it obtains an output power that equals 23 dBm and peak PAE of 29.5 % whereas, in the switching mode, the maximum saturated power is 22.3 dBm with peak a PAE of 28.6 %. Lastly, the active area of the proposed power amplifier is compacted compared to recently published papers and equals $0.53mm^2$.

Table 3: Performance comparison of linear and switch mode power amplifiers implemented in CMOS technology.

Index	This work		[4]	[5]	[6]	[7]
Freq.(GHz)	4.8		5	3-5	3/9	5.2
Technology	130 nm		130 nm	180 nm	180 nm	180nm
Mode	Linear	Switch	Linear	Linear	Linear	Push pull PA
P_{OUTSAT}(dBm)	23	22.3	18.5	11.3 Output P1dB	24.8/21.5	16
PAE_{Peak} (%)	29.5	28.6	13.3	14 @ 5GHz	32.8/10.7	30.9
P_{DC} of all PA	136mW for class-AB 26mW for class-F		417.6mW	30.6mW	236/365mA 3.6V	NA
Die area (mm^2)	0.53		0.62	1.65	1.06/0.79	0.5
Fully integration	YES		YES	YES	NO	YES
ACPR (dBc)	-36/15MHz channel BW		NA	NA	NA	NA
Results	Post Layout Simulation		Measured	Measured	Measured	Measured

6. References

[1] M. Mansour, A. Zekry, and R.S. Ghoname, “Building Radio Frequency Transmitter for LTE User Equipment,” Journal of Communications on Applied Electronics (CAE) , vol. 2, no.4 ,pp. 1-9, 2015.

[2] E. McCune, “High-efficiency, multi-mode, multi-band terminal power amplifiers,” IEEE Microwave Magazine, vol. 6, no. 1, pp. 44–55, Mar. 2005.

[3] M. Mansour, A. Zekry, M. K. Ali, and H. Shawkey, “A Reconfigurable Class-AB/F Power Amplifier for 0.1-4.2GHz Multistandard Applications”, Circuits, Systems, and Signal Processing, Published: 24 August 2020.

[4] S. Kang, D. Baek and S. Hong, "A 5-GHz WLAN RF CMOS Power Amplifier With a Parallel-Cascoded Configuration and an Active Feedback Linearizer," in IEEE Transactions on Microwave Theory and Techniques, vol. 65, no. 9, pp. 3230-3244, Sept. 2017.

[5] S. Wong, S. Maisurah, M. N. Osman, F. Kung and J. See, “High Efficiency CMOS Power Amplifier for 3 to 5 GHz Ultra-Wideband (UWB) Application,” in IEEE Transactions on Consumer Electronics, vol. 55, no. 3, pp. 1546-1550, August 2009.

[6] J. Ko and S. Nam, “A Two-Stage S-/X-Band CMOS Power Amplifier for High-Resolution Radar Transceivers,” IEEE Microw.Wireless Compon. Lett., vol. 28, no. 7, pp. 606-608, July 2018.

[7] T. Sadakiyo and H. Kanaya, "Development of highly efficient push-pull power amplifier with center tapped transformer for 5GHz application," 2017 IEEE 19th Electronics Packaging Technology Conference (EPTC), Singapore, 2017, pp. 1-4.

[8] B. Razavi, RF Microelectronics. Upper Saddle River, NJ: Prentice Hall, 2012.

[9] H. L. Kraus, C. W. Bostian, and F. H. Raab, Solid State Radio Engineering.New York: Wiley, 1980.

[10] P. Colantonio, F. Giannini, G. Leuzzi, and E. Limiti, “On the class-F power amplifier design,” Int. J. RF Microw. Comput.-Aided Eng., vol. 9, no. 2, pp. 129-149, 1999.