Abstract—This manuscript investigates the performance of HJ-ADG-DLTFET considering temperature variations from 200 K - 500 K and by varying Interface Trap Charges (ITC) density of negative (NITC) as well as positive polarity (PITC) by utilizing Silvaco ATLAS. This is done by evaluating analog/RF performance parameters such as transconductance ($g_m$), cut-off frequency ($f_c$) and Device efficiency (DE). Furthermore, temperature variations for the range from 200 – 500 K demonstrate the degradation of the off-state current of HJ-ADG-DLTFET. Also, DE enhances at low temperatures.

I. Introduction

Dopingless Tunnel FETs have been advancing as an appropriate replacement for Metal-Oxide-Semiconductor-Field-Effect-Transistors (MOSFETs) [1]. With that in mind, the reliability of TFET needs to be evaluated as TFET has different carrier injection mechanism and structural similarity of TFET and MOSFET does not guarantee reliability. Therefore, in this work, the authors have investigated the reliability of HJ-ADG-DLTFET in terms of ITC and temperature variations. The ITC originate due to process and radiation methods across interfaces. Here, ITC density is chosen in support with several published experimental and simulation reports and taken as $10^{12}$ cm$^{-2}$ to investigate with minimum deviation for ITC density for both i.e. NITC sand PITC. Withal, there is a need to evaluate the influence of temperature on HJ-ADG-DLTFET owing to semiconductor bandgap dependence on temperature, and increment in operating temperature resulting from increased chip density. Additionally, device needs to function properly in extreme conditions in several applications such as satellites, space, automotive, wireless/mobile, military and aircraft technologies.

II. Device Details

Fig. 1(a) displays the cross-sectional view of HJ-ADG-DLTFET, in which electron plasma is formed at drain by using 4.6 eV electrode, and hole plasma is formed in source section with 5.93 eV electrode on the intrinsic semiconductor body. The fundamental parameter comparison study for HJ-ADG-DLTFET and ADG-DLTFET has been reported in our earlier published work [2] with device simulation parameters and methodology. The comparative interfacial trap charge analysis of HJ-ADG-DLTFET with ADG-DLTFET has also been reported by authors in [3].

III. Results and Discussions

Fig.1(b) illustrates the influence of different ITC density on the $I_{ON}-V_{G0}$ characteristics and $g_m$ of HJ-ADG-DLTFET w.r.t. $V_{G0}$ at room temperature. The results demonstrate that the increment (decrement) in the PITC (NITC) enhances (reduces) the flat band voltage, and consequently, improves (worsens) the band bending of the conduction band and the valence band, following the lowering (increasing) of the tunneling barrier width. Consequently, the drain current increases (decreases) with the impact of PITC (NITC). It is evident from Fig. 1(b) that when PITC (NITC) is introduced at the semiconductor-dielectric, non-local BTBT increase (decreases), and hence $g_m$ increase (decrease). The high value of $g_m$ at higher gate bias demonstrates improved responsiveness for the translation of $V_{G0}$ into $I_0$, better linearity as higher derivatives of $g_m$ contribute towards linearity performance, and superior high-frequency attributes. Fig.1(c) illustrates the outcome of various ITC density on the device efficiency (DE) and $f_t$ of HJ-ADG-DLTFET in response to the applied gate voltage, at room temperature. It is demonstrated in Fig. 1(c) that DE (i.e., $g_m$) achieves a maximum at a small gate bias and then reduces as the gate bias is further increased due to small variations of drain current in the saturation region. The DE increases (decreases) due to the impact of PITC (NITC) due to more extensive variation in the drain current ($I_{ON}$) in correspondence to the $g_m$ with PITC (NITC). Additionally, Fig.1(c) illustrates that as the $V_{G0}$ increases, $f_t$ increases owing to the increment in $g_m$. Furthermore, $f_t$ increases (decreases) with PITC (NITC). Fig. 1(d) explains the deviation of drain and $g_m$ w.r.t. the applied $V_{G0}$, for the temperature range (200–500 K) at $N_i = 0$ cm$^{-2}$ (WITC), $N_i = 10^{12}$ cm$^{-2}$ (PITC) and at $N_i = -1 \times 10^{12}$ cm$^{-2}$ (NITC) respectively. It is apparent from Fig. 1(d), that temperature susceptibility on the $I_{ON}-V_{G0}$ characteristics relies on the applied bias, as a result of the different carrier transport scheme in the off-state (Shockley-read-hall (SRH) recombination) and on-state (band-to-band-tunneling). The $I_{ON}$ increases exponentially with rising temperature because Shockley-read-hall (SRH) recombination has an exponential temperature dependence at low $V_{G0}$. However, at high gate voltage, BTBT leads over SRH and results in small increments in the drain current. As HJ-ADG-DLTFET illustrates the increment of the drain current with increasing temperature, $g_m$ also shows increment with the temperature. Fig. 1(e) illustrates the deviation of $f_t$ and DE in accordance with the applied gate voltage, for the temperature range (200–500 K). The HJ-ADG-DLTFET illustrates the positive temperature co-efficient of the drain current. Consequently, $f_t$ increases with temperature as a result of the increment in the $I_0$ and $g_m$.

IV. Conclusion

This paper circumscribes the impact of ITC and temperature variations on HJ-ADG-DLTFET on a simulation basis for analog/RF applications. Additionally, HJ-ADG-DLTFET appears to have a positive temperature coefficient for drain current, and hence for $g_m$ and $f_t$ as well, for complete gate bias range. However, the presence of ITC does not affect much the temperature variations of the HJ-ADG-DLTFET, which proves the reliability of the device in the temperature-sensitive environment considering ITC variations.

References