

WELCOME TO ISQED'23

Greetings,

On behalf of the ISQED conference and technical committees, we are thrilled to welcome you to the 24th anniversary of the International Symposium on Quality Electronic Design, ISQED'23. After several years of virtual events due to the COVID pandemic, we are excited to announce that this year's event will be held in-person at the Seven Hills Conference Center, located in San Francisco State University, 800 Font Blvd, San Francisco, CA 94132.

For over two decades, ISQED has been the leading voice and pioneer in the field of Quality Electronic Design (QED). With the increasing complexity of semiconductor technology and design, it is more essential than ever before to follow QED and its underlying principles. ISQED'23 aims to lead the community in this direction with an extensive program consisting of keynotes, panels, tutorials, and over 100 peer-reviewed articles.

This year, the conference will be conducted virtually, with the technical sponsorship of the IEEE Electron Devices Society, the IEEE Circuits and Systems Society, IEEE Reliability Society, and in-cooperation with ACM/SigDA. Conference proceedings and papers will be published in IEEE Xplore digital library and indexed by Scopus.

ISQED'23 is organized around critical trends in AI/ML, Autonomous Vehicles, Security, IoT, and Quantum Computing. The conference program includes two keynote speeches, two embedded tutorials, a panel discussion, and numerous peer-reviewed technical papers that focus on these timely topics.

We are delighted to report that the number of quality papers submitted to the conference this year has been overwhelming. The two and a half-day technical program features four parallel sessions and over 100 peer-reviewed papers highlighting the latest trends in electronic circuit and system design and automation, testing, verification, sensors, security, semiconductor technologies, cyber-physical systems, and more.

All technical presentations, plenary sessions, panel discussions, tutorials, and related events will take place virtually on April 5-7, at Pacific Daylight Time (PDT).

We would like to take this opportunity to express our gratitude to the corporate sponsors of ISQED'23: Synopsys and Innovotek for their invaluable financial support of this conference.

General Chair
Sara Tehranipoor
West Virginia University

Program Chair
Cindy Yi
Virginia Tech

Program Co-Chair
Deliang Fan
Arizona State University

Special Sessions Chair
Hossein Sayadi
California State University, Long Beach

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Mimi Xie
The University of Texas at San Antonio

Tutorials Chair
Vita Pi-Ho Hu
National Taiwan University

Tutorials Co-Chair
Xiaolin Xun
Northeastern University

Panels Chair
Tosiron Adegbija,
University of Arizona

Panels Co-Chair
Fareena Saqib
University of North Carolina

Publication Chair
Paul Wesling
Hewlett Packard (retired)

ISQED Founder & Chair
Ali A. Iranmanesh
Silicon Valley Polytechnic Institute

ISQED'23 Best Papers

2A.3

DC-Model: A New Method for Assisting the Analog Circuit Optimization

*Yuan Wang, Jian Xin, Haixu Liu, Qian Qin, Chenkai Chai, Yukai Lu,
Jinglei Hao, Jianhao Xiao, Zuochang Ye, Yan Wang*
Tsinghua University, Beijing, China

6A.1

An Area Efficient Superconducting Unary CNN Accelerator

*Patricia Gonzalez-Guerrero, Kylie Huch, Nirmalendu Patra, Thom Popovici,
George Michelogiannakis*
Lawrence Berkeley National Laboratory, Berkeley, USA

Authors of best papers are acknowledged during the morning plenary session on Wednesday April 5.
ISQED'23 best papers are sponsored by Innovotek Inc.

ISQED'23 Organizing Committee

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Sara Tehranipoor
West Virginia University

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Cindy Yi
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Program Co-Chair
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Tosiron Adegbija,
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University of Tokyo

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Zhen Zhou, Intel Corp (Co-Chair)

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Hongyu An - Michigan Technological University
Kang Jun Bai - Air Force Research Laboratory
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Xin Fu - University of Houston
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Ishan Thakkar - University of Kentucky

TECHNICAL PROGRAM COMMITTEES

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Deliang Fan - Arizona State University

Dhruva Ghai - ORIENTAL UNIVERSITY INDORE

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Shih-Hsu Huang - Chung Yuan Christian University

Sheikh Ariful Islam - University of Texas Rio Grande Valley

Anand Iyer - Microsoft

Yu-Min Lee - National Yang Ming Chiao Tung University

Jerome Lescot - ST Microelectronics

Rung-Bin Lin - Yuan Ze University

Bin Lin - Cadence Design Systems

Murthy Palla - Synopsys Inc.

Chidhambaranathan Rajamanikkam - Synopsys

Andre Reis - UFRGS

Emre Salman - Stony Brook University

Takashi Sato - Kyoto University

Jia Wang - Illinois Institute of Technology

Hua Xiang - IBM Research

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Rui Zhang - Cadence Design Systems

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Serge Demidenko - Sunway University

Deliang Fan - Arizona State University

Patrick Girard - LIRMM / CNRS

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Dimitris Nikolos - University of Patras

Ernesto Sanchez - Politecnico di Torino

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Miroslav Velev - Aries Design Automation

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Hana Kubatova - CTU in Prague

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Vittorio Ferrari - University of Brescia

Tobias Gemmeke - RWTH Aachen University

Na Gong - University of South Alabama

Zhong Guan - UC Santa Barbara

Ankur Guha Roy - Broadcom Inc.

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Manjunath Kareppagoudr - Advanced Micro Devices inc

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Rakesh Kumar - Ampere Computing

Joshua Lee - Institute of Microelectronics (A*STAR)

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Mohamed El-Hadedy - CalPoly Pomona

Ava Hedayatipour - CSULB

Chen Pan - Texas A&M University-Corpus Christi

Richard Yarnell - University of Central Florida

Baogang Zhang - University of Central Florida

WIP - Work in Progress

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Sara Tehranipoor - West Virginia University

TECHNICAL PROGRAM COMMITTEES

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Zhijie Shi - University of Connecticut

Dominik Sisejkovic - Corporate Research Robert Bosch GmbH, Germany

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Cindy Yang Yi - Virginia Tech

Jiliang Zhang - Hunan University

Emerging Device and Process Technologies and Applications (EDPT)

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Arijit Banerjee - Advanced Micro Devices

Rajan Beera - Pall Corporation

Atul Bhargava - STMicroelectronics

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Masoud Zabihi - Northeastern University

GENERAL INFORMATION

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ISQED'23

April 5-7, 2023

Seven Hills Conference Center
San Francisco State University

AWARDS & RECOGNITIONS

Wednesday April 5, 8:40 AM - 9:00 AM

Track A - Nob Hill Room

Best Paper Awards

Recipients of the ISQED'23 Best Paper Awards will be recognized in this segment of the program. The best papers are shown in Page 2 of this document.

Keynotes

Keynote 1P.1

Wednesday, April 6, 9:00 AM - 9:35 AM

The Weakest Link: Microelectronics Security Against Physical Attacks

Prof. Domenic Forte
University of Florida

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Keynote 2P.1

Thursday April 6, 9:00 AM - 9:35 AM

Pushing the Energy-efficiency of Deep Learning Accelerators with Hardware-Software Co-design

Dr. Rangharajan Venkatesan
NVIDIA

Panel Discussion **Sponsored by Synopsys**

Wednesday, April 5, 3:15 PM - 4:45 PM

Track A - Nob Hill Room

Driving the Future: Exploring the Intersection of AI and Autonomous Vehicles

Two rapidly emerging technologies, Artificial Intelligence (AI) and autonomous vehicles (AV), are poised to revolutionize everyday life. Industries worldwide are investing billions of dollars to advance these transformative technologies, which have seen remarkable advancements over the past few decades. However, we have only scratched the surface of their potential impact on society. This panel will feature experts in the fields of AI and AVs who will discuss the current trends in AV, with a focus on leveraging advancements in AI to accelerate the development of AV. The panel will explore topics such as the reality of AI-driven electronic design, short-term and long-term predictions of how AI and AV will interact and their potential impact, security considerations in AI-driven AV design, practical research challenges and gaps, and potential directions for addressing these gaps.

Panelists:

Yankin Tanurhan - Synopsys
Ravikumar Chakaravarthy - AMD
Pratik Prabhanjan Brahma - Cruiz
Daryush Laqab - NVIDIA

Moderator:

Pallab Chatterjee - Roadway Media

Chairs:

Tosiron Adegbiya - University of Arizona (Chair)
Fareena Saqib - University of North Carolina (Co-Chair)

GENERAL INFORMATION

Embedded Tutorials

Chair & Moderators:

Vita Pi-Ho Hu - National Taiwan University (Chair)

Xiaolin Xun - Northeastern University (Co-Chair)

Track A - Nob Hill Room

Tutorial 1

Wednesday, April 5, 12:25 PM - 1:25 PM

Design Automation for Learning-Enabled Cyber-Physical Systems

Prof. Qi Zhu

Northwestern University

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Tutorial 2

Thursday April 6, 1:05 PM - 2:05 PM

Introduction to Quantum Computing: from Algorithm to Hardware

Prof. Hiu Yung Wong

San Jose State University

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TECHNICAL SESSIONS

There are a total of 20 paper sessions held on Wednesday to Friday. Technical sessions are held in the format of three parallel tracks **A, B, C** located respectively in Nob Hill Room, Russian Hill Room, and Mt. Davidson room.

ON-SITE REGISTRATION

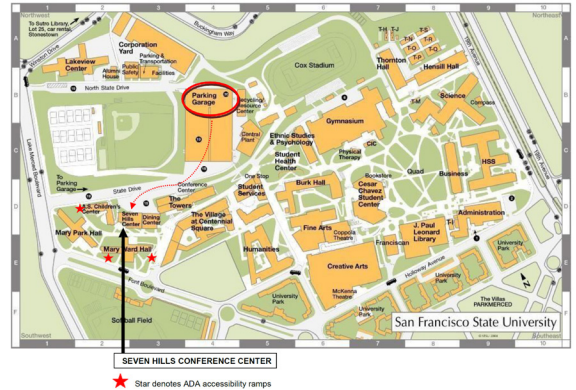
Tentative time schedule of on-site registration is as follows:

Wednesday, April 5, 8:00 AM - 2:00 PM

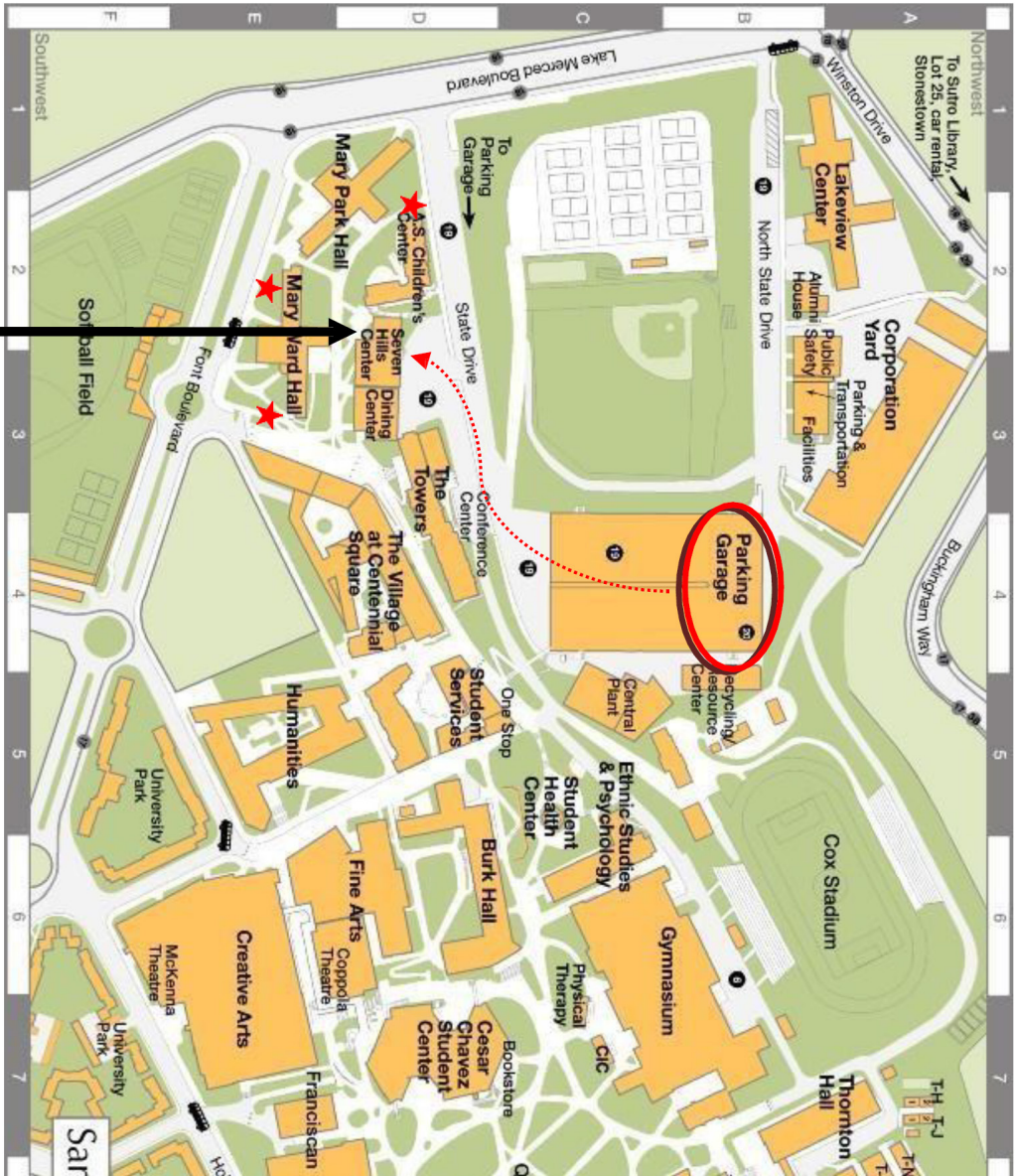
Thursday, April 6, 8:00 AM - 12:00 PM

Registration desk location will be at the conference center lobby.

Seven Hills Conference Center Map



UNIVERSITY MAP & CONFERENCE CENTER LOCATION+



SEVEN HILLS CONFERENCE CENTER

★ Star denotes ADA accessibility ramps

PROGRAM AT A GLANCE

WEDNESDAY APRIL 5

Wednesday, April 5, 2023

Please note all shown times are Pacific Daylight Time (PDT)

8:40am-9:00am	Plenary Session 1: (Nob Hill Room)		
	Introduction, Committee Recognitions, Best Paper Awards		
	Keynote: The Weakest Link: Microelectronics Security Against Physical Attacks Prof. Domenico Forte - University of Florida		
	9:35am-10:10am		
10:10am-10:20am	Break		
10:20am-11:40am	Session 1A (Nob Hill Room) Next Generation Computing Systems	Session 1B (Russian Hill Room) Design for Testability and Verification	Session 1C (Mt. Davidson Room) AI Applications in Computing System Design
11:40am-12:25pm	ISQED Luncheon		
12:25pm-13:25am	Embedded Tutorial 1 Design Automation for Learning-Enabled Cyber-Physical Systems <u>Presenter:</u> Prof. Qi Zhu - Northwestern University		
13:25pm-13:30pm	Break		
13:30pm-15:10pm	Session 2A (Nob Hill Room) Advances in Circuit and Physical Design	Session 2B (Russian Hill Room) Recent Advances in Secure Hardware Design	Session 2C (Mt. Davidson Room) Efficiency and Reliability of Memory
15:10pm-15:15pm	Break		
15:15pm-16:45pm	Panel Discussion - (Nob Hill Room) Driving the Future: Exploring the Intersection of AI and Autonomous Vehicles		

PROGRAM AT A GLANCE

THURSDAY APRIL 6

Thursday, April 6, 2023

Please note all shown times are Pacific Daylight Time (PDT)

8:45am-9:00am	Plenary Session 2: (Nob Hill Room)		
9:00am-9:35am	Welcome		
	Keynote: Pushing the Energy-efficiency of Deep Learning Accelerators with Hardware-Software Co-design Dr. Rangharajan Venkatesan - NVIDIA		
9:35am-9:40am	Break		
10:20am-11:40am	Session PW1 (Nob Hill Room) Poster & WIP Session 1	Session PW2 (Russian Hill Room) Poster & WIP Session 2	Session PW3 (Mt. Davidson Room) Poster & WIP Session 3
	Break		
11:40am-11:45am			
11:45am-12:25pm	Session 3A (Nob Hill Room) ML based CAD for Optimization	Session 3B (Russian Hill Room) AI Accelerator Hardware Design	Session3C (Mt. Davidson Room) Intelligent Edge Computing
	Lunch Break		
12:25pm-13:05			
13:05pm-14:05pm	Embedded Tutorial 2 (Nob Hill Room) Introduction to Quantum Computing: from Algorithm to Hardware <i>Presenter:</i> Prof. Hiu Yung Wong - San Jose State University		
	Break		
14:05pm-14:10pm			
14:10pm-15:50pm	Session 4A (Nob Hill Room) Advances in Analysis, Simulation and Computing	Session 4B (Russian Hill Room) Hardware Security: Attacks and Defenses	Session 4C (Mt. Davidson Room) Design for Heterogeneous Integration

Friday, April 7, 2023

Please note all shown times are Pacific Daylight Time (PDT)

9:00am-10:40am	Session 5A (Nob Hill Room) Low Power Circuit Design	Session 5B (Russian Hill Room) Advance secure circuits and Hardware Trojan Detection	Session 5C (Mt. Davidson Room) Efficient Algorithm, Hardware, and Computing Paradigm for Machine Learning
	Break		
10:40am-10:45am			
10:45am-12:05pm	Session 6A (Nob Hill Room) Design of Emerging Circuits & Systems	Session 6B (Russian Hill Room) Novel AI Computing	Session 6C (Mt. Davidson Room) Security for Resource-Limited Devices

FRIDAY APRIL 7

Wednesday April 5

9:00 AM - 9:35 AM

Room: Nob Hill

The Weakest Link: Microelectronics Security Against Physical Attacks



Prof. Domenic Forte
University of Florida

For the past decade and a half, the hardware security community has expended significant time on threats related to semiconductor globalization. With the passage of the CHIPS Act in the US and similar legislation around the world, untrusted foundries should no longer be considered the weakest link. It is time to refocus efforts towards physical attacks against microelectronics. Physical attacks exist across a wide spectrum – from low-cost/low-reward non-invasive attacks to high-cost/high-reward invasive attacks – and have successfully extracted on-chip assets and broken roots-of-trust in recent years. Some non-invasive attacks have even found success remotely. Further, the threat of semi-invasive attacks, such as optical probing, is growing. Semi-invasive attacks are low in cost like non-invasive attacks but nearly as powerful as invasive attacks. This keynote will review this dangerous landscape and discuss emerging approaches that bolster physical security. It is said that “Time is what determines security. With enough time nothing is unhackable.” Hence, more attention will be paid to techniques that quantifiably increase the time and complexity of physical attacks.

About Domenic Forte

Domenic Forte is an Associate Professor and the Steven A. Yatauro Faculty Fellow with the Electrical and Computer Engineering Department at University of Florida. He is also Associate Director for the Florida Institute for National Security (FINS). His research covers the domain of hardware security from transistors to printed circuit boards where he has over 200 publications. Dr. Forte is a senior member of the IEEE, a member of the ACM, and serves or has served on the technical program committees of leading events such as USENIX Security, NDSS, HOST, ASHES, DAC, ICCAD, ITC, ISTFA, and BTAS. Dr. Forte is a recipient of the Presidential Early Career Award for Scientists and Engineers (PECASE), the NSF CAREER Award, and the ARO Young Investigator Award. His research has also been recognized with best paper awards and nominations from IJCB, ISTFA, HOST, DAC, and AHS. For teaching and advising, he has received the Herbert Wertheim College of Engineering Doctoral Dissertation Advisor/Mentoring Award, the Excellence in Teaching Award from UF's ECE Graduate Student Organization, and the George Corcoran Outstanding Teaching Award from University of Maryland.

Thursday April 6

9:00 AM - 9:35 AM

Room: Nob Hill

Pushing the Energy-efficiency of Deep Learning Accelerators with Hardware-Software Co-design



Dr. Rangharajan Venkatesan

NVIDIA

Deep neural networks (DNNs) have emerged as a key approach to solving complex problems across many application spaces, including image recognition, natural language processing, robotics, health care, and autonomous driving. Designing custom hardware accelerators for deep neural networks is highly promising, as they offer significant performance and power advantages compared to general-purpose processors. This talk presents MAGNet, a hardware-software co-design framework that explores different data formats, quantization techniques, memory hierarchies, and dataflows. This talk describes a new data format VS-Quant for achieving low-precision computation and novel multi-level dataflows to improve energy efficiency.

About Rangharajan Venkatesan

Rangharajan Venkatesan is a Senior Research Scientist in the ASIC & VLSI Research group in NVIDIA. He received the B.Tech. degree in Electronics and Communication Engineering from the Indian Institute of Technology, Roorkee in 2009 and the Ph.D. degree in Electrical and Computer Engineering from Purdue University in August 2014. His research interests are in the areas of low-power VLSI design and computer architecture with a particular focus in deep learning accelerators. He has received Best Paper Awards for his work on deep learning accelerators from IEEE/ACM Symposium on Microarchitecture (MICRO) and Journal of Solid-State Circuits (JSSC). His work on spintronic memory design was recognized with the Best Paper Award at the International Symposium on Low Power Electronics and Design (ISLPED), and Best paper nomination at the Design, Automation and Test in Europe (DATE). His paper titled, "MACACO: Modeling and Analysis of Circuits for Approximate Computing", received the IEEE/ACM International Conference on Computer-Aided Design (ICCAD) Ten Year Retrospective Most Influential Paper Award in 2021. He has served as a member of the technical program committees of several leading IEEE/ACM conferences including ISSCC, DAC, MICRO, and ISLPED.

Panel Discussion

Wednesday April 5

3:15 PM–4:45 PM

Room: Nob Hill

Driving the Future: Exploring the Intersection of AI and Autonomous Vehicles

Summary:

Two rapidly emerging technologies, Artificial Intelligence (AI) and autonomous vehicles (AV), are poised to revolutionize everyday life. Industries worldwide are investing billions of dollars to advance these transformative technologies, which have seen remarkable advancements over the past few decades. However, we have only scratched the surface of their potential impact on society. This panel will feature experts in the fields of AI and AV who will discuss the current trends in AV, with a focus on leveraging advancements in AI to accelerate the development of AV. The panel will explore topics such as the reality of AI-driven electronic design, short-term and long-term predictions of how AI and AV will interact and their potential impact, security considerations in AI-driven AV design, practical research challenges and gaps, and potential directions for addressing these gaps.

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Ravikumar Chakaravarthy - AMD

Daryush Laqab - NVIDIA

Pratik Prabhanjan Brahma - Cruise

Moderator:

Pallab Chatterjee - Roadway Media

Panel Committee:

Tosiron Adegbija - University of Arizona (Chair)

Fareena Saqib - University of North Carolina, Charlotte (Co-Chair)

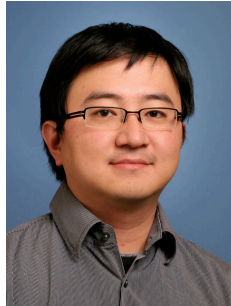
Embedded Tutorial 1

Wednesday April 5

12:25 AM - 1:25 PM

Nob Hill Room

Design Automation for Learning-Enabled Cyber-Physical Systems



Prof. Qi Zhu

Northwestern University

Summary:

Future learning-enabled cyber-physical systems (LE-CPSs), such as self-driving cars and robotic systems, will employ complex machine learning-based sensing, computation and communication components for their perception, prediction, planning, control, and coordination. However, ensuring their safety, robustness and security faces tremendous challenges, given the highly dynamic and uncertain environment they operate within, the fast increase of their functional and architectural complexity, the difficulty in analyzing deep neural network-based components, and the often-stringent resource and timing constraints. This calls for new design automation methodologies and tools that support rigorous, accurate and efficient modeling, synthesis, verification, and adaptation of LE-CPSs. In this tutorial, using connected and autonomous vehicles (CAVs) as an example, I will discuss these challenges and present some of our recent work to address them in a holistic manner, including 1) end-to-end verification, design and adaptation methods for ensuring robust and safe application of neural networks in perception and decision making; and 2) cross-layer methods based on weakly-hard paradigm for mitigating execution disturbances (e.g., timing violations, soft errors, malicious attacks).

About Qi Zhu

Qi Zhu is an Associate Professor at the ECE Department in Northwestern University. He received a Ph.D. in EECS from University of California, Berkeley in 2008, and a B.E. in CS from Tsinghua University in 2003. His research interests include design automation for cyber-physical systems (CPS) and Internet of Things, safe and secure machine learning for CPS and IoT, cyber-physical security, and system-on-chip design, with applications in domains such as connected and autonomous vehicles, energy-efficient smart buildings, and robotic systems. He is a recipient of the NSF CAREER award, the IEEE TCCPS Early-Career Award, and the Humboldt Research Fellowship for Experienced Researchers. He received best paper awards at DAC 2006, DAC 2007, ICCPS 2013, ACM TODAES 2016, and DATE 2022. He is the Conference Chair of IEEE TCCPS, and VP of Young Professionals at IEEE CEDA. He is an Associate Editor for IEEE TCAD, ACM TCPS, and IET Cyber-Physical Systems: Theory & Applications, and has served as a Guest Editor for the Proceedings of the IEEE, ACM TCPS, IEEE T-ASE, Elsevier JSA, and Elsevier Integration, the VLSI journal.

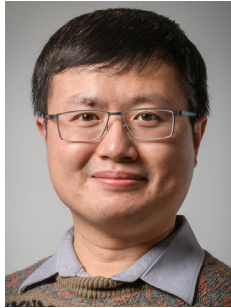
Embedded Tutorial 2

Thursday April 6

1:05 PM - 2:05 PM

Nob Hill Room

Introduction to Quantum Computing: from Algorithm to Hardware



Prof. Hiu Yung Wong
San Jose State University

Summary:

Quantum computing is expected to change the world by providing exponential speed-up in solving some very difficult problems. In this tutorial, we will first discuss the fundamental principles of quantum computing algorithms. We will run one of the basic quantum algorithms, the Deutsch algorithm, on IBM's quantum computer to further appreciate the origin of speed-up and the limitations in quantum computers. Error correction, which is essential to realize a fault-tolerant quantum computer, will be briefly covered. Finally, using the superconductor-based quantum computer as an example, we will study how to implement the essential operations in quantum computers, namely, qubit initialization, readout, and manipulations. It will be appreciated that powerful classical computers, which are used to control the qubits, are essential to the successful implementation of quantum computers.

About Hiu Yung Wong

Hiu Yung Wong is an Associate Professor and Silicon Valley AMDT Endowed Chair in Electrical Engineering, at San Jose State University. He received his Ph.D. degree in Electrical Engineering and Computer Science from the University of California, Berkeley in 2006. From 2006 to 2009, he worked as a Technology Integration Engineer at Spansion. From 2009 to 2018, he was a TCAD Senior Staff Application Engineer at Synopsys. He received the Curtis W. McGraw Research Award from ASEE Engineering Research Council in 2022, the NSF CAREER award and the Newnan Brothers Award for Faculty Excellence in 2021, and Synopsys Excellence Award in 2010. He is the author of the book, "Introduction to Quantum Computing: From a Layperson to a Programmer in 30 Steps". He is one of the founding faculties of the Master of Science in Quantum Technology at San Jose State University. His research interests include the application of machine learning in simulation and manufacturing, cryogenic electronics, quantum computing, and wide bandgap device simulations. His works have produced 1 book, 1 book chapter, more than 100 papers, and 10 patents.

SESSION 1A

Wednesday April 5

Next Generation Computing Systems

Chair: **Arnab Raha**, Intel

Co-Chair: **Kang Jun Bai**, AFRL

10:20AM

1A.1

38 **A SPICE-based Framework to Emulate Quantum Circuits with classical LC Resonators**

Md Mazharul Islam¹, Shafayat Hossain², Ahmedullah Aziz³

¹The University of Tennessee, ²Princeton University, ³University of Tennessee, Knoxville

10:40AM

1A.2

152 **Metal Inter-layer Via Keep-out-zone in M3D IC: A Critical Process-aware Design Consideration**

Madhava Sarma Vemuri and Umamaheswara Tida

North Dakota State University

11:00AM

1A.3

94 **AGNI: In-Situ, Iso-Latency Stochastic-to-Binary Number Conversion for In-DRAM Deep Learning**

Supreeth Mysore Shivanandamurthy, Sairam Sri Vatsavai, Ishan Thakkar, sayedahmad salehi

University of Kentucky

11:20AM

1A.4

50 **Design and Evaluation of multipliers for hardware accelerated on-chip EdDSA**

Harshita Gupta¹, Mayank Kabra², Nitin Patwari³, Prashanth H C⁴, Madhav Rao⁵

¹Thapar institute of information technology, Patiala, ²Student, ³Student, IIITB, ⁴IIIT-Bangalore, ⁵International Institute of Information Technology-Bangalore

SESSION 1B

Wednesday April 5

Design for Testability and Verification

Chair: **Chidhambaranathan R**, Synopsys

10:20AM

1B.1

120 **Self-Checking Performance Verification Methodology for Complex SoCs**

Prakash Ghosh¹, Aditya Chopra¹, Dwaraka Pai², Baljinder Sood²

¹NXP Semiconductor Inc, USA, ²NXP Semiconductors Inc, USA

10:40AM

1B.2

22 **Polynomial Formal Verification of a Processor: A RISC-V Case Study**

Lennart Weingarten¹, Alireza Mahzoon¹, Mehran Goli¹, Rolf Drechsler²

¹University of Bremen, ²University of Bremen/DFKI

11:00AM

1B.3

150 **Application of Machine Learning for Quality Risk Factor Analysis of Electronic Assemblies**

Brendan Reidy¹, David Duggan¹, Bernard Glasauer², Peng Su², Ramtin Zand¹

¹University of South Carolina, ²Component Engineering, Juniper Networks

11:20AM

1B.4

70 **Quality-driven Design Methodology for PUFs in FPGAs for Secure IoT**

Xiangyun Wang¹, Yicheng Song¹, Katyayani Prakash¹, Zeljko Zilic¹, Tomas Langsetmo²

¹McGill University, ²KNOX Industries Inc.

SESSION 1C

Wednesday April 5

AI Applications in Computing System Design

Chair: **Hossein Sayadi**, California State University, Long Beach

10:20AM

1C.1

- 174 **HD2FPGA: Automated Framework for Accelerating Hyperdimensional Computing on FPGAs**

Tianqi Zhang¹, Sahand Salamat², Behnam Khaleghi², Justin Morris³, Baris Aksanli⁴, Tajana Rosing¹

¹UCSD, ²University of California, San Diego, ³CSUSM, ⁴San Diego State University

10:40AM

1C.2

- 114 **XOR-CiM: An Efficient Computing-in-SOT-MRAM Design for Binary Neural Network Acceleration**

Mehrdad Morsali¹, Ranyang Zhou¹, Sepehr Tabrizchi², Arman Roohi³, Shaahin Angizi¹

¹New jersey Institute of Technology, ²University of Nebraska–Lincoln, ³University of Nebraska - Lincoln

11:00AM

1C.3

- 117 **Security and Reliability Challenges in Machine Learning for EDA: Latest Advances**

Zhiyao Xie, Tao Zhang, Yifeng Peng

Hong Kong University of Science and Technology

11:20AM

1C.4

- 187 **Image-Based Zero-Day Malware Detection in IoMT Devices: A Hybrid AI-Enabled Method**

Zhangying He and Hossein Sayadi

California State University, Long Beach

SESSION 2A

Wednesday April 5

Advances in Circuit and Physical Design

Chair: **Rui Zhang**, Cadence Inc.

Co-Chair: **Sheikh Ariful Islam**, University of Texas Rio Grande Valley

1:30PM

2A.1

101 **Routability-aware Placement Guidance Generation for Mixed-size Designs**

Chieh-Yu Cheng and Ting-Chi Wang

National Tsing Hua University

1:50PM

2A.2

103 **MC-MCF: A Multi-Capacity Model for Ordered Escape Routing**

Zhenyi Gao, Sheqin Dong, Zhicong Tang, Wenjian Yu

Tsinghua University

2:10PM

2A.3

137 **DC-Model: A New Method for Assisting the Analog Circuit Optimization**

Yuan Wang, Jian Xin, Haixu Liu, Qian Qin, Chenkai Chai, Yukai Lu, Jinglei Hao, Jianhao

Xiao, Zuochang Ye, Yan Wang

Tsinghua University

2:30PM

2A.4

146 **Accounting for Floorplan Irregularity and Configuration Dependence in FPGA Routing Delay Models**

Gabriel Barajas¹, Jonathan Greene², Fei Li¹, James Tandon³

¹Microchip, ²Cambios Computing LLC, ³California State University East Bay

2:50PM

2A.5

171 An Effective Cost-Skew Tradeoff Heuristic for VLSI Global Routing

Andrew Kahng¹, Shreyas Thumathy², Mingyu Woo³

¹UCSD CSE and ECE Departments, ²Canyon Crest Academy, ³UCSD ECE Department

SESSION 2B

Wednesday April 5

Recent Advances in Secure Hardware Design

Chair: **Soheil Salehi**, University of Arizona

1:30PM

2B.1

Automated Supervised Topic Modeling Framework for Hardware Weaknesses

14 *Rakibul Hassan¹, Charan Bandi¹, Meng-Tien Tsai², Shahriar Golchin³, Sai Manoj Pudukotai Dinakarrao¹, Setareh Rafatirad², Soheil Salehi⁴*

¹George Mason University, ²University of California Davis, ³University of Arizona, ⁴Department of Electrical and Computer Engineering, University of Arizona

1:50PM

2B.2

19 Polymorphic Sensor to Detect Laser Logic State Imaging Attack

Sourav Roy¹, Shahin Tajik², Domenic Forte¹

¹University of Florida, ²Worcester Polytechnic Institute

2:10PM

2B.3

122 Low Overhead System-Level Obfuscation through Hardware Resource Sharing

Daniel Xing¹, Michael Zuzak², Ankur Srivastava¹

¹University of Maryland, ²Rochester Institute of Technology

2:30PM

2B.4

79 SPRED: Spatially Distributed Laser Fault Injection Resilient Design

tasnuva farheen¹, Shahin Tajik², Domenic Forte¹

¹University of Florida, ²Worcester Polytechnic Institute

2:50PM

2B.5

98 Enlarging Reliable Pairs via Inter-Distance Offset for a PUF Entropy-Boosting Algorithm

Md Omar Faruque and Wenjie Che

New Mexico State University

SESSION 2C

Wednesday April 5

Efficiency and Reliability of Memory

Chair: **Hongyu An**, Michigan Technological University

1:30PM

2C.1

49 eDRAM-OESP: A novel performance efficient in-embedded-DRAM-compute design for on-edge signal processing application

Mayank Kabra¹, Prashanth H C², Kedar Deshpande¹, Madhav Rao³

¹Student, ²IIT-Bangalore, ³International Institute of Information Technology-Bangalore

1:50PM

2C.2

115 CMDS: Cross-layer Dataflow Optimization for DNN Accelerators Exploiting Multi-bank Memories

Man Shi¹, Steven Coleman¹, Charlotte VanDeMierop¹, Antony Joseph², Maurice Meijer², Wim Dehaene¹, Marian Verhelst¹

¹KU Leuven, ²NXP Semiconductor

2:10PM

2C.3

127 **HIE-DRAM: High-Performance Efficient In-DRAM Computing Architecture for SIMD**

Mayank Kabra¹, Prashanth H C², Kedar Deshpande¹, Madhav Rao³

¹Student, ²IIT-Bangalore, ³International Institute of Information Technology-Bangalore

2:30PM

2C.4

168 **AGRAS: Aging and memory request rate aware scheduler for PCM memories**

Aswathy NS¹ and Hemangee Kapoor²

¹IIT Guwahati, ²Indian Institute of Technology Guwahati

SESSION PW1

Thursday April 6

PW1

Chair: **Sara Tehranipoor**, West Virginia University

9:40AM

PW1.1

4 **Accurate Estimation of Circuit Delay Variance with Limited Monte Carlo Simulations Using Bayesian Inference**

Chithira R.

National Institute of Technology Calicut

9:45AM

PW1.2

9 **DSEAdd: FPGA based Design Space Exploration for Approximate Adders with Variable Bit-precision**

Archie Mishra and Nanditha Rao

IIT Bangalore

9:50AM

PW1.3

Emerging Interconnect Exploration for SRAM Application Using Nonconventional H-Tree and Center-Pin Access

- 18 *Zhenlin Pei¹, Mahta Mayahinia², Hsiao-Hsuan Liu³, Mehdi Tahoori², Shairfe Salahuddin⁴, Francky Catthoor⁴, Zsolt Tokei⁴, Chenyun Pan⁵*

¹The University of Texas at Arlington, ²Karlsruhe institute of technology (KIT), ³Katholieke Universiteit Leuven (KU Leuven), ⁴IMEC, ⁵University of Texas at Arlington

9:55AM

PW1.4

A Low-overhead PUF-based Secure Scan Design

- 23 *Wei Zhou¹, Aijiao Cui¹, Cassi Chen², Gang Qu³*

¹Harbin Institute of Technology (Shenzhen), ²University of California, Berkeley, ³University of Maryland

10:00AM

PW1.5

- 31 **Deep Image Segmentation for Defect Detection in Photo-lithography Fabrication**

Omari Paul¹, Sakib Abrar¹, Richard Mu¹, Riadul Islam², Manar Samad¹

¹Tennessee State University, ²University of Maryland at Baltimore County

10:05AM

PW1.6

- 36 **Performance Analysis of Cylindrical Through Silicon Via with Interfacial Crack**

Vandana Kumari, Maya Chandrakar, Manoj Majumder

IIIT Naya Raipur

10:10AM

PW1.7

A Flexible Cluster Tool Simulation Framework with Wafer Batch Dispatching Time Recommendation

- 54 *Hsin-Ping Yen¹, Shiuan-Hau Huang¹, Yan-Hsiu Liu², Kuang-Hsien Tseng², Ji-Fu Kung², Yi-Ting Li¹, Yung-Chih Chen³, Chun-Yao Wang⁴*

¹National Tsing Hua University, ²United Microelectronics Corporation, ³National Taiwan University of Science and Technology, ⁴Dept. CS, National Tsing Hua University

10:15AM

PW1.8

- 59 **Hardware Performance Counter Enhanced Watchdog for Embedded Software Security**

Karl Ott¹ and Rabi N. Mahapatra²

¹Texas A&M University, ²Professor

10:20AM

PW1.9

- 60 **Power Savings in USB Hubs Through a Proactive Scheduling Strategy**

Bikrant Das Sharma¹, Abdul Ismail², Chris Meyers³

¹Rice University, ²Intel Corporation, USB Implementers Forum, ³Fresco Logic

10:25AM

PW1.10

- 63 **DK Lock: Dual Key Logic Locking Against Oracle-Guided Attacks**

Jordan Maynard¹ and Amin Rezaei²

¹California State University Long Beach, ²California State University, Long Beach

SESSION PW2

Thursday April 6

PW2

Chair: **Cindy Yi**, Virginia Tech

Co-Chair: **Kang Jun Bai**, AFRL

9:40AM

PW2.1

- 69 **Reproducing Fear Conditioning of Rats with Unmanned Ground Vehicles and Neuromorphic Systems**

Noah Zins and Hongyu An

Michigan Technological University

9:45AM

PW2.2

71 High-Throughput Hardware Implementation for Haraka in SPHINCS+

Yueqin Dai, Yifeng Song, Jing Tian, Zhongfeng Wang

Nanjing University

9:50AM

PW2.3

Analysis of Machine Learning Techniques for Time Domain Waveform Prediction in Analog and Mixed Signal Integrated Circuit Verification

74 *Dhanasekar V¹, Vinodhini Gunasekaran¹, Anusha Challa¹, Bama Srinivasan¹, Dhurga Devi J¹, Selvi Ravindran¹, Ranjani Parthasarathi¹, Ramakrishna P V¹, Gopika Geetha Kumar², Venkateswaran Padmanabhan³, Guha Lakshmanan³, Lakshmanan Balasubramanian³*

¹College of Engineering Guindy, Anna University, ²Carnegie Mellon University, Pennsylvania, ³Texas Instruments (India) Pvt. Ltd.

9:55AM

PW2.4

Focusing on the Key Suspicious Trojan Nets with a Collaborative Approach

75 *Shih-Lung Pao¹, Chuan-Pin Huang¹, Yen-Chi Peng¹, Ing-Jer Huang²*

¹Department of Computer Science and Engineering, National Sun Yat-Sen University, ²Department of Computer Science and Engineering, Digital Content and Multimedia Technology Research Center, National Sun Yat-Sen University

10:00AM

PW2.5

CMP-SiL: Confidential Multi Party Software-in-the-Loop Simulation Framework

134 *Shalabh Jain¹, Pradeep Pappachan¹, Jorge Guajardo², Sven Trieflinger³, Indrasen Raghupatruni³, Thomas Huber³*

¹Robert Bosch LLC, ²Bosch Research and Technology Center, Robert Bosch LLC, ³Robert Bosch GmbH

- 10:05AM
PW2.6
81 **A2OP: an A* Algorithm Optimizer with the Heuristic Function for PCB Automatic Routing**
Quanbao Guo and Keni Qiu
Capital Normal University
- 10:15AM
PW2.7
82 **Decomposable Architecture and Fault Mitigation Methodology for Deep Learning Accelerators**
Ning-Chi Huang¹, Min-Syue Yang¹, Ya-Chu Chang¹, Kai-Chiang Wu²
¹Department of Computer Science, National Yang Ming Chiao Tung University, ²Department of Computer Science, National Chiao Tung University
- 10:20AM
PW2.8
97 **NetViz: A Tool for Netlist Security Visualization**
James Geist¹, Travis Meade¹, Shaojie Zhang¹, Yier Jin²
¹University of Central Florida, ²University of Florida
- 10:25AM
PW2.9
102 **A True Random Number Generator for Probabilistic Computing using Stochastic Magnetic Actuated Random Transducer Devices**
Ankit Shukla¹, Laura Heller¹, Md Golam Morshed², Laura Rehm³, Avik Ghosh², Andrew Kent³, Shaloo Rakheja¹
¹University of Illinois at Urbana-Champaign, ²University of Virginia, ³New York University
- 10:30AM
PW2.10
108 **Attributed Graph Transformation for Generating Synthetic Benchmarks for Hardware Security**
Juneeth kumar Meka and Ranga Vemuri
University of Cincinnati

SESSION PW3

Thursday April 6

PW3

Chair: **Vidya Chhabria**, Arizona State University

9:40AM

PW3.1

- 112 **Secure Control Loop Execution of Cyber-Physical Devices Using Predictive State Space Checks**

Kwondo Ma¹, Chandramouli Amarnath¹, Abhijit Chatterjee¹, Jacob Abraham²

¹Georgia Institute of Technology, ²University of Texas at Austin

9:45AM

PW3.2

- 131 **Cryogenic In-memory Binary Multiplier Using Quantum Anomalous Hall Effect Memories**

Arun Govindankutty¹, Shamiul Alam², Sanjay Das¹, Ahmedullah Aziz², Sumitha George¹

¹North Dakota State University, ²The University of Tennessee, Knoxville

9:50AM

PW3.3

- 140 **SQRTLIB : Library of Hardware Square Root Designs**

Prashanth H C¹, Sriniketh S S², Shrikrishna Hebbar², Chinmaye R², Madhav Rao³

¹IIT-Bangalore, ²RVCE, ³International Institute of Information Technology-Bangalore

9:55AM

PW3.4

- 148 **Binary Synaptic Array for Inference and Training with Built-in RRAM Electroforming Circuit**

Ashvinikumar Dongre and Gaurav Trivedi

Indian Institute of Technology Guwahati India

10:00AM

PW3.5

149 **Neural Network Partitioning for Fast Distributed Inference**

Robert Viramontes and Azadeh Davoodi

University of Wisconsin - Madison

10:05AM

PW3.6

155 **DAGGER: Exploiting Language Semantics for Program Security in Embedded Systems**

Garett Cunningham, Harsha Chenji, Gordon Stewart, David Juedes, Avinash Karanth

Ohio University

10:10AM

PW3.7

156 **Exploiting Programmable Dipole Interaction in Straintronic Nanomagnet Chains for Ising Problems**

Nastaran Darabi¹, Maeesha Binte Hashem¹, Supriyo Bandyopadhyay², Amit Trivedi¹

¹University of Illinois at Chicago, ²Virginia Commonwealth University

10:15AM

PW3.8

157 **A Bit-Parallel Deterministic Stochastic Multiplier**

Sairam Sri Vatsavai and Ishan Thakkar

University of Kentucky

10:20AM

PW3.9

158 **ACPC: Covert Channel Attack on Last Level Cache using Dynamic Cache Partitioning**

Jaspinder Kaur¹ and Shirshendu Das²

¹Indian Institute of Technology Ropar, ²Indian Institute of Technology Hyderabad

10:25AM

PW3.10

169 **Intrinsic Parameter Fluctuation and Process Variation Effect of Vertically Stacked Silicon Nanosheet Complementary Field-Effect Transistors**

Sekhar Kola, Yiming Li, Min-Hui Chuang

National Yang Ming Chiao Tung University

10:30AM

PW3.11

176 SpotOn: A Gradient-based Targeted Data Poisoning Attack on Deep Neural Networks

Yash Khare¹, Kumud Lakara², Sparsh Mittal³, Arvind Kaushik⁴, Rekha Singhal⁵

¹Amrita Vishwa Vidyapeetham, ²Manipal Institute of Technology, ³IIT Roorkee, ⁴NXP Semiconductors, ⁵TCS Research

SESSION 3A

Thursday April 6

ML based CAD for Optimization

Chair: **Murthy Palla**, Synopsys Inc.

Co-Chair: **Rui Zhang**, Cadence Inc.

10:45AM

3A.1

29 PreAxC: Error Distribution Prediction for Approximate Computing Quality Control using Graph Neural Networks

Lakshmi Sathidevi¹, Abhinav Sharma², Nan Wu³, Xun Jiao⁴, Cong "Callie" Hao¹

¹Georgia Institute of Technology, ²Indian Institute of Information Technology, Guwahati, ³UC Santa Barbara, ⁴Villanova University

11:05AM

3A.2

86 DeepAxe: A Framework for Exploration of Approximation and Reliability Trade-offs in DNN Accelerators

Mahdi Taheri¹, Mohamad Riazati², Mohammad Hasan Ahmadilivani³, Maksim Jenihhin³, Masoud Daneshtalab², Jaan Raik⁴, Mikael Sjödin², Björn Lisper²

¹PhD researcher at Tallinn university of Technology, ²Mälardalen University, Västerås, ³Tallinn University of Technology, Tallinn, Estonia, ⁴Tallinn University of Technology, Tallinn

11:25AM

3A.3

- 121 **TOTAL: Topology Optimization of Operational Amplifier via Reinforcement Learning**

Zihao Chen, Songlei Meng, Fan Yang, Li Shang, Xuan Zeng
Fudan University

11:45AM

3A.4

- 154 **Design of Hardware Accelerators to Compute Parametric Capacitance Tables**

Sandeep Koranne
Mentor Graphics Corporation

12:05PM

3A.5

- 175 **Dilated Involutional Pyramid Network (DInPNet): A Novel Model for Printed Circuit Board (PCB) Components Classification**

Ananya Mantravadi¹, Dhruv Makwana², Sai Chandra Teja R², Sparsh Mittal³, Rekha Singhal⁴

¹IIT Raichur, ²Independent Researcher, ³IIT Roorkee, ⁴TCS Research

SESSION 3B

Thursday April 6

AI Accelerator Hardware Design

Chair: **Kang Jun Bai**, AFRL

Co-Chair: **Ji Li**, MicroSoft

10:45AM

3B.1

- 51 **An Optical XNOR-Bitcount Based Accelerator for Efficient Inference of Binary Neural Networks**

Sairam Sri Vatsavai, Venkata Sai Praneeth Karempudi, Ishan Thakkar
University of Kentucky

11:05AM

3B.2

- 160 **Heterogeneous Multi-Functional Look-Up-Table-based Processing-in-Memory Architecture for Deep Learning Acceleration**
Sathwika Bavikadi¹, Purab Ranjan Sutradhar², Amlan Ganguly², Sai Manoj Pudukotai Dinakarrao¹
¹George Mason University, ²Rochester Institute of Technology

11:25AM

3B.3

- 135 **HFGCN: High-speed and Fully-optimized GCN Accelerator**
MinSeok Han¹, Jiwan Kim¹, Donggeon Kim¹, Hyunuk Jeong¹, Gilho Jung¹, Myeongwon Oh¹, Hyundong Lee², Yunjeong Go², HyunWoo Kim¹, Jongbeom Kim¹, Taigon Song¹
¹Kyungpook National University (KNU), ²Kyungpook National University

11:45AM

3B.4

- 90 **Knowledge Distillation between DNN and SNN for Intelligent Sensing Systems on Loihi Chip**
Shiya Liu¹ and Yang Yi²
¹EMD Electronics, ²Virginia Tech

12:05PM

3B.5

- 142 **Lightweight Instruction Set for Flexible Dilated Convolutions and Mixed-Precision Operands**
Simon Friedrich¹, Shambhavi Balamuthu Sampath², Robert Wittig¹, Manoj Rohit Vemparala³, Nael Fafous³, Emil Matus⁴, Walter Stechele⁵, Gerhard Fettweis¹
¹TU Dresden, ²BMW, ³BMW AG, ⁴Technische Universität Dresden, ⁵TUM

SESSION 3C

Thursday April 6

Intelligent Edge Computing

Chair: **Hossein Sayadi**, California State University, Long Beach

10:45AM

3C.1

- 186 **PriML: An Electro-Optical Accelerator for Private Machine Learning on Encrypted Data**

Mengxin Zheng¹, Fan Chen¹, Lei Jiang¹, Qian Lou²

¹Indiana University Bloomington, ²University of Central Florida

11:05AM

3C.2

- 191 **ISSAC: An Self-organizing and Self-healing MAC Design for Intermittent Communication Systems**

Ruben Dominguez¹, Wen Zhang¹, Hongzhi Xu², Pablo Rangel³, Chen Pan⁴

¹Texas A&M University - Corpus Christi, ²Jishou University, ³Texas A&M University - Corpus Christi, ⁴Texas A&M University-Corpus Christi

11:25AM

3C.3

- 188 **A Deep Learning Approach for Ventricular Arrhythmias Classification using Microcontroller**

Ya-sine Agrignan¹, Shanglin Zhou¹, Jun Bai¹, Sahidul Islam², Sheida Nabavi¹, Mimi Xie², Caiwen Ding¹

¹University of Connecticut, ²University of Texas at San Antonio

11:45AM

3C.4

- 189 **Reinforcement Learning-Based Guidance of Autonomous Vehicles**

Joseph Clemmons and Yufang Jin

University of Texas at San Antonio

SESSION 4A

Thursday April 6

Advances in Analysis, Simulation and Computing

Chair: **Chidhambaranathan Rajamanikkam**, Utah State University
Co-Chair: **Anand Iyer**, Synopsys Inc.

2:10PM

4A.1

24 **Fast Electromigration Simulation for Chip Power Grids**

Bijan Shahriari and Farid Najm

University of Toronto

2:30PM

4A.2

93 **On-Interposer Decoupling Capacitors Placement for Interposer-based 3DIC**

Po-Yang Chen, Chang-Yun Liu, Hung-Ming Chen, Po-Tsang Huang

National Yang Ming Chiao Tung University

2:50PM

4A.3

96 **Analysis of Pattern-dependent Rapid Thermal Annealing Effects on SRAM Design**

Vidya Chhabria¹ and Sachin S. Sapatnekar²

¹Arizona State University, ²University of Minnesota

3:10PM

4A.4

109 **Reverse Engineering Word-Level Models from Look-Up Table Netlists**

Ram Venkat Narayanan, Aparajithan Nathamuni-Venkatesan, Kishore

Pula, Sundarakumar Muthukumaran, Ranga Vemuri

University of Cincinnati

3:30PM

4A.5

- 92 **Novel Implementation of High-Performance Polynomial Multiplication for Unified KEM Saber based on TMVP Design Strategy**

Pengzhou He and Jiafeng Xie

Villanova University

SESSION 4B

Thursday April 6

Hardware Security: Attacks and Defenses

Chair: **Soheil Salehi**, University of Arizona

2:10PM

4B.1

Unraveling Latch Locking Using Machine Learning, Boolean Analysis, and ILP

- 39 *Dake Chen¹, Xuan Zhou¹, Yinghua Hu¹, Yuke Zhang¹, Kaixin Yang¹, Andrew Rittenbach², Pierluigi Nuzzo¹, Peter Beere³*

¹University of Southern California, ²USC Information Sciences Institute, ³Univ. of Southern California

2:30PM

4B.2

Resynthesis-based Attacks Against Logic Locking

- 141 *Felipe Almeida¹, Levent Aksoy¹, Quang-Linh Nguyen², Sophie Dupuis², Marie-Lise Flottes³, Samuel Pagliarini⁴*

¹Tallinn University of Technology, ²LIRMM, ³LIRMM CNRS, ⁴Tallinn University of Technology (TalTech)

2:50PM

4B.3

VAST: Validation of VP-based Heterogeneous Systems against Availability Security

167 Properties using Static Information Flow Tracking

Ece Demirhan Coskun¹, Muhammad Hassan¹, Mehran Goli², Rolf Drechsler²

¹Cyber-Physical Systems, DFKI GmbH, ²Institute of Computer Science, University of Bremen

3:10PM

4B.4

41 MAAS: Hiding Trojans in Approximate Circuits

Qazi Arbab Ahmed¹, Muhammad Awais¹, Marco Platzner²

¹Paderborn Univeristy, ²Paderborn University

3:30PM

4B.5

106 Efficient Decryption Architecture for Classic McEliece

Xinyuan Qiao, Suwen Song, Jing Tian, Zhongfeng Wang

Nanjing University

SESSION 4C

Thursday April 6

Design for Heterogeneous Integration

Chair: **Gina Adam**, George Washington University

2:10PM

4C.1

182 Testbench on a Chip: A Yield Test Vehicle for Resistive Memory Devices

Luke Upton¹, Guenole Lallement¹, Michael Scott¹, Joyce Taylor², Robert Radway¹, Dennis Rich¹, Mark Nelson³, Subhasish Mitra¹, Boris Murmann¹

¹Stanford University, ²Intrinsix Corporation, ³SkyWater Technology

2:30PM

4C.2

- 183 **Integrating emerging devices with CMOS for analog in-memory computing**

Qiangfei Xia

University of Massachusetts Amherst

2:50PM

4C.3

- 184 **Integrating Emerging Memories for Analog DNN Accelerators**

An Chen

IBM

3:10PM

4C.4

- 185 **An Infrastructure for Large-scale Reconfigurable Neuronal Network Emulations**

Gopabandhu Hota and Gert Cauwenberghs

UC San Diego

SESSION 5A

Friday April 7

Low Power Circuit Design

Chair: **Amit Trivedi**, University of Illinois at Chicago

Co-Chair: **Hongyu An**, Michigan Technological University

9:00AM

5A.1

- 173 **A Novel Pseudo-Flash Based Digital Low Dropout (LDO) Voltage Regulator**

Cheng-Yen Lee¹, Sunil Khatri¹, Sarma Vrudhula²

¹Texas A&M University, ²Arizona State University

9:20AM

5A.2

20 A Low Power SRAM with Fully Dynamic Leakage Suppression for IoT Nodes

Jun Yin and Mircea Stan

University of Virginia

9:40AM

5A.3

118 Error Diluted Approximate Multipliers Using Positive And Negative Compressors

Bindu G Gowda¹, Prashanth H C², Madhav Rao³

¹International Institute of Information Technology Bangalore, ²IIT-

Bangalore, ³International Institute of Information Technology-Bangalore

10:00AM

5A.4

138 Scalable Low-Cost Sorting Network with Weighted Bit-Streams

Brady Prince¹, Hassan Najafi², Bingzhe Li¹

¹Oklahoma State University, ²University of Louisiana

SESSION 5B

Friday April 7

Advance Secure Circuits and Hardware Trojan Detection

Chair: **Setareh Rafatirad**, University of California Davis

9:00AM

5B.1

177 Novel, Configurable Approximate Floating-point Multipliers for Error-Resilient Applications

Vishesh Mishra¹, Sparsh Mitta², Rekha Singhal³, Manoj Nambiar³

¹IIT Kanpur, ²IIT Roorkee, ³TCS Research

9:20AM

5B.2

Design Space Exploration of Modular Multipliers for ASIC FHE accelerators

- 161 *Deepraj Soni¹, Mohammed Nabeel Thari Moopan², Homer Gamil³, Oleg Mazonka⁴, Brandon Reagen⁵, Ramesh Karri⁶, Michail Maniatakos⁴*

¹New York University Tandon School of Engineering, ²New York University, ³NYUAD, ⁴New York University Abu Dhabi, ⁵NYU/Facebook, ⁶NYU

9:40AM

5B.3

H-Saber: An FPGA-Optimized Version for Designing Fast and Efficient Post-Quantum

- 13 **Cryptography Hardware Accelerators**

Andrea Guerrieri¹, Gabriel Da Silva Marques², Francesco Regazzoni³, Andres Upegui²

¹EPFL and HES-SO, ²University of Applied Sciences Western Switzerland, ³University of Amsterdam and Universita della Svizzera Italiana

10:00AM

5B.4

- 126 **A Novel Method Against Hardware Trojans in Approximate Circuits**

Yuqin Dou¹, CHONGYAN GU², Chenghua Wang¹, Weiqiang Liu¹

¹Nanjing University of Aeronautics and Astronautics, ²Queen's University Belfast

10:20AM

5B.5

Using Path Features for Hardware Trojan Detection Based on Machine Learning

- 78 **Techniques**

Chia-Heng Yen¹, Jung-Che Tsai¹, Kai-Chiang Wu²

¹National Yang Ming Chiao Tung University, ²Department of Computer Science, National Chiao Tung University

SESSION 5C

Friday April 7

Efficient Algorithm, Hardware, and Computing Paradigm for Machine Learning

Chair: **Kang Jun Bai**, AFRL

9:00AM

5C.1

- 136 **Locality-sensing Fast Neural Network (LFNN): An Efficient Neural Network Acceleration Framework via Locality Sensing for Real-time Videos Queries**

Xiaotian Ma, Jiaqi Tang, Yu Bai

California State University, Fullerton

9:20AM

5C.2

- 113 **Image Quantization Tradeoffs in a YOLO-based FPGA Accelerator Framework**

Richard Yarnell, Mousam Hossain, Ronald DeMara

University of Central Florida

9:40AM

5C.3

- 111 **Automatic Subnetwork Search Through Dynamic Differentiable Neuron Pruning**

Zigeng Wang¹, Bingbing Li¹, Xia Xiao¹, Tianyun Zhang², Mikhail Bragin¹, Bing Yan³, Caiwen Ding¹, Sanguthevar Rajasekaran¹

¹University of Connecticut, ²Cleveland State University, ³Rochester Institute of Technology

10:00AM

5C.4

- 84 **A Novel Stochastic LSTM Model Inspired by Quantum Machine Learning**

Joseph Lindsay and Ramtin Zand

University of South Carolina

SESSION 6A

Friday April 7

Design of Emerging Circuits & Systems

Chair: **Rasit Topaloglu**, IBM

Co-Chair: **Ujwal Radhkrishna**, Texas Instruments Inc.

10:45AM

6A.1

16 **An Area Efficient Superconducting Unary CNN Accelerator**

Patricia Gonzalez-Guerrero, George Michelogiannakis, Kylie Huch, Nirmalendu Patra, Thom Popovici

LBL

11:05AM

6A.2

91 **A Novel Scalable Array Design for III-V Compound Semiconductor-based Non-volatile Memory (UltraRAM) with Separate Read-Write Paths**

Shamiul Alam¹, Kazi Asifuzzaman², Ahmedullah Aziz³

¹University of Tennessee Knoxville, ²Oak Ridge National Laboratory, ³University of Tennessee, Knoxville

11:25AM

6A.3

172 **ZOCHEN: Compression using Zero chain elimination and encoding to improve endurance of Non-volatile Memories**

Nishant Bharti¹, Arijit Nath², Swati Upadhyay¹, Hemangee Kapoor³

¹IIT Guwahati, ²IIT Guwahati, India, ³Indian Institute of Technology Guwahati

11:45AM

6A.4

28 **A Polymorphic Electro-Optic Logic Gate for High-Speed Reconfigurable Computing Circuits**

Venkata Sai Praneeth Karempudi, Sairam Sri Vatsavai, Ishan Thakkar, Todd Hastings
University of Kentucky

SESSION 6B

Friday April 7

Novel AI Computing

Chair: **Hongyu An**, Michgan Tech

Co-Chair: **Haowen Fang**, synopsys

10:45AM

6B.1

87 **Spiking Domain Feature Extraction with Temporal Dynamic Learning**

Honghao Zheng and Yang (Cindy) Yi

Virginia Tech

11:05AM

6B.2

37 **Moving Towards Game-Changing Technology: Fabrication and Application of HfO2 RRAM for In-Memory Computing**

Kang Jun Bai¹, Daniel Titcombe², Jack Lombardi¹, Clare Thiem¹, Nathaniel Cady²

¹Air Force Research Laboratory, ²SUNY Polytechnic Institute

11:25AM

6B.3

Cache Register Sharing Structure for Channel-level Near-memory Processing in NAND Flash Memory

133 *HyunWoo Kim¹, Seungwon Baek¹, Minyoung Jung², Jaehong Song¹, Hyodong Kim¹, Junhyeon Kim¹, Seongju Kim¹, Taigon Song¹, Jongbeom Kim¹, Hyundong Lee³, Yunjeong Go³*

¹Kyungpook National University (KNU), ²Kyungpook National University (KNU), ³Kyungpook National University

11:45AM

6B.4

73 **Online Training from Streaming Data with Concept Drift on FPGAs**

Esther Roorda and Steve Wilton

University of British Columbia

SESSION 6C

Friday April 7

Security for Resource-Limited Devices

Chair: **Ava Hedayatipour**, California State University, Long Beach

10:45AM

6C.1

Attacks on Continuous Chaos Communication and Remedies for Resource Limited Devices

179

Rahul Vishwakarma¹, Ravi Monani², Amin Rezaei², Hossein Sayadi², Mehrdad Aliasgari², Ava Hedayatipour³

¹California State University Long Beach, ²California State University, Long Beach, ³CSULB

11:05AM

6C.2

Split-Slope Chaotic Map Providing High Entropy Across Wide Range

178

Partha Sarathi Paul¹, Maisha Sadia¹, Anurag Dhungel¹, Parker Hardy¹, Md Sakib Hasan²

¹Graduate Student, ²Assistant Professor

11:25AM

6C.3

Reconfigurable low-power Cryptographic processor based on LFSR for Trusted IoT platforms

181

Mohamed El-Hadedy¹, Russell Hua², Kazutomo Yoshii³, Wen-mei Hwu⁴, Martin Margala⁵

¹CalPoly Pomona, ²California State Polytechnic University, Pomona, ³Argonne National Lab, ⁴University of Illinois at Urbana-Champaign, ⁵University of Louisiana at Lafayette

11:45AM

6C.4

180 Automating Hardware Trojan Detection Using Unsupervised Learning: A Case Study of FPGA

Jaya Dofe¹, Shailesh Rajput², Wafi Danesh³

¹California State University, ²California State University Fullerton, ³University of Missouri, Kansas City