Final Program

2023
24th International Symposium on
QUALITY ELECTRONIC DESIGN

April 5-7, 2023
Seven Hills Conference Center
San Francisco State University
San Francisco, CA USA

International Society for Quality Electronic Design
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Greetings,

On behalf of the ISQED conference and technical committees, we are thrilled to welcome you to the 24th anniversary of the International Symposium on Quality Electronic Design, ISQED’23. After several years of virtual events due to the COVID pandemic, we are excited to announce that this year’s event will be held in-person at the Seven Hills Conference Center, located in San Francisco State University, 800 Font Blvd, San Francisco, CA 94132.

For over two decades, ISQED has been the leading voice and pioneer in the field of Quality Electronic Design (QED). With the increasing complexity of semiconductor technology and design, it is more essential than ever before to follow QED and its underlying principles. ISQED’23 aims to lead the community in this direction with an extensive program consisting of keynotes, panels, tutorials, and over 100 peer-reviewed articles.

This year, the conference will be conducted virtually, with the technical sponsorship of the IEEE Electron Devices Society, the IEEE Circuits and Systems Society, IEEE Reliability Society, and in-cooperation with ACM/SigDA. Conference proceedings and papers will be published in IEEE Xplore digital library and indexed by Scopus.

ISQED’23 is organized around critical trends in AI/ML, Autonomous Vehicles, Security, IoT, and Quantum Computing. The conference program includes two keynote speeches, two embedded tutorials, a panel discussion, and numerous peer-reviewed technical papers that focus on these timely topics.

We are delighted to report that the number of quality papers submitted to the conference this year has been overwhelming. The two and a half-day technical program features four parallel sessions and over 100 peer-reviewed papers highlighting the latest trends in electronic circuit and system design and automation, testing, verification, sensors, security, semiconductor technologies, cyber-physical systems, and more.

All technical presentations, plenary sessions, panel discussions, tutorials, and related events will take place in hybrid format on April 5-7, at Pacific Daylight Time (PDT).

We would like to take this opportunity to express our gratitude to the corporate sponsors of ISQED’23: Synopsys and Innovotek for their invaluable financial support of this conference.

General Chair
Sara Tehranipoor
West Virginia University

Program Chair
Cindy Yi
Virginia Tech

Program Co-Chair
Deliang Fan
Arizona State University

Special Sessions Chair
Hossein Sayadi
California State University, Long Beach

Special Sessions Co-Chair
Mimi Xie
The University of Texas at San Antonio

Tutorials Co-Chair
Xiaolin Xun
Northeastern University

Panels Chair
Tosiron Adegbiija
University of Arizona

Publication Chair
Paul Wesling
Hewlett Packard (retired)

ISQED Founder & Chair
Ali A. Iranmanesh
Silicon Valley Polytechnic Institute

Tutorials Chair
Vita Pi-Ho Hu
National Taiwan University

Panels Co-Chair
Fareena Saeed
University of North Carolina
2A.3
DC-Model: A New Method for Assisting the Analog Circuit Optimization
Yuan Wang, Jian Xin, Haixu Liu, Qian Qin, Chenkai Chai, Yukai Lu,
Jinglei Hao, Jianhao Xiao, Zuochang Ye, Yan Wang
Tsinghua University, Beijing, China

6A.1
An Area Efficient Superconducting Unary CNN Accelerator
Patricia Gonzalez-Guerrero, Kylie Huch, Nirmalendu Patra, Thom Popovici,
George Michelogiannakis
Lawrence Berkeley National Laboratory, Berkeley, USA
### ISQED’23 Organizing Committee

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<tr>
<td>General Chair</td>
<td>Sara Tehranipoor</td>
<td>West Virginia University</td>
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<tr>
<td>Program Chair</td>
<td>Cindy Yi</td>
<td>Virginia Tech</td>
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<td>National Taiwan University</td>
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<td>Northeastern University</td>
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<td>Hewlett Packard (retired)</td>
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<td>Panel Chair</td>
<td>Tosiron Adegbi,</td>
<td>University of Arizona</td>
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<tr>
<td>Panel Co-Chair</td>
<td>Fareena Saqib</td>
<td>University of North Carolina</td>
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<td>Special Sessions Co-Chair</td>
<td>Mimi Xie</td>
<td>The University of Texas at San Antonio</td>
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<tr>
<td>Plenary Chair</td>
<td>Ali A. Iranmanesh</td>
<td>Silicon Valley Polytechnic Institute</td>
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<td>Tutorials Co-Chair</td>
<td>Xiaolin Xun</td>
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<td>University of North Carolina</td>
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<tr>
<td>Special Sessions Chair</td>
<td>Hossein Sayadi</td>
<td>California State University, Long Beach</td>
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### GLOBAL REPRESENTATIVES

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<tr>
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<tr>
<td>Europe Chair</td>
<td>George P. Alexiou</td>
<td>University of Patras and RA-CTI, Patras, Greece</td>
</tr>
<tr>
<td>Brazil &amp; South America Chair</td>
<td>Fabiano Passuelo Hessel</td>
<td>Pontificia Universidade Catolica do Rio do Sul, Brazil</td>
</tr>
<tr>
<td>Taiwan Chair</td>
<td>Shih-Hsu Huang</td>
<td>Chung Yuan Christian University</td>
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<tr>
<td>China Chair</td>
<td>Gaofeng Wang</td>
<td>Hangzhou Dianzi University</td>
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<tr>
<td>Japan Chair</td>
<td>Masahiro Fujita</td>
<td>University of Tokyo</td>
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### TECHNICAL PROGRAM COMMITTEES

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Jiliang Zhang - Hunan University

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Lan Wei, University of Waterloo (Co-Chair)
Volkan Kursun, Norwegian University of Science and Technology (Co-Chair)

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Shawana Tabassum - The University of Texas at Tyler
Jinhui Wang - University of South Alabama
Mustafa Berke Yeten - Istanbul Technical University
Masoud Zabihi - Notheastern University
Panel Discussion
Sponsored by Synopsys

Wednesday, April 5, 3:15 PM - 4:45 PM
Track A - Nob Hill Room

Driving the Future: Exploring the Intersection of AI and Autonomous Vehicles

Two rapidly emerging technologies, Artificial Intelligence (AI) and autonomous vehicles (AV), are poised to revolutionize everyday life. Industries worldwide are investing billions of dollars to advance these transformative technologies, which have seen remarkable advancements over the past few decades. However, we have only scratched the surface of their potential impact on society. This panel will feature experts in the fields of AI and AVs who will discuss the current trends in AV, with a focus on leveraging advancements in AI to accelerate the development of AV. The panel will explore topics such as the reality of AI-driven electronic design, short-term and long-term predictions of how AI and AV will interact and their potential impact, security considerations in AI-driven AV design, practical research challenges and gaps, and potential directions for addressing these gaps.

Panelists:
Yankin Tanurhan - Synopsys
Ravikumar Chakaravarthy - AMD
Pratik Prabhanjan Brahma - Cruiz
Daryush Laqab - NVIDIA

Moderator:
Pallab Chatterjee - Roadway Media

Chairs:
Tosiron Adegbija - University of Arizona (Chair)
Fareena Saqib - University of North Carolina (Co-Chair)
GENERAL INFORMATION

Embedded Tutorials

Chair & Moderators:
Vita Pi-Ho Hu - National Taiwan University (Chair)
Xiaolin Xun - Northeastern University (Co-Chair)

Track A - Nob Hill Room
Tutorial 1
Wednesday, April 5, 12:25 PM -1:25 PM
Design Automation for Learning-Enabled Cyber-Physical Systems

Prof. Qi Zhu
Northwestern University

Tutorial 2
Thursday April 6, 1:05 PM -2:05 PM
Introduction to Quantum Computing: from Algorithm to Hardware

Prof. Hiu Yung Wong
San Jose State University

TECHNICAL SESSIONS
There are a total of 20 paper sessions held on Wednesday to Friday. Technical sessions are held in the format of three parallel tracks A, B, C located respectively in Nob Hill Room, Russian Hill Room, and Mt. Davidson room.

ON-SITE REGISTRATION
Tentative time schedule of on-site registration is as follows:

Wednesday, April 5, 8:00 AM - 2:00 PM
Thursday, April 6, 8:00 AM -12:00 PM

Registration desk location will be at the conference center lobby.

Seven Hills Conference Center

ISQED’23 conference will be held in Seven Hills Conference Center, located in San Francisco State University, 800 Font Blvd, San Francisco, CA 94132.

If you are using navigator the best address to use is: 796 state drive, San Francisco, CA 94132. (Note: make sure to use Google Maps app) At the end of State Drive is the Public Parking Lot (“Lot 20”). Parking is $6.25 for less than 2 hours, and $10 for 2+ hours. Pay stations on each floor accept $1, $5 and $10 bills as well as credit/debit cards. Be advised, pay stations do not provide change. Please have exact amount. From the garage, Seven Hills’ entrance can be accessed from State Drive by walking Southwest towards the A.S. Children’s Center and taking the staircase beside it up one flight. Wheelchair access: go past the staircase and take a left onto the path. Follow to the entrance to the Seven Hills Conference Center.
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<tr>
<th>Time</th>
<th>Session A (Nob Hill Room)</th>
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<td>10:00-10:20am</td>
<td>Keynote: The Weakest Link: Microelectronics Security Against Physical Attacks</td>
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<tr>
<td>10:20-10:40am</td>
<td>Introduction, Committee Recognitions, Best Paper Awards</td>
</tr>
<tr>
<td>10:45-11:05am</td>
<td>Tutorial 1</td>
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<tr>
<td>11:10-11:30am</td>
<td>Design Automation for Learning-Enabled Cyber-Physical Systems (Prof. Qilin Zhou - Northwestern University)</td>
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<tr>
<td>11:45-12:05pm</td>
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<td>12:20-12:40pm</td>
<td>Session 1A (Nob Hill Room)</td>
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<tr>
<td>12:45-1:05pm</td>
<td>Session 1B (Russian Hill Room)</td>
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<td>1:10-1:30pm</td>
<td>Session 2A (Nob Hill Room)</td>
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<td>1:35-1:55pm</td>
<td>Session 2B (Russian Hill Room)</td>
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<td>2:10-2:30pm</td>
<td>Panel Discussion - Exploring the Intersection of AI and Autonomous Vehicles</td>
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<tr>
<td>2:35-2:55pm</td>
<td>Break</td>
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<tr>
<td>3:10-3:30pm</td>
<td>Session 3A (Nob Hill Room)</td>
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<td>3:35-3:55pm</td>
<td>Session 3B (Russian Hill Room)</td>
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<td>4:10-4:30pm</td>
<td>Break</td>
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<tr>
<td>4:45-5:05pm</td>
<td>Session 4A (Nob Hill Room)</td>
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<td>5:10-5:30pm</td>
<td>Session 4B (Russian Hill Room)</td>
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<td>5:45-5:55pm</td>
<td>Break</td>
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<tr>
<td>6:00-6:20pm</td>
<td>Session 5A (Nob Hill Room)</td>
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<tr>
<td>6:25-6:45pm</td>
<td>Session 5B (Russian Hill Room)</td>
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Please note all shown times are Pacific Daylight Time (PDT).
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<thead>
<tr>
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<th>Session</th>
<th>Location</th>
<th>Presenter</th>
<th>Title</th>
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</thead>
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<tr>
<td>9:00am-9:30am</td>
<td>Welcome</td>
<td>Nob Hill Room</td>
<td>Dr. Ranjith Venkatesan</td>
<td>Pushing the Energy-efficiency of Deep Learning Accelerators with Hardware-Software Co-design</td>
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<tr>
<td>9:30am-9:45am</td>
<td>Break</td>
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<tr>
<td>9:45am-11:00am</td>
<td>Session PW1 (Nob Hill Room)</td>
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<td>Break</td>
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<tr>
<td>11:15am-12:00pm</td>
<td>Session PW2 (Russian Hill Room)</td>
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<td>Session PW3 (Mt. Davidson Room)</td>
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<td>Lunch Break</td>
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<td>Session 4A (Nob Hill Room)</td>
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<td>2:30pm-3:00pm</td>
<td>Break</td>
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<tr>
<td>3:00pm-4:00pm</td>
<td>Session 4B (Russian Hill Room)</td>
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<tr>
<td>4:00pm-4:15pm</td>
<td>Break</td>
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<td>4:15pm-5:15pm</td>
<td>Lunch Break</td>
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<td>5:15pm-6:00pm</td>
<td>Session 4C (Mt. Davidson Room)</td>
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<td>6:15pm-6:30pm</td>
<td>Session 4D (Mt. Davidson Room)</td>
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<td>6:30pm-7:00pm</td>
<td>Break</td>
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**Thursday, April 6, 2023**

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The Weakest Link: 
Microelectronics Security Against Physical Attacks

For the past decade and a half, the hardware security community has expended significant time on threats related to semiconductor globalization. With the passage of the CHIPS Act in the US and similar legislation around the world, untrusted foundries should no longer be considered the weakest link. It is time to refocus efforts towards physical attacks against microelectronics. Physical attacks exist across a wide spectrum – from low-cost/low-reward non-invasive attacks to high-cost/high-reward invasive attacks – and have successfully extracted on-chip assets and broken roots-of-trust in recent years. Some non-invasive attacks have even found success remotely. Further, the threat of semi-invasive attacks, such as optical probing, is growing. Semi-invasive attacks are low in cost like non-invasive attacks but nearly as powerful as invasive attacks. This keynote will review this dangerous landscape and discuss emerging approaches that bolster physical security. It is said that “Time is what determines security. With enough time nothing is unhackable.” Hence, more attention will be paid to techniques that quantifiable increase the time and complexity of physical attacks.

About Domenic Forte
Domenic Forte is an Associate Professor and the Steven A. Yatauro Faculty Fellow with the Electrical and Computer Engineering Department at University of Florida. He is also Associate Director for the Florida Institute for National Security (FINS). His research covers the domain of hardware security from transistors to printed circuit boards where he has over 200 publications. Dr. Forte is a senior member of the IEEE, a member of the ACM, and serves or has served on the technical program committees of leading events such as USENIX Security, NDSS, HOST, ASHES, DAC, ICCAD, ITC, ISTFA, and BTAS. Dr. Forte is a recipient of the Presidential Early Career Award for Scientists and Engineers (PECASE), the NSF CAREER Award, and the ARO Young Investigator Award. His research has also been recognized with best paper awards and nominations from IJCB, ISTFA, HOST, DAC, and AHS. For teaching and advising, he has received the Herbert Wertheim College of Engineering Doctoral Dissertation Advisor/Mentoring Award, the Excellence in Teaching Award from UF’s ECE Graduate Student Organization, and the George Corcoran Outstanding Teaching Award from University of Maryland.
Deep neural networks (DNNs) have emerged as a key approach to solving complex problems across many application spaces, including image recognition, natural language processing, robotics, health care, and autonomous driving. Designing custom hardware accelerators for deep neural networks is highly promising, as they offer significant performance and power advantages compared to general-purpose processors. This talk presents MAGNet, a hardware-software co-design framework that explores different data formats, quantization techniques, memory hierarchies, and dataflows. This talk describes a new data format VS-Quant for achieving low-precision computation and novel multi-level dataflows to improve energy efficiency.

About Rangharajan Venkatesan
Rangharajan Venkatesan is a Senior Research Scientist in the ASIC & VLSI Research group in NVIDIA. He received the B.Tech. degree in Electronics and Communication Engineering from the Indian Institute of Technology, Roorkee in 2009 and the Ph.D. degree in Electrical and Computer Engineering from Purdue University in August 2014. His research interests are in the areas of low-power VLSI design and computer architecture with a particular focus in deep learning accelerators. He has received Best Paper Awards for his work on deep learning accelerators from IEEE/ACM Symposium on Microarchitecture (MICRO) and Journal of Solid-State Circuits (JSSC). His work on spintronic memory design was recognized with the Best Paper Award at the International Symposium on Low Power Electronics and Design (ISLPED), and Best paper nomination at the Design, Automation and Test in Europe (DATE). His paper titled, “MACACO: Modeling and Analysis of Circuits for Approximate Computing”, received the IEEE/ACM International Conference on Computer-Aided Design (ICCAD) Ten Year Retrospective Most Influential Paper Award in 2021. He has served as a member of the technical program committees of several leading IEEE/ACM conferences including ISSCC, DAC, MICRO, and ISLPED.
Panel Discussion

Wednesday April 5
3:15 PM–4:45 PM
Room: Nob Hill

ISQED’23 panel discussion is sponsored by Synopsys

Driving the Future: Exploring the Intersection of AI and Autonomous Vehicles

Summary:
Two rapidly emerging technologies, Artificial Intelligence (AI) and autonomous vehicles (AV), are poised to revolutionize everyday life. Industries worldwide are investing billions of dollars to advance these transformative technologies, which have seen remarkable advancements over the past few decades. However, we have only scratched the surface of their potential impact on society. This panel will feature experts in the fields of AI and AV who will discuss the current trends in AV, with a focus on leveraging advancements in AI to accelerate the development of AV. The panel will explore topics such as the reality of AI-driven electronic design, short-term and long-term predictions of how AI and AV will interact and their potential impact, security considerations in AI-driven AV design, practical research challenges and gaps, and potential directions for addressing these gaps.

Panelists:
Yankin Tanurhan - Synopsys
Ravikumar Chakaravarthy - AMD
Daryush Laqab - NVIDIA
Pratik Prabhanjan Brahma - Cruise

Moderator:
Pallab Chatterjee - Roadway Media

Panel Committee:
Tosiron Adegbija - University of Arizona (Chair)
Fareena Saqib - University of North Carolina, Charlotte (Co-Chair)
Design Automation for Learning-Enabled Cyber-Physical Systems

Summary:
Future learning-enabled cyber-physical systems (LE-CPSs), such as self-driving cars and robotic systems, will employ complex machine learning-based sensing, computation and communication components for their perception, prediction, planning, control, and coordination. However, ensuring their safety, robustness and security faces tremendous challenges, given the highly dynamic and uncertain environment they operate within, the fast increase of their functional and architectural complexity, the difficulty in analyzing deep neural network-based components, and the often-stringent resource and timing constraints. This calls for new design automation methodologies and tools that support rigorous, accurate and efficient modeling, synthesis, verification, and adaptation of LE-CPSs. In this tutorial, using connected and autonomous vehicles (CAVs) as an example, I will discuss these challenges and present some of our recent work to address them in a holistic manner, including 1) end-to-end verification, design and adaptation methods for ensuring robust and safe application of neural networks in perception and decision making; and 2) cross-layer methods based on weakly-hard paradigm for mitigating execution disturbances (e.g., timing violations, soft errors, malicious attacks).

About Qi Zhu
Qi Zhu is an Associate Professor at the ECE Department in Northwestern University. He received a Ph.D. in EECS from University of California, Berkeley in 2008, and a B.E. in CS from Tsinghua University in 2003. His research interests include design automation for cyber-physical systems (CPS) and Internet of Things, safe and secure machine learning for CPS and IoT, cyber-physical security, and system-on-chip design, with applications in domains such as connected and autonomous vehicles, energy-efficient smart buildings, and robotic systems. He is a recipient of the NSF CAREER award, the IEEE TCCPS Early-Career Award, and the Humboldt Research Fellowship for Experienced Researchers. He received best paper awards at DAC 2006, DAC 2007, ICCPS 2013, ACM TODAES 2016, and DATE 2022. He is the Conference Chair of IEEE TCCPS, and VP of Young Professionals at IEEE CEDA. He is an Associate Editor for IEEE TCAD, ACM TCPS, and IET Cyber-Physical Systems: Theory & Applications, and has served as a Guest Editor for the Proceedings of the IEEE, ACM TCPS, IEEE T-ASE, Elsevier JSA, and Elsevier Integration, the VLSI journal.
**Embedded Tutorial 2**

**Thursday April 6**  
1:05 PM - 2:05 PM  
Nob Hill Room

**Introduction to Quantum Computing: from Algorithm to Hardware**

![Prof. Hiu Yung Wong](image)

**Prof. Hiu Yung Wong**  
*San Jose State University*

**Summary:**  
Quantum computing is expected to change the world by providing exponential speed-up in solving some very difficult problems. In this tutorial, we will first discuss the fundamental principles of quantum computing algorithms. We will run one of the basic quantum algorithms, the Deutsch algorithm, on IBM’s quantum computer to further appreciate the origin of speed-up and the limitations in quantum computers. Error correction, which is essential to realize a fault-tolerant quantum computer, will be briefly covered. Finally, using the superconductor-based quantum computer as an example, we will study how to implement the essential operations in quantum computers, namely, qubit initialization, readout, and manipulations. It will be appreciated that powerful classical computers, which are used to control the qubits, are essential to the successful implementation of quantum computers.

**About Hiu Yung Wong**  
Hiu Yung Wong is an Associate Professor and Silicon Valley AMDT Endowed Chair in Electrical Engineering, at San Jose State University. He received his Ph.D. degree in Electrical Engineering and Computer Science from the University of California, Berkeley in 2006. From 2006 to 2009, he worked as a Technology Integration Engineer at Spansion. From 2009 to 2018, he was a TCAD Senior Staff Application Engineer at Synopsys. He received the Curtis W. McGraw Research Award from ASEE Engineering Research Council in 2022, the NSF CAREER award and the Newnan Brothers Award for Faculty Excellence in 2021, and Synopsys Excellence Award in 2010. He is the author of the book, “Introduction to Quantum Computing: From a Layperson to a Programmer in 30 Steps”. He is one of the founding faculties of the Master of Science in Quantum Technology at San Jose State University. His research interests include the application of machine learning in simulation and manufacturing, cryogenic electronics, quantum computing, and wide bandgap device simulations. His works have produced 1 book, 1 book chapter, more than 100 papers, and 10 patents.
SESSION 1A

Wednesday April 5

Next Generation Computing Systems

Chair: Arnab Raha, Intel
Co-Chair: Kang Jun Bai, AFRL

10:20AM
1A.1
A SPICE-based Framework to Emulate Quantum Circuits with classical LC Resonators
Md Mazharul Islam¹, Shafayat Hossain², Ahmedullah Aziz³
¹The University of Tennessee, ²Princeton University, ³University of Tennessee, Knoxville

10:40AM
1A.2
Metal Inter-layer Via Keep-out-zone in M3D IC: A Critical Process-aware Design Consideration
Madhava Sarma Vemuri and Umamaheswara Tida
North Dakota State University

11:00AM
1A.3
AGNI: In-Situ, Iso-Latency Stochastic-to-Binary Number Conversion for In-DRAM Deep Learning
Supreeth Mysore Shivanandamurthy, Sairam Sri Vatsavai, Ishan Thakkar, sayedahmad salehi
University of Kentucky

11:20AM
1A.4
Design and Evaluation of multipliers for hardware accelerated on-chip EdDSA
Harshita Gupta¹, Mayank Kabra², Nitin Patwari³, Prashanth H C⁴, Madhav Rao⁵
¹Thapar institute of information technology, Patiala, ²Student, ³Student, IIITB, ⁴IIIT-Bangalore, ⁵International Institute of Information Technology-Bangalore
SESSION 1B

Wednesday April 5

Design for Testability and Verification

Chair: Chidhambaranathan R, Synopsys

10:20AM
1B.1 Self-Checking Performance Verification Methodology for Complex SoCs
Prokash Ghosh¹, Aditya Chopra¹, Dwaraka Pai², Baljinder Sood²
¹NXP Semiconductor Inc, USA, ²NXP Semiconductors Inc, USA

10:40AM
1B.2 Polynomial Formal Verification of a Processor: A RISC-V Case Study
Lennart Weingarten¹, Alireza Mahzoon¹, Mehran Goli¹, Rolf Drechsler²
¹University of Bremen, ²University of Bremen/DFKI

11:00AM
1B.3 Application of Machine Learning for Quality Risk Factor Analysis of Electronic Assemblies
Brendan Reidy¹, David Duggan¹, Bernard Glasauer², Peng Su², Ramtin Zand¹
¹University of South Carolina, ²Component Engineering, Juniper Networks

11:20AM
1B.4 Quality-driven Design Methodology for PUFs in FPGAs for Secure IoT
Xiangyun Wang¹, Yicheng Song¹, Katyayani Prakash¹, Zeljko Zilic¹, Tomas Langsetmo²
¹McGill University, ²KNOX Industries Inc.
SESSION 1C

Wednesday April 5

AI Applications in Computing System Design

Chair: Hossein Sayadi, California State University, Long Beach

10:20AM
1C.1
HD2FPGA: Automated Framework for Accelerating Hyperdimensional Computing on FPGAs
Tianqi Zhang$, Sahand Salamat$, Behnam Khaleghi$, Justin Morris$, Baris Aksanli$, Tajana Rosing$
$^1$UCSD, $^2$University of California, San Diego, $^3$CSUSM, $^4$San Diego State University

10:40AM
1C.2
XOR-CiM: An Efficient Computing-in-SOT-MRAM Design for Binary Neural Network Acceleration
Mehrdad Morsali$, Ranyang Zhou$, Sepehr Tabrizchi$, Arman Roohi$, Shaahin Angizi$
$^1$New jersey Institute of Technology, $^2$University of Nebraska–Lincoln, $^3$University of Nebraska - Lincoln

11:00AM
1C.3
Security and Reliability Challenges in Machine Learning for EDA: Latest Advances
Zhiyao Xie, Tao Zhang, Yifeng Peng
Hong Kong University of Science and Technology

11:20AM
1C.4
Image-Based Zero-Day Malware Detection in IoMT Devices: A Hybrid AI-Enabled Method
Zhangying He and Hossein Sayadi
California State University, Long Beach
SESSION 2A

Wednesday April 5

Advances in Circuit and Physical Design

Chair: Rui Zhang, Cadence Inc.
Co-Chair: Sheikh Ariful Islam, University of Texas Rio Grande Valley

1:30PM
2A.1
101 Routability-aware Placement Guidance Generation for Mixed-size Designs
Chieh-Yu Cheng and Ting-Chi Wang
National Tsing Hua University

1:50PM
2A.2
103 MC-MCF: A Multi-Capacity Model for Ordered Escape Routing
Zhenyi Gao, Sheqin Dong, Zhicong Tang, Wenjian Yu
Tsinghua University

2:10PM
2A.3
137 DC-Model: A New Method for Assisting the Analog Circuit Optimization
Yuan Wang, Jian Xin, Haixu Liu, Qian Qin, Chenkai Chai, Yukai Lu, Jinglei Hao, Jianhao Xiao, Zuochang Ye, Yan Wang
Tsinghua University

2:30PM
2A.4
146 Accounting for Floorplan Irregularity and Configuration Dependence in FPGA Routing Delay Models
Gabriel Barajas\textsuperscript{1}, Jonathan Greene\textsuperscript{2}, Fei Li\textsuperscript{1}, James Tandon\textsuperscript{3}
\textsuperscript{1}Microchip, \textsuperscript{2}Cambios Computing LLC, \textsuperscript{3}California State University East Bay
2:50PM
2A.5
171  An Effective Cost-Skew Tradeoff Heuristic for VLSI Global Routing
Andrew Kahng\textsuperscript{1}, Shreyas Thumathy\textsuperscript{2}, Mingyu Woo\textsuperscript{3}
\textsuperscript{1}UCSD CSE and ECE Departments, \textsuperscript{2}Canyon Crest Academy, \textsuperscript{3}UCSD ECE Department

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SESSION 2B

Wednesday April 5

Recent Advances in Secure Hardware Design

Chair: Soheil Salehi, University of Arizona

1:30PM
2B.1
Automated Supervised Topic Modeling Framework for Hardware Weaknesses
Rakibul Hassan\textsuperscript{1}, Charan Bandi\textsuperscript{1}, Meng-Tien Tsai\textsuperscript{2}, Shahriar Golchin\textsuperscript{3}, Sai Manoj Pudukotai Dinakarrao\textsuperscript{1}, Setareh Rafatirad\textsuperscript{2}, Soheil Salehi\textsuperscript{4}
\textsuperscript{1}George Mason University, \textsuperscript{2}University of California Davis, \textsuperscript{3}University of Arizona, \textsuperscript{4}Department of Electrical and Computer Engineering, University of Arizona

1:50PM
2B.2
Polymorphic Sensor to Detect Laser Logic State Imaging Attack
Sourav Roy\textsuperscript{1}, Shahin Tajik\textsuperscript{2}, Domenic Forte\textsuperscript{1}
\textsuperscript{1}University of Florida, \textsuperscript{2}Worcester Polytechnic Institute

2:10PM
2B.3
Low Overhead System-Level Obfuscation through Hardware Resource Sharing
Daniel Xing\textsuperscript{1}, Michael Zuzak\textsuperscript{2}, Ankur Srivastava\textsuperscript{1}
\textsuperscript{1}University of Maryland, \textsuperscript{2}Rochester Institute of Technology
SESSION 2C

Wednesday April 5

Efficiency and Reliability of Memory

Chair: Hongyu An, Michigan Technological University

1:30PM
2C.1
eDRAM-OESP: A novel performance efficient in-embedded-DRAM-compute design for on-edge signal processing application
Mayank Kabra¹, Prashanth H C², Kedar Deshpande¹, Madhav Rao³
¹Student, ²IIIT-Bangalore, ³International Institute of Information Technology-Bangalore

1:50PM
2C.2
CMDS: Cross-layer Dataflow Optimization for DNN Accelerators Exploiting Multi-bank Memories
Man Shi¹, Steven Colleman¹, Charlotte VanDeMieroop¹, Antony Joseph², Maurice Meijer², Wim Dehaene¹, Marian Verhelst¹
¹KU Leuven, ²NXP Semiconductor
HIE-DRAM: High-Performance Efficient In-DRAM Computing Architecture for SIMD
Mayank Kabra¹, Prashanth H C², Kedar Deshpande¹, Madhav Rao³
¹Student, ²IIIT-Bangalore, ³International Institute of Information Technology-Bangalore

AGRAS: Aging and memory request rate aware scheduler for PCM memories
Aswathy NS¹ and Hemangee Kapoor²
¹IIT Guwahati, ²Indian Institute of Technology Guwahati

SESSION PW1
Thursday April 6

PW1

Chair: Hossein Sayadi, California State University, Long Beach

9:40AM
PW1.1
Accurate Estimation of Circuit Delay Variance with Limited Monte Carlo Simulations Using Bayesian Inference
Chithira R.
National Institute of Technology Calicut

9:45AM
PW1.2
DSEAdd: FPGA based Design Space Exploration for Approximate Adders with Variable Bit-precision
Archie Mishra and Nanditha Rao
IIIT Bangalore
9:50AM
PW1.3
Emerging Interconnect Exploration for SRAM Application Using Nonconventional H-Tree and Center-Pin Access
Zhenlin Pei¹, Mahta Mayahinia², Hsiao-Hsuan Liu³, Mehdi Tahoori², Shairfe Salahuddin⁴, Francky Catthoor⁴, Zsolt Tokei⁴, Chenyun Pan⁵
¹The University of Texas at Arlington, ²Karlsruhe institute of technology (KIT), ³Katholieke Universiteit Leuven (KU Leuven), ⁴IMEC, ⁵University of Texas at Arlington

9:55AM
PW1.4
A Low-overhead PUF-based Secure Scan Design
Wei Zhou¹, Aijiao Cui¹, Cassi Chen², Gang Qu³
¹Harbin Institute of Technology (Shenzhen), ²University of California, Berkeley, ³University of Maryland

10:00AM
PW1.5
Deep Image Segmentation for Defect Detection in Photo-lithography Fabrication
Omari Paul¹, Sakib Abrar¹, Richard Mu¹, Riadul Islam², Manar Samad¹
¹Tennessee State University, ²University of Maryland at Baltimore County

10:05AM
PW1.6
Performance Analysis of Cylindrical Through Silicon Via with Interfacial Crack
Vandana Kumari, Maya Chandrakar, Manoj Majumder
IIIT Naya Raipur

10:10AM
PW1.7
A Flexible Cluster Tool Simulation Framework with Wafer Batch Dispatching Time Recommendation
Hsin-Ping Yen¹, Shiu-Hsuan Huang¹, Yan-Hsiu Liu², Kuang-Hsien Tseng², Ji-Fu Kung², Yi-Ting Li², Yung-Chih Chen³, Chun-Yao Wang⁴
¹National Tsing Hua University, ²United Microelectronics Corporation, ³National Taiwan University of Science and Technology, ⁴Dept. CS, National Tsing Hua University
10:15AM
PW1.8
Hardware Performance Counter Enhanced Watchdog for Embedded Software Security
Karl Ott\textsuperscript{1} and Rabi N. Mahapatra\textsuperscript{2}
\textsuperscript{1}Texas A&M University, \textsuperscript{2}Professor

10:20AM
PW1.9
Power Savings in USB Hubs Through a Proactive Scheduling Strategy
Bikrant Das Sharma\textsuperscript{1}, Abdul Ismail\textsuperscript{2}, Chris Meyers\textsuperscript{3}
\textsuperscript{1}Rice University, \textsuperscript{2}Intel Corporation, USB Implementers Forum, \textsuperscript{3}Fresco Logic

10:25AM
PW1.10
DK Lock: Dual Key Logic Locking Against Oracle-Guided Attacks
Jordan Maynard\textsuperscript{1} and Amin Rezaei\textsuperscript{2}
\textsuperscript{1}California State University Long Beach, \textsuperscript{2}California State University, Long Beach
SESSION PW2

Thursday April 6

PW2

Chair: Kang Jun Bai, AFRL

9:40AM
PW2.1
Reproducing Fear Conditioning of Rats with Unmanned Ground Vehicles and Neuromorphic Systems
Noah Zins and Hongyu An
Michigan Technological University

9:45AM
PW2.2
High-Throughput Hardware Implementation for Haraka in SPHINCS+
Yueqin Dai, Yifeng Song, Jing Tian, Zhongfeng Wang
Nanjing University

9:50AM
PW2.3
Dhanasekar V1, Vinodhini Gunasekaran1, Anusha Challa1, Bama Srinivasan1, Dhurga Devi J1, Selvi Ravindran1, Ranjani Parthasarathi1, Ramakrishna P V1, Gopika Geetha Kumar2, Venkateswaran Padmanabhan3, Guha Lakshmanan3, Lakshmanan Balasubramanian3
1College of Engineering Guindy, Anna University, 2Carnegie Mellon University, Pennsylvania, 3Texas Instruments (India) Pvt. Ltd.
9:55AM
PW2.4
Focusing on the Key Suspicious Trojan Nets with a Collaborative Approach
Shih-Lung Pao¹, Chuan-Pin Huang¹, Yen-Chi Peng¹, Ing-Jer Huang²
¹Department of Computer Science and Engineering, National Sun Yat-Sen University, ²Department of Computer Science and Engineering, Digital Content and Multimedia Technology Research Center, National Sun Yat-Sen University

10:00AM
PW2.5
CMP-SiL: Confidential Multi Party Software-in-the-Loop Simulation Framework
Shalabh Jain¹, Pradeep Pappachan¹, Jorge Guajardo², Sven Trieﬂinger³, Indrasen Raghupatrini³, Thomas Huber³
¹Robert Bosch LLC, ²Bosch Research and Technology Center, Robert Bosch LLC, ³Robert Bosch GmbH

10:05AM
PW2.6
A2OP: an A* Algorithm OPtimizer with the Heuristic Function for PCB Automatic Routing
Quanbao Guo and Keni Qiu
Capital Normal University

10:15AM
PW2.7
Decomposable Architecture and Fault Mitigation Methodology for Deep Learning Accelerators
Ning-Chi Huang¹, Min-Syue Yang¹, Ya-Chu Chang¹, Kai-Chiang Wu²
¹Department of Computer Science, National Yang Ming Chiao Tung University, ²Department of Computer Science, National Chiao Tung University

10:20AM
PW2.8
NetViz: A Tool for Netlist Security Visualization
James Geist¹, Travis Meade¹, Shaojie Zhang¹, Yier Jin²
¹University of Central Florida, ²University of Florida
10:25AM
PW2.9
A True Random Number Generator for Probabilistic Computing using Stochastic Magnetic Actuated Random Transducer Devices
Ankit Shukla¹, Laura Heller¹, Md Golam Morshed², Laura Rehm³, Avik Ghosh², Andrew Kent³, Shaloo Rakheja¹
¹University of Illinois at Urbana-Champaign, ²University of Virginia, ³New York University

10:30AM
PW2.10
Attributed Graph Transformation for Generating Synthetic Benchmarks for Hardware Security
Juneeth kumar Meka and Ranga Vemuri
University of Cincinnati
SESSION PW3

Thursday April 6

PW3

Chair: Vidya Chhabria, Arizona State University

9:40AM
PW3.1
Secure Control Loop Execution of Cyber-Physical Devices Using Predictive State Space Checks
Kwondo Ma1, Chandramouli Amarnath1, Abhijit Chatterjee1, Jacob Abraham2
1Georgia Institute of Technology, 2University of Texas at Austin

9:45AM
PW3.2
Cryogenic In-memory Binary Multiplier Using Quantum Anomalous Hall Effect Memories
Arun Govindankutty1, Shamiul Alam2, Sanjay Das1, Ahmedullah Aziz2, Sumitha George1
1North Dakota State University, 2The University of Tennessee, Knoxville

9:50AM
PW3.3
SQRTLIB : Library of Hardware Square Root Designs
Prashanth H C1, Sriniketh S S2, Shrikrishna Hebbar2, Chinmaye R2, Madhav Rao3
1IIT-Bangalore, 2RVCE, 3International Institute of Information Technology-Bangalore

9:55AM
PW3.4
Binary Synaptic Array for Inference and Training with Built-in RRAM Electroforming Circuit
Ashvinikumar Dongre and Gaurav Trivedi
Indian Institute of Technology Guwahati India
10:00AM
PW3.5
Neural Network Partitioning for Fast Distributed Inference
Robert Viramontes and Azadeh Davoodi
University of Wisconsin - Madison

10:05AM
PW3.6
DAGGER: Exploiting Language Semantics for Program Security in Embedded Systems
Garett Cunningham, Harsha Chenji, Gordon Stewart, David Juedes, Avinash Karanth
Ohio University

10:10AM
PW3.7
Exploiting Programmable Dipole Interaction in Straintronic Nanomagnet Chains for Ising Problems
Nastaran Darabi\(^1\), Maeesha Binte Hashem\(^1\), Supriyo Bandyopadhyay\(^2\), Amit Trivedi\(^1\)
\(^1\)University of Illinois at Chicago, \(^2\)Virginia Commonwealth University

10:15AM
PW3.8
A Bit-Parallel Deterministic Stochastic Multiplier
Sairam Sri Vatsavai and Ishan Thakkar
University of Kentucky

10:20AM
PW3.9
ACPC: Covert Channel Attack on Last Level Cache using Dynamic Cache Partitioning
Jaspinder Kaur\(^1\) and Shirshendu Das\(^2\)
\(^1\)Indian Institute of Technology Ropar, \(^2\)Indian Institute of Technology Hyderabad

10:25AM
PW3.10
Intrinsic Parameter Fluctuation and Process Variation Effect of Vertically Stacked Silicon Nanosheet Complementary Field-Effect Transistors
Sekhar Kola, Yiming Li, Min-Hui Chuang
National Yang Ming Chiao Tung University
10:30AM

PW3.11

SpotOn: A Gradient-based Targeted Data Poisoning Attack on Deep Neural Networks

Yash Khare¹, Kumud Lakara², Sparsh Mittal³, Arvind Kaushik⁴, Rekha Singhal⁵

¹Amrita Vishwa Vidyapeetham, ²Manipal Institute of Technology, ³IIT Roorkee, ⁴NXP Semiconductors, ⁵TCS Research
SESSION 3A

Thursday April 6

ML based CAD for Optimization

Chair: Murthy Palla, Synopsys Inc.
Co-Chair: Rui Zhang, Cadence Inc.

10:45AM
3A.1
PreAxC: Error Distribution Prediction for Approximate Computing Quality Control using Graph Neural Networks
Lakshmi Sathidevi1, Abhinav Sharma2, Nan Wu3, Xun Jiao4, Cong "Callie" Hao1
1Georgia Institute of Technology, 2Indian Institute of Information Technology, Guwahati, 3UC Santa Barbara, 4Villanova University

11:05AM
3A.2
DeepAxe: A Framework for Exploration of Approximation and Reliability Trade-offs in DNN Accelerators
Mahdi Taheri1, Mohamad Riazati2, Mohammad Hasan Ahmadilivani3, Maksim Jenihhin3, Masoud Daneshtalab2, Jaan Raik4, Mikael Sjödin2, Björn Lisper2
1PhD researcher at Tallinn university of Technology, 2Mälardalen University, Västerås, 3Tallinn University of Technology, Tallinn, Estonia, 4Tallinn University of Technology, Tallinn

11:25AM
3A.3
TOTAL: Topology Optimization of Operational Amplifier via Reinforcement Learning
Zihao Chen, Songlei Meng, Fan Yang, Li Shang, Xuan Zeng
Fudan University
11:45AM
3A.4
154 Design of Hardware Accelerators to Compute Parametric Capacitance Tables
Sandeep Koranne
Mentor Graphics Corporation

12:05PM
3A.5
175 Dilated Involutional Pyramid Network (DInPNet): A Novel Model for Printed Circuit Board (PCB) Components Classification
Ananya Mantravadi¹, Dhruv Makwana², Sai Chandra Teja R², Sparsh Mittal³, Rekha Singhal⁴
¹IIIT Raichur, ²Independent Researcher, ³IIT Roorkee, ⁴TCS Research
SESSION 3B

Thursday April 6

AI Accelerator Hardware Design

Chair: Kang Jun Bai, AFRL
Co-Chair: Ji Li, MicroSoft

10:45AM
3B.1
An Optical XNOR-Bitcount Based Accelerator for Efficient Inference of Binary Neural Networks
Sairam Sri Vatsavai, Venkata Sai Praneeth Karempudi, Ishan Thakkar
University of Kentucky

11:05AM
3B.2
Heterogeneous Multi-Functional Look-Up-Table-based Processing-in-Memory Architecture for Deep Learning Acceleration
Sathwika Bavikadi¹, Purab Ranjan Sutradhar², Amlan Ganguly², Sai Manoj Pudukotai Dinakarao¹
¹George Mason University, ²Rochester Institute of Technology

11:25AM
3B.3
HFGCN: High-speed and Fully-optimized GCN Accelerator
MinSeok Han¹, Jiwan Kim¹, Donggeon Kim¹, Hyunuk Jeong¹, Gilho Jung¹, Myeongwon Oh¹, Hyundong Lee², Yunjeong Go², HyunWoo Kim¹, Jongbeom Kim¹, Taigon Song¹
¹Kyungpook National University (KNU), ²Kyungpook National University

11:45AM
3B.4
Knowledge Distillation between DNN and SNN for Intelligent Sensing Systems on Loihi Chip
Shiya Liu¹ and Yang Yi²
¹EMD Electronics, ²Virginia Tech
3B.5
Lightweight Instruction Set for Flexible Dilated Convolutions and Mixed-Precision Operands
Simon Friedrich¹, Shambhavi Balamuthu Sampath², Robert Wittig¹, Manoj Rohit Vemparala³, Nael Fasfous³, Emil Matus⁴, Walter Stechele⁵, Gerhard Fettweis¹
¹TU Dresden, ²BMW, ³BMW AG, ⁴Technische Universität Dresden, ⁵TUM

SESSION 3C
Thursday April 6
Intelligent Edge Computing

Chair: Hossein Sayadi, California State University, Long Beach

10:45AM
3C.1
PriML: An Electro-Optical Accelerator for Private Machine Learning on Encrypted Data
Mengxin Zheng¹, Fan Chen¹, Lei Jiang¹, Qian Lou²
¹Indiana University Bloomington, ²University of Central Florida

11:05AM
3C.2
ISSAC: An Self-organizing and Self-healing MAC Design for Intermittent Communication Systems
Ruben Dominguez¹, Wen Zhang¹, Hongzhi Xu², Pablo Rangel³, Chen Pan⁴
¹Texas A&M University - Corpus Christi, ²Jishou University, ³Texas A&M University - Corpus Christi, ⁴Texas A&M University-Corpus Christi
11:25AM
3C.3
**A Deep Learning Approach for Ventricular Arrhythmias Classification using Microcontroller**
Ya-sine Agrignan\(^1\), Shanglin Zhou\(^1\), Jun Bai\(^1\), Sahidul Islam\(^2\), Sheida Nabavi\(^1\), Mimi Xie\(^2\), Caiwen Ding\(^1\)
\(^1\)University of Connecticut, \(^2\)University of Texas at San Antonio

11:45AM
3C.4
**Reinforcement Learning-Based Guidance of Autonomous Vehicles**
Joseph Clemmons and Yufang Jin
University of Texas at San Antonio

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**SESSION 4A**

Thursday April 6

**Advances in Analysis, Simulation and Computing**

Chair: Chidhambaranathan Rajamanikkam, Utah State University
Co-Chair: Anand Iyer, Synopsys Inc.

2:10PM
4A.1
**Fast Electromigration Simulation for Chip Power Grids**
Bijan Shahriari and Farid Najm
University of Toronto

2:30PM
4A.2
**On-Interposer Decoupling Capacitors Placement for Interposer-based 3DIC**
Po-Yang Chen, Chang-Yun Liu, Hung-Ming Chen, Po-Tsang Huang
National Yang Ming Chiao Tung University
2:50PM

4A.3

Analysis of Pattern-dependent Rapid Thermal Annealing Effects on SRAM Design
Vidya Chhabria\textsuperscript{1} and Sachin S. Sapatnekar\textsuperscript{2}
\textsuperscript{1}Arizona State University, \textsuperscript{2}University of Minnesota

3:10PM

4A.4

Reverse Engineering Word-Level Models from Look-Up Table Netlists
Ram Venkat Narayanan, Aparajithan Nathamuni-Venkatesan, Kishore Pula, Sundarakumar Muthukumaran, Ranga Vemuri
University of Cincinnati

3:30PM

4A.5

Novel Implementation of High-Performance Polynomial Multiplication for Unified KEM Saber based on TMVP Design Strategy
Pengzhou He and Jiafeng Xie
Villanova University

SESSION 4B

Thursday April 6

Hardware Security: Attacks and Defenses

Chair: Soheil Salehi, University of Arizona

2:10PM

4B.1

Unraveling Latch Locking Using Machine Learning, Boolean Analysis, and ILP
Dake Chen\textsuperscript{1}, Xuan Zhou\textsuperscript{1}, Yinghua Hu\textsuperscript{1}, Yuke Zhang\textsuperscript{1}, Kaixin Yang\textsuperscript{1}, Andrew Rittenbach\textsuperscript{2}, Pierluigi Nuzzo\textsuperscript{1}, Peter Beerel\textsuperscript{3}
\textsuperscript{1}University of Southern California, \textsuperscript{2}USC Information Sciences Institute, \textsuperscript{3}Univ. of Southern California
2:30PM

**4B.2**

Resynthesis-based Attacks Against Logic Locking

Felipe Almeida¹, Levent Aksoy¹, Quang-Linh Nguyen², Sophie Dupuis³, Marie-Lise Flottes³, Samuel Pagliarini⁴

¹Tallinn University of Technology, ²LIRMM, ³LIRMM CNRS, ⁴Tallinn University of Technology (TalTech)

2:50PM

**4B.3**

VAST: Validation of VP-based Heterogeneous Systems against Availability Security Properties using Static Information Flow Tracking

Ece Demirhan Coskun¹, Muhammad Hassan¹, Mehran Goli², Rolf Drechsler²

¹Cyber-Physical Systems, DFKI GmbH, ²Institute of Computer Science, University of Bremen

3:10PM

**4B.4**

MAAS: Hiding Trojans in Approximate Circuits

Qazi Arbab Ahmed¹, Muhammad Awais¹, Marco Platzner²

¹Paderborn University, ²Paderborn University

3:30PM

**4B.5**

Efficient Decryption Architecture for Classic McEliece

Xinyuan Qiao, Suwen Song, Jing Tian, Zhongfeng Wang

Nanjing University
SESSION 4C

Thursday April 6

Design for Heterogeneous Integration

Chair: Gina Adam, George Washington University

2:10PM
4C.1 Testbench on a Chip: A Yield Test Vehicle for Resistive Memory Devices
Luke Upton¹, Guenole Lallement¹, Michael Scott¹, Joyce Taylor², Robert Radway¹, Dennis Rich¹, Mark Nelson³, Subhasish Mitra¹, Boris Murmann¹
¹Stanford University, ²Intrinsix Corporation, ³SkyWater Technology

2:30PM
4C.2 Integrating emerging devices with CMOS for analog in-memory computing
Qiangfei Xia
University of Massachusetts Amherst

2:50PM
4C.3 Integrating Emerging Memories for Analog DNN Accelerators
An Chen
IBM

3:10PM
4C.4 An Infrastructure for Large-scale Reconfigurable Neuronal Network Emulations
Gopabandhu Hota and Gert Cauwenberghs
UC San Diego
SESSION 5A

Friday April 7

Low Power Circuit Design

Chair: Amit Trivedi, University of Illinois at Chicago
Co-Chair: Hongyu An, Michigan Technological University

9:00AM
5A.1
173 A Novel Pseudo-Flash Based Digital Low Dropout (LDO) Voltage Regulator
Cheng-Yen Lee\textsuperscript{1}, Sunil Khatri\textsuperscript{1}, Sarma Vrudhula\textsuperscript{2}
\textsuperscript{1}Texas A&M University, \textsuperscript{2}Arizona State University

9:20AM
5A.2
20 A Low Power SRAM with Fully Dynamic Leakage Suppression for IoT Nodes
Jun Yin and Mircea Stan
University of Virginia

9:40AM
5A.3
118 Error Diluted Approximate Multipliers Using Positive And Negative Compressors
Bindu G Gowda\textsuperscript{1}, Prashanth H C\textsuperscript{2}, Madhav Rao\textsuperscript{3}
\textsuperscript{1}International Institute of Information Technology Bangalore, \textsuperscript{2}IIIT-Bangalore, \textsuperscript{3}International Institute of Information Technology-Bangalore

10:00AM
5A.4
138 Scalable Low-Cost Sorting Network with Weighted Bit-Streams
Brady Prince\textsuperscript{2}, Hassan Najafi\textsuperscript{2}, Bingzhe Li\textsuperscript{1}
\textsuperscript{1}Oklahoma State University, \textsuperscript{2}University of Louisiana
SESSION 5B

Friday April 7

Advance Secure Circuits and Hardware Trojan Detection

Chair: Setareh Rafatirad, University of California Davis

9:00AM
5B.1

Novel, Configurable Approximate Floating-point Multipliers for Error-Resilient Applications
Vishesh Mishra1, Sparsh Mittal2, Rekha Singhal3, Manoj Nambiar3
1IIT Kanpur, 2IIT Roorkee, 3TCS Research

9:20AM
5B.2

Design Space Exploration of Modular Multipliers for ASIC FHE accelerators
Deepraj Soni1, Mohammed Nabeel Thari Moopan2, Homer Gamil3, Oleg Mazonka4, Brandon Reagen5, Ramesh Karri6, Michail Maniatakos4
1New York University Tandon School of Engineering, 2New York University, 3NYUAD, 4New York University Abu Dhabi, 5NYU/Facebook, 6NYU

9:40AM
5B.3

H-Saber: An FPGA-Optimized Version for Designing Fast and Efficient Post-Quantum Cryptography Hardware Accelerators
Andrea Guerrieri1, Gabriel Da Silva Marques2, Francesco Regazzoni3, Andres Upegui2
1EPFL and HES-SO, 2University of Applied Sciences Western Switzerland, 3University of Amsterdam and Universita della Svizzera Italiana

10:00AM
5B.4

A Novel Method Against Hardware Trojans in Approximate Circuits
Yuqin Dou1, CHONGYAN GU2, Chenghua Wang1, Weiqiang Liu1
1Nanjing University of Aeronautics and Astronautics, 2Queen's University Belfast
Using Path Features for Hardware Trojan Detection Based on Machine Learning Techniques

Chia-Heng Yen¹, Jung-Che Tsai¹, Kai-Chiang Wu²

¹National Yang Ming Chiao Tung University, ²Department of Computer Science, National Chiao Tung University
SESSION 5C

Friday April 7

Efficient Algorithm, Hardware, and Computing Paradigm for Machine Learning

Chair: Kang Jun Bai, AFRL

9:00AM
5C.1
Locality-sensing Fast Neural Network (LFNN): An Efficient Neural Network Acceleration Framework via Locality Sensing for Real-time Videos Queries
Xiaotian Ma, Jiaqi Tang, Yu Bai
California State University, Fullerton

9:20AM
5C.2
Image Quantization Tradeoffs in a YOLO-based FPGA Accelerator Framework
Richard Yarnell, Mousam Hossain, Ronald DeMara
University of Central Florida

9:40AM
5C.3
Automatic Subnetwork Search Through Dynamic Differentiable Neuron Pruning
Zigeng Wang\textsuperscript{1}, Bingbing Li\textsuperscript{1}, Xia Xiao\textsuperscript{1}, Tianyun Zhang\textsuperscript{2}, Mikhail Bragin\textsuperscript{1}, Bing Yan\textsuperscript{3}, Caiwen Ding\textsuperscript{1}, Sanguthevar Rajasekaran\textsuperscript{1}
\textsuperscript{1}University of Connecticut, \textsuperscript{2}Cleveland State University, \textsuperscript{3}Rochester Institute of Technology

10:00AM
5C.4
A Novel Stochastic LSTM Model Inspired by Quantum Machine Learning
Joseph Lindsay and Ramtin Zand
University of South Carolina
SESSION 6A

Friday April 7

Design of Emerging Circuits & Systems

Chair: Rasit Topaloglu, IBM
Co-Chair: Ujwal Radhkrishna, Texas Instruments Inc.

10:45AM
6A.1
An Area Efficient Superconducting Unary CNN Accelerator
Patricia Gonzalez-Guerrero, George Michelogiannakis, Kylie Huch, Nirmalendu Patra, Thom Popovici
LBL

11:05AM
6A.2
A Novel Scalable Array Design for III-V Compound Semiconductor-based Non-volatile Memory (UltraRAM) with Separate Read-Write Paths
Shamiul Alam¹, Kazi Asifuzzaman², Ahmedullah Aziz³
¹University of Tennessee Knoxville, ²Oak Ridge National Laboratory, ³University of Tennessee, Knoxville

11:25AM
6A.3
ZOCHEN: Compression using Zero chain elimination and encoding to improve endurance of Non-volatile Memories
Nishant Bharti¹, Arijit Nath², Swati Upadhyay³, Hemangee Kapoor³
¹IIT Guwahati, ²IIT Guwahati, India, ³Indian Institute of Technology Guwahati

11:45AM
6A.4
A Polymorphic Electro-Optic Logic Gate for High-Speed Reconfigurable Computing Circuits
Venkata Sai Praneeth Karempudi, Sairam Sri Vatsavai, Ishan Thakkar, Todd Hastings
University of Kentucky
SESSION 6B

Friday April 7

Novel AI Computing

Chair: Hongyu An, Michigan Technological University
Co-Chair: Haowen Fang, Synopsys

10:45AM
6B.1
87 Spiking Domain Feature Extraction with Temporal Dynamic Learning
Honghao Zheng and Yang (Cindy) Yi
Virginia Tech

11:05AM
6B.2
37 Moving Towards Game-Changing Technology: Fabrication and Application of HfO2 RRAM for In-Memory Computing
Kang Jun Bai1, Daniel Titcombe2, Jack Lombardi1, Clare Thiem1, Nathaniel Cady2
1Air Force Research Laboratory, 2SUNY Polytechnic Institute

11:25AM
6B.3
133 Cache Register Sharing Structure for Channel-level Near-memory Processing in NAND Flash Memory
HyunWoo Kim1, Seungwon Baek1, Minyoung Jung3, Jaehong Song1, Hyodong Kim1, Junhyeon Kim1, Seongju Kim1, Taigon Song1, Jongbeom Kim1, Hyundong Lee3, Yunjeong Go3
1Kyungpook National University (KNU), 2Kyungpook National University (KNU), 3Kyungpook National University

11:45AM
6B.4
73 Online Training from Streaming Data with Concept Drift on FPGAs
Esther Roorda and Steve Wilton
University of British Columbia
SESSION 6C

Friday April 7

Security for Resource-Limited Devices

Chair: Ava Hedayatipour, California State University, Long Beach

10:45AM
6C.1
Attacks on Continuous Chaos Communication and Remedies for Resource Limited Devices
Rahul Vishwakarma¹, Ravi Monani², Amin Rezaei², Hossein Sayadi², Mehrdad Aliasgari², Ava Hedayatipour³
¹California State University Long Beach, ²California State University, Long Beach, ³CSULB

11:05AM
6C.2
Split-Slope Chaotic Map Providing High Entropy Across Wide Range
Partha Sarathi Paul¹, Maisha Sadia¹, Anurag Dhungel¹, Parker Hardy¹, Md Sakib Hasan²
¹Graduate Student, ²Assistant Professor

11:25AM
6C.3
Reconfigurable low-power Cryptographic processor based on LFSR for Trusted IoT platforms
Mohamed El-Hadedy¹, Russell Hua², Kazutomoyoshi³, Wen-mei Hwu⁴, Martin Margala⁵
¹CalPoly Pomona, ²California State Polytechnic University, Pomona, ³Argonne National Lab, ⁴University of Illinois at Urbana-Champaign, ⁵University of Louisiana at Lafayette
Automating Hardware Trojan Detection Using Unsupervised Learning: A Case Study of FPGA

Jaya Dofe¹, Shailesh Rajput², Wafi Danesh³

¹California State University, ²California State University Fullerton, ³University of Missouri, Kansas City
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