Call for Papers

ISQED 2015
16th International Symposium & Exhibits on
QUALITY ELECTRONIC DESIGN

ISQED Symposium 2015
www.ISQED.org

March 2-4, 2015. Santa Clara Convention Center, Santa Clara, CA, USA

The International Symposium on Quality Electronic Design (ISQED) is the leading Electronic IC and System Design conference, aimed at bridging the gap among electronic design tools and processes, integrated circuit technologies, processes & manufacturing, to achieve design quality. ISQED is the pioneer and leading international conference dealing with design for manufacturability and quality issues front-to-back. ISQED emphasizes a holistic approach toward electronic design and intends to highlight and accelerate cooperation among the IC & System Design, EDA, Semiconductor Process Technology and Manufacturing communities. ISQED spans three days, Monday through Wednesday, in three parallel tracks, hosting over 100 technical presentations, several keynote speakers, workshops/tutorials and other informal meetings. Past conference proceedings and papers have been published in the IEEE Xplore digital library and indexed by SCOPUS. For any question please contact the publication committee by sending email to isqed2015@isqed.org. Alternatively you may contact the TPC chair Dr. Peter Wright at pwright.isqed@gmail.com.

Papers are accepted in the following areas

A pioneer and leading multidisciplinary conference, ISQED accepts and promotes papers in the following areas:

Hardware and System Security (HSS)

Hardware security attacks and defenses. Side-channel attacks and prevention. Reverse engineering and hardware obfuscation. Hardware tamper and Trojan detection. Hardware authentication and attestation. Hardware-based security primitives including PUFs, TRNGs and ciphers. Security, privacy, and trust protocols using hardware security primitives. Trusted information flow using integration of architecture and hardware security primitives. Trusted synthesis using untrusted tools. Trusted manufacturing including split manufacturing, remote integrated circuit enabling and disabling, watermarking, and fingerprinting. Hardware and software usage metering techniques. Techniques and metrics for hardware system data confidentiality, hardware design confidentiality, integrity and authenticity. System security assessment techniques. Computer architecture and implementation techniques that ensure software and/ or system security. Approaches for trusted remote sensing and computing.

Smart Sensors & IoT - Design and Technology (SSDT)

Sensor and actuator devices for IOT and industrial use. Circuits and links, and their design for sensor interfaces. Energy harvesting techniques. Device, circuit, and package level modeling of sensors. Sensor calibration. Networked sensors and data processing algorithms. Sensor fusion and sensor networks. Bio-sensors. Energy management in sensor chips. Sensors for robotics. Wearable and implantable sensors. Wireless sensor networks. Environmental sensors and sensors for ambient assisted living, for building automation, for automotive applications, and for aircraft. Underlying device technologies for sensors, such as MEMS, magnetic, optical, etc. Touch screen sensors and capacitive vs. resistive sensing. Temperature sensors and arrays. Sensor Integration: Hardware & Software. Indoor positioning and navigation using inertial sensors. MEMS microphones and speakers. Chemical sensors.

System-level Design and Methodologies (SDM)

Emerging system-level design paradigms, methods and tools aiming at quality of systems including multi-core processors, embedded systems, SoC, novel accelerator designs, and heterogeneous architecture designs. ESL design process and flow management. System-level design modeling, analysis, synthesis, and estimation for correct high-quality hardware/software systems. New concepts, methods and tools addressing the hardware and system design complexity and usage of technology information and manufacturing feedback in the system-, RTL- and logic level design. The influence of the nanometer technologies' issues on the system-, RTL- and logic-level design. System-level trade-off analysis and multi-objective (e.g. yield, power, delay, area, etc.) optimization.

Package and Three-Dimensional Integration (PTDI)

Architecture, circuit, package, and PCB/PWB design and effect on quality in emerging forms of vertical integration including 3D IC, 2.5D Interposer, multi-chip module, and other innovative packaging techniques. Tools and methodologies dealing with electrical, stress, and thermal modeling and simulation for improved quality of product. Novel partitioning, power delivery design, clock tree design, heatsink/cooling methods, and design for test/yield techniques in vertically integrated circuits/chips. Design and technology solutions in system-on-chip versus system in a package (SiP) solutions. Die-package co-design and trade-off analysis.

Integrated Circuit Design (ICD)

Low power circuits, memory, analog, RF, programmable logic, and FPGA circuits. Power-aware computing and communication. Design techniques and architecture for leakage current management, total power optimization, and power management. Low power interconnect solutions. Analog-to-digital and digital-to-analog converters. Robust SRAM cell and circuits. Effect of device and process reliability, robustness, and variation on the design of reliable circuits. Circuit design for reliability effects such as gate oxide integrity, electromigration, ESD, HCI, NBTI, PBTI etc.

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EDA Methodologies & IP Cores; Interoperability, Security, and Reuse (EDA)

EDA tools addressing management of design process, design flows and design databases. EDA tools interoperability issues and implications. Emerging EDA standards. EDA design methodologies and tools that address issues which impact the quality of the realization of designs into physical integrated circuits. IP modeling and abstraction. Design and maintenance of technology independent hard and soft IP blocks. Methods and tools for analysis, comparison and qualification of libraries and hard IP blocks. Challenges and solutions of the integration, testing, qualifying, and manufacturing of IP blocks from multiple vendors. Third party testing of IP blocks. Risk management of IP reuse. IP authoring tools and methodologies. Design for IP security. Novel techniques for IP water marking. Application of EDA tools to non-traditional problems such as smart power grid, Solar energy, etc.

Design Verification and Design for Testability (DVFT)

Hardware and software formal, assertion, and simulation based design verification techniques to ensure the functional correctness of hardware early in the design cycle. DFT and BIST for digital and SoC. DFT for analog/mixed-signal ICs and systems-on-chip, DFT/BIST for memories. Test synthesis and synthesis for testability. DFT economics, DFT case studies. DFT and ATE. Fault diagnosis, IDDQ test, novel test methods, effectiveness of test methods, fault models and ATPG, and DPPM prediction. SoC/IP testing strategies. Design methodologies dealing with the link between testability and manufacturing.

Physical Design, Methodologies & Tools (PDM)

Physical design for manufacturing; Physical synthesis flows for correct-by-construction quality silicon, implementation of large SoC designs. Tool frameworks and data-models for tightly integrated incremental synthesis, placement, routing, and timing analysis. Placement, optimization, and routing techniques for low-power and noise sensitivity reduction. Tool flows and techniques for antenna rule and electromigration rule avoidance and fixing. Spare-cell strategies for ECO, decoupling capacitance and antenna rule fixing. Reliable clock distribution methodologies for Gigahertz designs and near/sub-threshold designs. Physical design methodologies and tools, dealing with issues such as: timing closure, R, L, C extraction, ground/Vdd bounce, signal noise, cross-talk, substrate noise, power rail integrity, electromigration, hot carriers, EOS/ESD, plasma induced damage and other yield limiting effects, high frequency effects, thermal effects, power estimation, and EMI/EMC.

Emerging Process & Device Technologies and Design Issues (EDT)

Emerging processes & device technologies and implications on IC design with respect to the design's time to market, yield, reliability, and quality. Emerging issues in new and novel technologies such as Double-Gate (DG)-MOSFET, FinFETs, tunnel FETs, GAA, DSA, SWD, high-bandwidth metallization, carbon nanotubes, and nano devices. Advanced SOI technologies such as trap-rich high-resistivity SOI, etc for wireless front-end SOC implementation. Specialty technologies (eg. MEMs, CIS co-integration with application processors) for the IOT market. Device design and circuit optimization in emerging non-volatile memory and logic, such as Spin-Transfer Torque MRAM, Spintronic electronics, Phase Change Memory, Resistive RAM, and Memristors, 3D integration . Use of novel devices for cognitive computing, quantum computing, neuromorphic computing.

Design Technology Co-Optimization; Designing at the Manufacturing Frontier (DTCO)

Optimization-based methodologies that address the interaction between design (custom, semi-custom, ASIC, FPGA, RF, memory, etc.) and advanced-node manufacturing techniques such as multiple patterning, EUV, SADP, DSA, monolithic 3D, advanced interconnect (air gap for local interconnect, Si-photonics,…), etc. DFM/DFY/DFQ definitions, methodologies, matrices, and standards. Analysis, modeling, and abstraction of manufacturing process parameters and effects for accurately predicting and/or optimizing silicon performance including reliability and aging mechanisms, variation parameters, and circuit-level analysis. Design, synthesis, and place and route of ICs considering factors such as: OPC, phase shifting, proximity correction, sub-wavelength lithography, manufacturing yield, and technology capability. Design and manufacturability issues for digital, analog, mixed signal, RF, MEMS, opto-electronic, biochemical-electronic, and nanotechnology based ICs. Redundancy and other yield improving techniques. Global, social, and economic implications of design quality. Mask making methods and advances impacting manufacturability and yield. Single event upset/transient fail analysis.

Submission of Papers

Paper submission must be done on-line through the conference web site at **www.isqed.org**. The guidelines for the final paper format are provided on the conference web site. Authors should submit original, unpublished papers (4 pages long and consistent with the format provided in the ISQED website) along with an abstract of about 200 words. Accepted submissions can provide a revised paper from 4-8 pages long. To permit a **blind review**, **do not** include name(s) or affiliation(s) of the author(s) on the manuscript and abstract. The complete contact author information needs to be entered separately. Please check the as-printed appearance of your paper before sending your paper. In case of any problems email isqed2015@isqed.org. Please note the following important dates:

Paper Submission Deadline	**Sept. 19, 2014**
Acceptance Notifications	December 5, 2014
Final Camera-Ready paper	January 10, 2015

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