Electrical Characteristic and Power Consumption Fluctuations of Trapezoidal Bulk FinFET Devices and Circuits Induced by Random Line Edge Roughness

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Abstract

In this work, we use an experimentally calibrated 3D quantum-mechanically-corrected device simulation to study different types of line edge roughness (LER) on the DC/AC and digital circuit characteristic variability of 14-nm-gate HKMG trapezoidal bulk FinFETs. By using a time-domain Gaussian noise function as the LER-profile generator, we compare four types of LER: fin-LER inclusive of resist-LER and spacer-LER, sidewall-LER, and gate-LER for the trapezoidal bulk FinFETs. The resist-LER is most influential on characteristic fluctuation. For the same type, spacer-LER has at least 85 % improvement on σV_{th} compared with resist-LER. As for the digital circuit characteristic, the rectangle-shape bulk FinFET has larger timing fluctuation.

Keywords

Line edge roughness, fin-, resist-, spacer-, sidewall-, gate-LER, trapezoidal bulk FinFET, and digital circuit.

1. Introduction

Multi-gate FETs are in great demand for the CMOS technology downscaling beyond the sub-22 nm. HKMG bulk FinFET transistor is one of the promising candidates owing to the better gate control and suppression on short-channel effects (SCEs) [1]. In addition to the improvement on DC characteristics, device manufacturability and its fluctuation suppression are also crucial issues for further scaling [2]. In reality, fabricating a fin channel with uniform thickness along the fin-height, fin-width, and gate-length direction is incapable under the limitation on lithography processes and etching steps [3]. The actual channel fins may be fabricated as trapezoidal shape and device performance will be degraded by remarkable SCEs. For variability issues, random dopant fluctuation (RDF) is a major fluctuation source [4-5] for low-standby-power devices due to the need of heavy channel doping implantation in enhancing the threshold voltage (V_{th}); while the workfunction fluctuation (WKF) and LER [6] plays a significant role in characteristic variation for the device with low cannel doping implantation. So far, it has been reported that using the amorphous TaSiN as gate metal material can largely reduce the WKF [7]. However, LER is still severe and becomes more serious in the nano-sized multi-gate devices since the LER does not scale down with technology node [8]. Multi-gate FETs are particularly sensitive to LER because the gate control ability is highly related to the physical geometry [9]. Various researches about LER and nonideal geometry of FinFET devices were reported recently [10-11, 14-16]; nevertheless, the study which contains both issues simultaneously has not been well investigated yet. Furthermore, the AC and digital circuit characteristic of trapezoidal bulk FinFETs fluctuated by LER have rarely been paid attention to.

In this study, different type of LER on characteristic fluctuation of trapezoidal bulk FinFETs is compared and explored. For DC characteristic, the on-/off-state current characteristic and SCE parameters' fluctuation of the 14-nm-gate trapezoidal HKMG bulk FinFET are investigated. For AC and digital circuit characteristic, the gate capacitance, timing, and power consumption are analyzed. The article is organized as follows. Sec. 2 briefs the statistical simulation method for generating LER profile on trapezoidal bulk FinFET devices with different fin angles. Sec. 3 discusses the characteristic fluctuation from each type of LER on the studied devices. Finally, the conclusions are drawn.

2. Device Configuration and Simulation Method

The fin angle (θ) is defined as the angle between the sidewall and horizontal line in bottom side of the fin channel. The fin angle may vary with the lithography, STI, and etching. Therefore, fin channels of devices with different trapezoidal shapes are fabricated. The structural parameters are shown in Fig. 1(a). In this study, we assume that the top-fin width (W_{top}) is fixed at 8 nm and the bottom-fin (W_{bottom}) widths vary with the fin angle for the 14-nm-gate HKMG bulk FinFET devices. The fin angle ranges from 70^o to 90^o. The $W_{sidewall}$ varies while the fin height is fixed at 16 nm. The total fin width (W_{total}) = $2 \times W_{sidewall} + W_{top}$, where W_{top} and W_{bottom} are top and bottom fin widths. The value of W_{total} is getting larger when the fin angle is getting smaller. The absolute value of the nominal V_{th} of trapezoidal bulk FinFETs with different fin angles is 250 mV. The subthreshold swing (SS) and drain induced barrier lowering (DIBL) are degraded due to the large fin width and poor gate control. Fig. 1(b) shows the LER simulation method. A Gaussian noise function is used to generate random line edge profiles and then appends them on the regular edges of nominal trapezoidal bulk FinFETs. The standard deviation is set to 1 nm. The magnitude distribution of line edge profiles is followed by Gaussian distribution. To capture devices' characteristic affected by the surface roughness and LER scattering, Enhanced Lombardi model [12], which considers mobility degradation at silicon-insulator interface due to scattering and calculates a normal electric field dependent mobility, is included in the 3D quantum-mechanically corrected device simulation. The device model includes the drift-diffusion equations coupled with the density gradient equations [2-3, 13]. Figs. 2(a)-(c) shows four types of LER on the fin channel and gate material; they are fin-LER, which

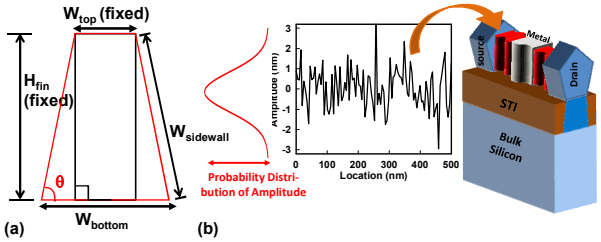

Figure 1: (a) Cross-sectional plot of device structure. (b) The simulation method of LER. For the LER simulation, Gaussian noise function is used to generate random edge profiles and then append them on the regular edges of nominal bulk FinFET devices. The distribution of edge amplitude follows Gaussian distribution.

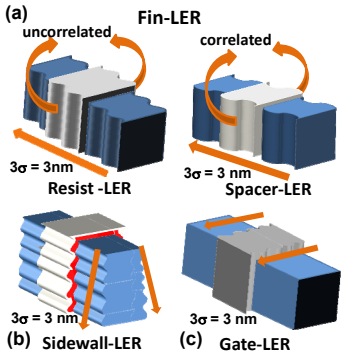

Figure 2: Different LER of FinFET devices. (a) Fin-LER (b) Sidewall-LER (c) Gate-LER. The fin-LER can be grouped into resist-LER and spacer-LER based on the process method. The standard deviation of each LER is set to 1 nm.

can be grouped into resist-LER, and spacer-LER based on the fin patterning technology, sidewall-LER, and gate-LER. The fin-LER is that the fin width varies along the direction from the source to drain sides. The difference between the resist- and spacer-LER is the correlation of line edge roughness profiles between two edges of the fin channel. The resist-LER has different displacement at two sides of fin channel edge. The spacer-LER has almost the same line edge roughness at two sides of fin edges, which the fin width is identical along the channel direction. The sidewall-LER is the fin width variation at the sidewall of the fin channel, which is perpendicular to the source side to the drain side. The rough profiles at two fin sidewalls are not the same. The gate-LER can be treated as the parallel connection of many FETs with different gate lengths.

3. Results and Discussion

3.1. DC Characteristic

LER is stochastic and is difficult to be corrected by optical proximity correction. It is affected by many factors during pattern definition and fundamentally induced by erosion of polymer at the edges of a resist during fabrication. The on-/off-state current characteristics of the bulk FinFET devices with different fin angles under the resist- LER, sidewall-LER, gate-LER, and spacer-LER are shown in Figs. 3 (a)-(d), respectively. For bulk FinFETs with a larger fin angle has small on-state current due to the small W_{total}; however, the on-/off-state current ratio is better because the

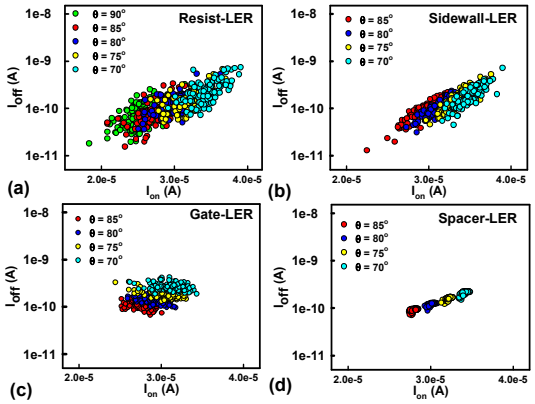

Figure 3: The I_{on}-I_{off} characteristic of the bulk FinFETs with different fin angles under the (a) resist-LER, (b) sidewall-LER, (c) gate-LER, and (d) spacer-LER.

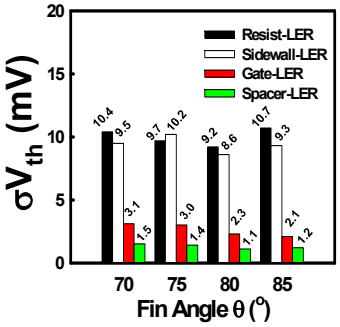

Figure 4: The V_{th} fluctuation of trapezoidal bulk FinFET devices with different fin angles fluctuated by LERs.

off-state current can be significantly reduced by good gate control of narrow fin width. Moreover, the resist-LER and sidewall-LER make the on-/off-state current distribution be dispersive, and the degree of dispersion has small correlation with the fin angle. Figure 4 shows the plot of V_{th} fluctuation (σV_{th}) versus bulk FinFETs with different fin angles suffering from different types of LER. For the viewpoint of gate control, the spacer-LER gives rise to the similar gate control due to same fin width of all the fluctuated devices. However, the fin width varies dramatically along the fin channels for those resist-LER-fluctuated devices. Thus, the gate control would be seriously affected and surface roughness is severe. Comparing resist-LER with spacer-LER, there is at least 85% improvement from resist-LER to spacer-LER on σV_{th}. The fin width related gate control plays a more significant role than the roughness scattering induced different level of mobility degradation for DC characteristic fluctuation. For the sidewall-LER, because of the coupling of electric field from the top gate and the lateral gates, the carriers do not flow from the source side to the drain side straightly. Therefore, conduction carriers suffer considerable surface roughness scattering compared with the resist-LER. However, the seriousness of the surface roughness scattering and gate control variation remain almost the same for the bulk FinFETs with the same fin width, the gate-LER and spacer-LER has slight σV_{th}. Overall, σV_{th} is almost independent on the fin angle for all LER, and resist-LER and sidewall-LER inducing σV_{th} is significant. We also find that

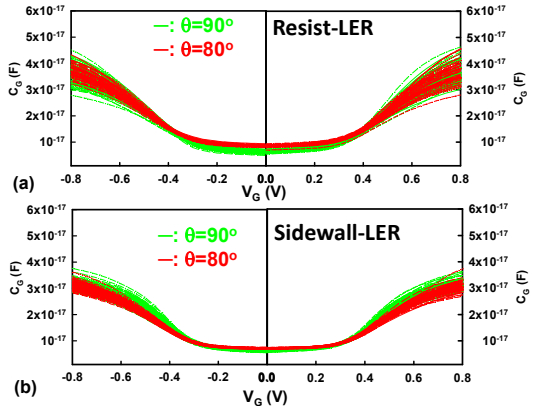

Figure 5: The dispersive C_G-V_G curves of rectangle bulk FinFET and trapezoidal one by resist- and sidewall-LER.

Table I: LIST OF THE GATE CAPACITANCE FLUCTUATION.

θ (°)	σC_G (F) Resist-LER		σC_G (F) Sidewall-LER	
	N	P	N	P
80	3.21E-18	3.33E-18	1.66E-18	1.86E-18
90	3.51E-18	2.4E-18	1.69E-18	1.67E-18

the resist-LER induces the largest fluctuation in DIBL and SS for every trapezoidal bulk FinFETs. The spacer-LER also has the least influence on the parameter variation of SCE.

3.2. AC and Digital Circuit Characteristic

The AC and digital circuit characteristic are displayed in following paragraphs. The gate capacitance versus gate voltage (C_G-V_G) characteristic of nominal rectangle-shape bulk FinFET and trapezoidal FinFET under the same $V_{th.}$ is calculated, the depletion gate capacitance of trapezoidal bulk FinFET is large due to the small depletion width by non-vertical gate coupling of sidewall gates. However, the inversion gate capacitance is small for trapezoidal bulk FinFET. We speculate the reason is that the inversion charges distribute farther from gate surface in trapezoidal bulk FinFETs than rectangle-shape bulk FinFETs. The equivalent thickness of inversion charge is large, thus, the inversion gate capacitance is small. Figs. 5 (a)-(b) show the dispersive C_G-V_G characteristic for N-/P-type bulk FinFET devices fluctuated by resist-LER, and sidewall-LER. At low gate bias, the capacitive response is dominated by depletion region. The variation of depletion width induced by LER is small under the vertical channel structure. Consequently, the same doping concentration gives rise to light fluctuation on gate capacitance no matter in 90-degree or 80-degree bulk FinFET. When high gate bias is achieved, the inversion charge dominates the capacitive response. The gate capacitance approximates to oxide capacitance, which equals ε_{SiO2}xArea/EOT. Due to the larger variation on gate area induced by LER, the fluctuation of inversion gate capacitance is serious. The associated values of fluctuation on gate capacitance (σC_G) of different-fin-angles and N-/P-type bulk FinFETs are listed in Table I. The influence of resist-LER is larger than that of sidewall-LER.

We further explore the digital characteristic fluctuated by LER of an inverter circuit. Fig. 6 shows the timing of resist-/sidewall-LER. Fig. 6(a) is the average time interval during falling transition is short due to the large driving capability

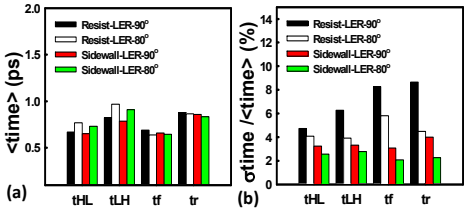

Figure 6: The timing of resist-/sidewall- LER on the studied bulk FinFET inverter.

Table II: LIST OF THE LOAD CAPACITANCE FLUCTUATION.

θ (°)	Resist-LER σC_{load} (F)	Sidewall-LER σC_{load}
80	4.76E-18	2.59E-18
90	4.10E-18	2.42E-18

of N-FinFET. For timing fluctuation, the rectangle-shape bulk FinFET has larger timing fluctuation, as shown in Fig. 6(b). It can be explained by the load capacitance fluctuation, as listed in Table II. The rectangle-shape bulk FinFET has large load capacitance fluctuation. Besides, the resist-LER induces large timing fluctuation in comparison with the timing fluctuation caused from sidewall-LER. This phenomenon also results from the load capacitance fluctuation, as listed in Table II.

Fig. 7 shows power consumptions of the studied devices. The total power (P_{total}) consists of the static power $P_{stat} = V_{DD} \cdot I_{leakage}$, the short circuit power $P_{sc} = f \cdot V_{DD} \cdot \int_T I_{sc}(\tau) d\tau$, and the dynamic power $P_{dyn} = C_{load} \cdot V_{DD}^2 \cdot f$, where $I_{leakage}$ is the leakage current that flows between the power rails in the absence of switching activity. The f is the clock rate. I_{sc} is the short circuit current, which is observed as both N-FinFET as well as P-FinFET are turned on and leading a DC path between the power rails. T is the switching period. As plotted in Fig. 7, the rectangle-shape bulk FinFETs show a smaller P_{stat} than the 80-degree bulk FinFETs due to the smaller leakage current. The short circuit power is determined by the time of existence of DC path between the power rails and the short circuit current. The inset of Fig. 7 plots the short circuit current versus the time interval of 90- and 80-degree bulk FinFETs, the 80-degree bulk FinFET has larger short circuit current than the rectangle-shape bulk FinFET. Therefore, the short circuit power dissipation of 80-degree bulk FinFET is larger than that of the rectangle-shape bulk FinFET device. For the dynamic power consumption, the rectangle-shape bulk FinFETs show larger dynamic power dissipation due to its larger load capacitance than that of 80-degree bulk FinFETs. Notably, the P_{dyn} and P_{sc} are the dominating factors in power dissipation. Figs. 8(a)-(b) show the normalized variation of each power consumption induced by the resist-LER and the sidewall-LER, respectively. The fluctuation of P_{stat} (σP_{stat}) is the largest one among all power consumptions. When electronic products are under standby models, large σP_{stat} is severe for battery power consumption. The magnitude of P_{stat} on the total operation power consumption is little; the fluctuation of total operation power consumption mainly induced by the fluctuation of P_{dyn} and P_{sc}. In the analysis of the resist-LER on power consumption, the variation of P_{sc} is particularly large of 80-degree bulk FinFETs. Overall, the fluctuation of total operation power

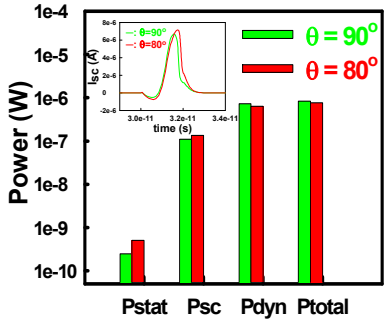

Figure 7: The power consumption of the nominal bulk FinFET devices and the inset is the short circuit current.

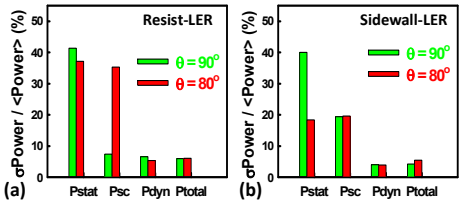

Figure 8: The normalized variation of each power consumption induced by (a) resist- and (b) sidewall-LER.

consumption follows the fluctuation of P_{sc}.

4. Conclusions

The electrical characteristic fluctuation of 14-nm-gate HKMG trapezoidal bulk FinFET induced by LER was analyzed. For the comparison between trapezoidal bulk FinFETs, different fin-angle trapezoidal bulk FinFETs suffer comparable DC characteristic fluctuation by the same type LER. The resist- and sidewall-LER significantly influence device characteristic among all LER. The influence of LER in the inverter circuit was estimated. The rectangle-shape device has larger timing fluctuation than that of trapezoidal one due to the larger σC_G. For the fluctuation of power consumption, the normalized σP_{stat} is larger than others. Moreover, resist-LER is most influential on DC/AC and power consumption fluctuation. The resist-defined pattering method can be replaced by spacer-defined patterning, where the fluctuation can be largely reduced.

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5. References

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