A Droop Measurement Built-in Self-Test Circuit for Digital Low-Dropout Regulators

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Abstract

Today's highly integrated system-on-chips (SOCs) employ several integrated voltage regulators to achieve higher power efficiency and smaller board area. Testing of voltage regulators is essential to validate the final product. In this work, we present a unique droop measurement built-in self-test (BIST) circuit for digital low-dropout regulators (DLDOs). The proposed BIST system is capable of storing transient droop information with less than 1.05 % error for droop voltages ranging from 45 mV to 520 mV for nominal DLDO output voltage of 1.6 V where supply voltage is 1.8 V. Additionally, a reuse based 10-bit successive-approximation (SAR) analog-to-digital converter (ADC) is incorporated to generate a digital output corresponding to the stored droop information as the BIST measurement result. The on-chip DLDO decoupling capacitor (~1 nF) is reconfigured as a charge scaling array for ADC operation during testing to increase reusability. The proposed BIST circuit is designed with 0.18 µm CMOS process in Cadence Virtuoso and verified with corner simulations.

Keywords

built-in self-test (BIST), droop measurement, voltage regulator, power management

1. Introduction

Lately, on-chip power management systems have drawn significant attention by the industry [1-3]. Advantages such as reducing circuit board real estate and enhancing the power efficiency make integrated voltage regulators a hot topic, especially for battery powered devices. However, increasing complexity in design to achieve aforementioned advantages brings challenges into test area. Since the integrated voltage regulator outputs are inherently tied to their load, they are not usually accessible from external pins. Conventional methods for testing or debugging are challenging due to routing complexity and accuracy concerns [4]. Therefore, on-chip test solutions for analog blocks are essential.

Even though the conventional analog low-dropout regulators (LDO) are realizable fully on-chip for integrated voltage regulation, their design is challenging in advanced low voltage process nodes. DLDOs are more suitable than analog LDOs at low voltage processes. DLDO has been first reported in [5] and it is considered as the conventional DLDO architecture, which is shown in Figure 1. It contains a clocked comparator, a bi-directional shift register, and a power PMOS array. It regulates the output voltage (V_{OUT}) by comparing V_{OUT} to an external reference voltage (V_{REF}) and instructing the shift register to increase or decrease the number of turned on power PMOS devices in each clock cycle. Due to the clocked control mechanism, its transient performance is inherently slower as compared to its analog counterpart. To overcome transient performance challenges, many design techniques have been presented [3], [6]-[9].

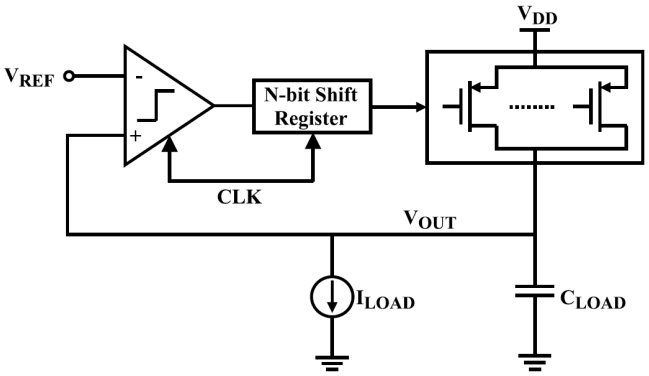

Figure 1: Conventional DLDO architecture.

There are several DLDO designs that use droop detection mechanisms embedded in their regulator core to enhance transient performance. For instance, in [6] and [7], a clocked window comparator is embedded in DLDO core for threshold based peak detection. In [8], a clocked comparator and a digital tunable-replica-circuit are used for droop detection. In [9], a time difference based digital control circuit is employed for transient event detection. Moreover, droop detection circuits are widely used in on-chip power supply monitors. In [10] and [11], analog, threshold based architectures are used to detect supply droop. In [12] and [13], analog, sample and hold based architectures are used while a digital based circuit is used in [14] to detect peaks of power supply voltage.

This paper presents a droop measurement BIST circuit suited for DLDO verification. A DLDO is used to serve as circuit-under-test (CUT) to prove BIST circuit functionality. A clocked, sample and hold based droop detector is used to store the undershoot voltage as a representation of droop. Clocked architecture eliminates the DC current consumption of the droop detector circuit. Proposed BIST circuit also includes a reuse based 10-bit SAR ADC to convert analog droop information to digital BIST output. The decoupling capacitor of DLDO (C_{LOAD}) is reconfigured as a charge scaling array during ADC operation. Additionally, the droop detector circuit is reconfigured and reused as a clocked comparator in ADC operation.

The rest of the paper is organized as follows. Section 2 describes the proposed test method. In section 3, circuit implementation of the building blocks is presented. Section 4 presents the simulation results. Finally, conclusion and future work are given Section 5.

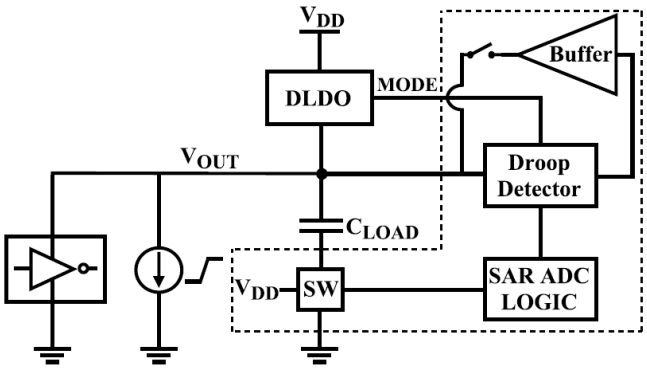

Figure 2: Droop measurement BIST test bench.

2. Proposed BIST method

Droop measurement BIST test bench is shown in Figure 2. It is composed of the DLDO, a droop detector, a SAR ADC logic, ADC switches (SW) connected to the bottom plate of the C_{LOAD}, an analog buffer, a test current load, and an inverter array to represent a digital load.

The droop measurement BIST starts with the assumption that the DLDO under test is in regulation. Once the load step is applied to the DLDO, the regulator output node, V_{OUT}, experiences a voltage droop. When the droop is detected by the DLDO, the BIST droop detector is triggered by the MODE signal from DLDO core as shown in Figure 2. The activated BIST droop detector tracks V_{OUT} and stores its lowest voltage during the transient event as a measurement of droop. After the minimum V_{OUT} is detected and stored, the DLDO is disabled and the system reconfigures itself for ADC operation. The SAR ADC logic outputs a 10-bit BIST measurement result corresponding to the detected lowest DLDO voltage.

There are several DLDOs capable of detecting output voltage overshoot and/or undershoot with different control mechanisms [6]-[8]. If such a case happens, a signal indicating that the DLDO is out of regulation is generated and the DLDO control loop responds to recover from this transient event. In this work, this signal is used to trigger test operation. The analog buffer shown in Figure 2 is used for ADC operation. The disabled inverter array, which is 20 times larger than the power PMOS array, was tied to V_{OUT} node to resemble a realistic digital load. The parasitics and leakage due to the disabled digital load are taken into account.

3. Circuit implementation

3.1. DLDO design

The architecture presented in [7] was adopted for DLDO design which serves as CUT to evaluate the proposed droop measurement system. The architecture incorporates a fine and coarse loop with an embedded peak detector. The fine loop uses smaller PMOS devices and a lower clock frequency whereas the coarse loop uses bigger PMOS devices and a higher clock frequency. Only the fine loop is enabled during steady-state. If the peak detector detects significant undershoot or overshoot, it enables the coarse loop for a short time for fast transient recovery.

This presented DLDO includes 32 fine and 32 coarse power PMOS devices. Clock signals of 20 MHz and 100 MHz frequencies were used in the fine and coarse loop, respectively. The peak detector output, MODE, goes high if V_{OUT} deviates from V_{REF} by +/-25 mV. A V_{REF} of 1.6 V is used for target V_{OUT} while V_{DD} is 1.8 V and C_{LOAD} is nearly 1 nF.

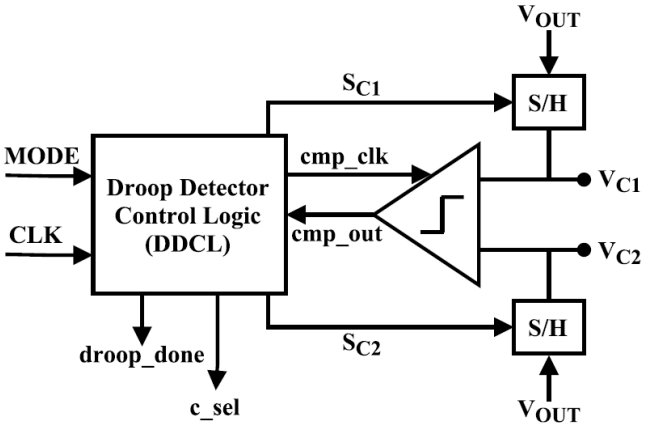

Figure 3: Droop detector block diagram.

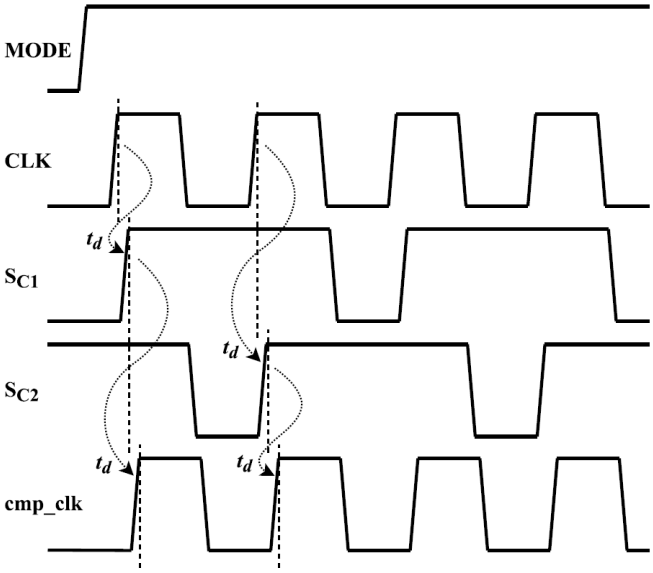

Figure 4: Timing diagram of the droop detector.

Unlike conventional DLDOs, the bottom plate of C_{LOAD} is not directly tied to ground as shown in Figure 2. Instead, it is connected to ground via NMOS type switches in order to reuse this capacitor block in ADC operation as a charge scaling capacitor array. The benefit of reusing the capacitor block for two different operations comes at the expense of additional resistance in series with the decoupling capacitor due to the added NMOS switch. This series resistance is reduced by using larger NMOS switches for regular DLDO operation.

3.2. Droop detector design

The simplified block diagram of the droop detector is shown in Figure 3. Similar to [13], two identical sample and hold (S/H) circuits are employed at the input stage. The rest of the circuit consists of a droop detector control logic (DDCL) and a clocked comparator. It uses the clock signal (CLK) from the DLDO core. The droop detector is enabled by the MODE signal generated by the DLDO indicating that

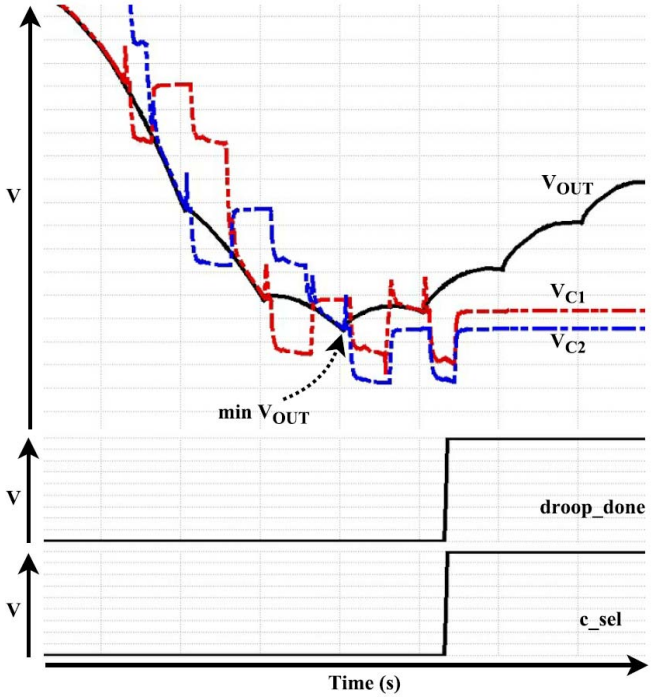

Figure 5: Droop detector operation during a transient event.

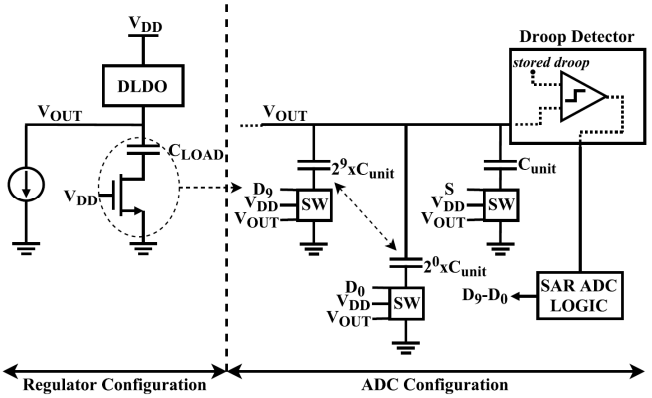

Figure 6: C_{LOAD} configuration in different operation modes.

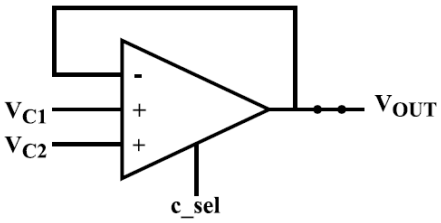

Figure 7: Buffer configuration.

the DLDO output is out of error band. Since the test applies a load step, the MODE signal is considered as a droop indicator. When this signal is received by the DDCL, the DLDO output already starts to decay and this is where droop detector is enabled.

The DLDO can only turn on or off a number of power PMOS devices at CLK rising edges. Therefore, when the load step is applied, the V_{OUT} decreases until a clock edge where the DLDO meets load current demand and V_{OUT} starts to recover from the droop. Until transient recovery starts, the lowest V_{OUT} is observed at the end of each clock cycle. Therefore, sampling V_{OUT} at clock edge during a droop event results in storing lowest V_{OUT} value in a given clock cycle.

DDCL is responsible for generating the sampling signals for sample and hold blocks (S_{C1} and S_{C2}) and comparator clock signal (cmp_clk) in a droop event. The timing diagram of the droop detector signals is given in Figure 4. When MODE goes high, S_{C1} and S_{C2} signals are generated to sample V_{OUT} on the sampling capacitors, alternatively at each rising edge of the CLK. The sampled voltages, V_{C1} and V_{C2}, are compared just after either of the sampling operations is completed with the cmp_clk signal. The comparator output is then evaluated by DDCL to determine if V_{OUT} continues to decay. In a monotonic V_{OUT} droop event, the comparator output toggles at each comparison. If the same output is received by DDCL, successively, the droop_done signal goes high indicating V_{OUT} started to rise.

An example of the droop detector operation is shown in Figure 5. As long as the latest sampled voltage is lower than the previously sampled voltage, which is stored by the other S/H block, the droop_done signal stays low. Once the DLDO starts to recover from the load step, the droop detector can respond to that change one clock cycle later and asserts the droop_done signal to stop the sampling operation. At that moment, the lowest value of V_{OUT} in the load step event is already stored in one of the S/H capacitors. The c_sel signal indicates the S/H capacitor that holds the lowest V_{OUT} value, which is used as ADC input.

In the S/H block design, the sampling capacitor was selected to be 1.5 pF and the sampling switch was designed with only PMOS devices. To reduce the error during the sampling phase due to charge injection and clock feedthrough, a charge cancellation PMOS device was added to the S/H block.

3.3. ADC design

A reuse based 10-bit SAR ADC was designed to convert the stored droop information to digital as a BIST measurement result. DLDO decoupling capacitor, C_{LOAD}, is reused as a charge scaling digital-to-analog converter (DAC) during this phase and the droop detector block was reused as ADC comparator as well. Figure 6 shows configurations of C_{LOAD} in two different operation modes. During regular DLDO operation, NMOS type switches connect bottom plate of the capacitor to ground. For ADC operation, C_{LOAD} is reconfigured as a capacitor array to be used as a DAC with ADC switches after NMOS switches are disabled.

Since C_{LOAD} is reconfigured as a DAC, the V_{OUT} node turns into the DAC output during the ADC operation, as shown in Figure 6. However, the parasitic capacitance related to V_{OUT} is significant as V_{OUT} is originally DLDO output. To mitigate the parasitics problem, the circuit technique proposed in [15] was implemented in the ADC design.

As the DAC output voltage, V_{OUT}, is tied to disabled DLDO power devices and load circuits, this voltage is prone to leakage during conversion. Making the DAC output node subject to leakage for a shorter time is important for measurement accuracy. Considering this fact, the already available 20 MHz clock signal was used for the ADC clock.

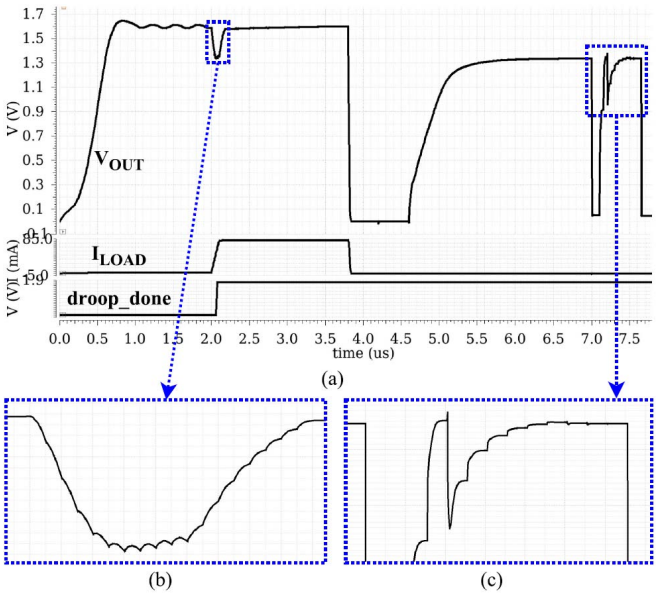

Figure 8: (a) V_{OUT} waveform during total BIST procedure. Zoomed V_{OUT} waveform during (b) load step event and (c) ADC operation.

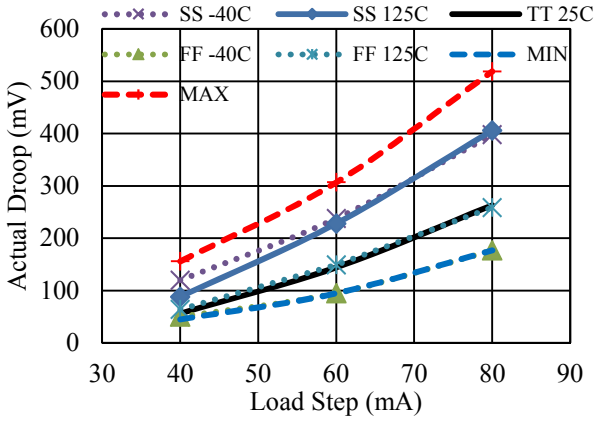

Figure 9: CUT droop voltages at different load steps.

So, there is no need for a dedicated ADC clock from external circuitry in this design. The unit capacitor (C_{unit}) is 950 fF and V_{DD} of 1.8 V was selected as ADC reference voltage since supply voltages are well controlled during wafer-level testing [4].

3.4. Buffer design

To make use of the technique proposed in [15], the ADC input should be sampled on the unit capacitors' top and bottom plates prior to conversion. Since the ADC input is analog droop information stored on a small S/H capacitor, the selected technique requires a circuit to buffer this voltage to V_{OUT} node. Therefore, a conventional Miller amplifier followed by a source follower input stage was used as the buffer. The simplified buffer configuration is shown in Figure 7. The droop detector outputs V_{C1} and V_{C2} are positive inputs of the buffer and c_sel signal determines which positive input is going to be buffered on V_{OUT}.

4. Simulation results

Figure 8(a) shows the entire droop measurement operation which can be shown in 4 steps. Initially, the

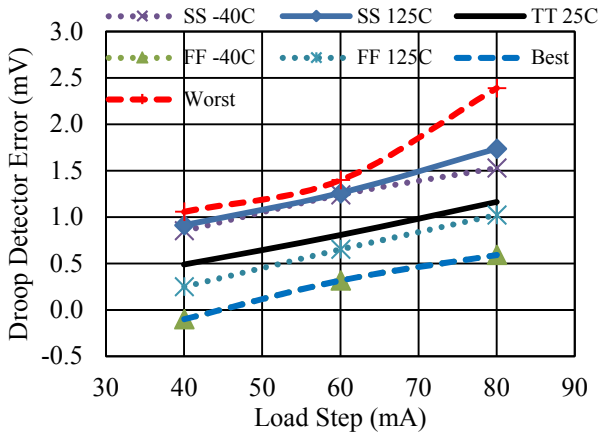

Figure 10: Droop detection error in millivolts.

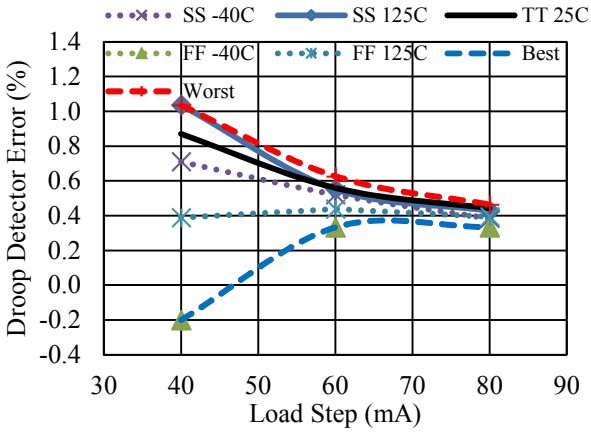

Figure 11: Droop detection error in percentage.

DLDO is enabled with 2 mA load current with only fine PMOS power devices to have a smooth startup into target 1.6 V. In the next step, the droop test is enabled and a rise time controlled load step is applied to the V_{OUT} node. Even though the droop is detected after a load step is applied, the DLDO is not disabled to show the recovery from transient load event. Then, the DLDO is disabled and test current is removed. In the next step, the buffer operation starts and the V_{OUT} node is buffered to V_{C1} or V_{C2} voltage. 2.5 µs is allocated for the output voltage settling. Once this step is complete, the ADC operation takes over and the digital code representing the minimum V_{OUT} voltage (V_{C1} or V_{C2}) can be read out from the ADC output.

One could think that precharging V_{OUT} to V_{DD} to reduce buffer settling time is a better design practice since V_{C1} or V_{C2} voltage is most likely closer to V_{DD} than it is to ground. However, making V_{OUT} equal to V_{DD} causes leakage which degrades the measurement accuracy. For this reason, V_{OUT} is discharged to ground before buffering at the expense of settling time as shown in Figure 8(a).

Measuring transient droop that covers a wide voltage range is essential to examine the effectiveness of the droop detector under different process and temperature corners. Hence, 40 mA, 60 mA and 80 mA load steps with the same rise time (100 ns) are applied to CUT at all process and temperature corners. Figure 9 shows the actual CUT droop

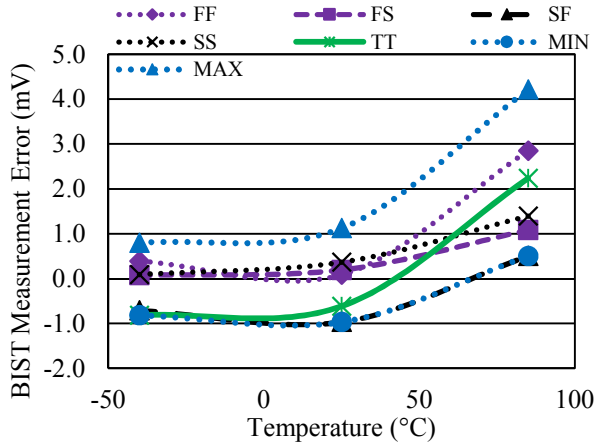

Figure 12: BIST measurement error (-40 °C to 85 °C).

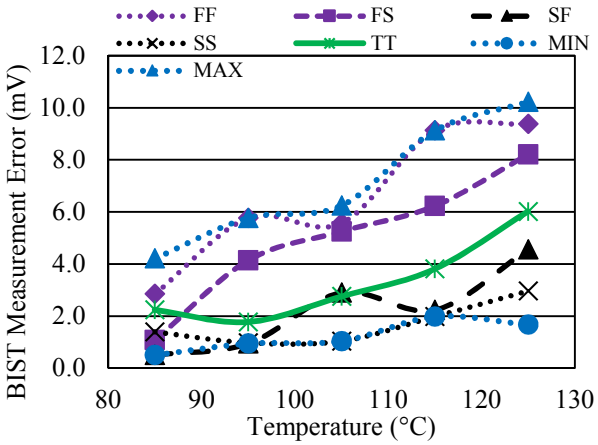

Figure 13: BIST measurement error (85 °C to 125 °C).

voltages at different load steps. The actual droop ranges from 45 mV to 520 mV under all different corners and applied load steps.

The droop detector error in millivolts is shown in Figure 10. The error of the droop detector is always between -0.1 mV and 2.39 mV where the actual droop voltages are between 45 mV and 520 mV. The error slightly shifts in the positive direction when the load step current is increased. As V_{OUT} reduces to lower voltages with high load current, the PMOS switches used in the S/H block become more resistive and results in higher sampling error at higher droop voltages. However, the error in percentage of this block reduces as the applied load step increases as shown in Figure 11. The sampling error in millivolts is fairly stable across different load steps, therefore increased droops yield lower percentage droop detection error. The maximum stored droop error is less than 1.05 %, which is adequate for the intended application.

A reuse based SAR ADC design is the final stage of BIST circuit architecture for the digital test output. Since the ADC uses the droop information stored on the droop detector as its input, any error on the droop detector affects the total error. Figure 12 shows the total BIST measurement error which is given as the difference between actual droop information and 10-bit test output corresponding to the droop. The total error of the whole BIST system is between -1 mV and 4.2 mV from -40 °C to 85 °C across all corners.

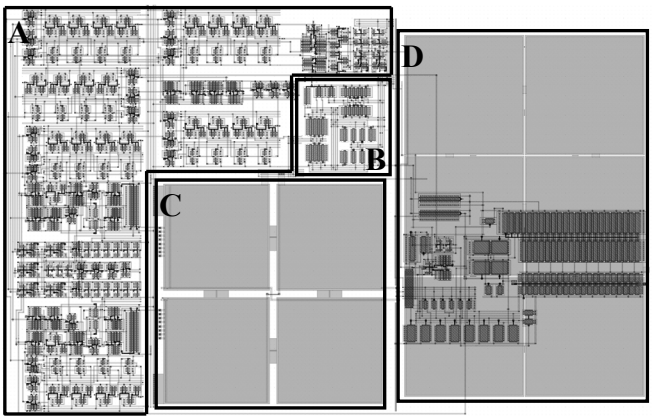

Figure 14: Droop detector and buffer layout. A:DDCL B: Comparator. C: S/H Capacitors. D: Buffer.

Table 1: Area of BIST blocks.

Block	Dimensions	Area
Droop Detector	100 µm × 104 µm	10400 µm^2
- DDCL	—	5956 µm^2
- Comparator	21 µm × 23 µm	483 µm^2
- S/H Capacitors	57 µm × 57 µm	3249 µm^2
Buffer	63 µm × 93 µm	5859 µm^2
TOTAL	166 µm × 104 µm	17264 µm^2

Table 2: Comparison table.

Paper	[12]	[13]	[14]	This Work
Circuit Objective	Power Supply Noise Peak Detection			DLDO Droop Meas.
Technology	180 nm	180 nm	45 nm	180 nm
V_{DD} (V)	1.8	—	1.2	1.8
Error (mV)	5% @ 1 GHz	<10 @ 100 MHz	<5	-1 to 4.2
Temperature Range (°C)	—	—	-40 to 100	-40 to 85
Area (µm^2)	—	—	—	17264*
Clock Requirement	No	No	No	Yes

(* Includes the droop detector and buffer area.)

Leakage currents on the system become dominant enough to affect the ADC accuracy beyond 85 °C due to the inherent connection of V_{OUT} to the DLDO power PMOS array and the disabled inverter array. Even though all process corners show a similar error trend as temperature increases, FF and FS corners cause the worst error, as expected. The error between the actual droop and test output can reach 10.2 mV at 125 °C as shown in Figure 13. However, the whole system works reliably from -40 °C to 85 °C. Employing a leakage cancellation circuitry can be helpful to increase measurement accuracy up to 125 °C, if necessary. The layout of the droop detector and the buffer block is shown in Figure 14. Area details are given in Table 1. The total area of the two main blocks is 17264 µm^2. According to the comparison between the works with similar objective given in Table 2, presented work has good accuracy.

5. Conclusion

A droop measurement BIST circuit suited for digital low-dropout regulators is proposed. Less than 1.05 % error is achieved in storing the droop information. The BIST measurement error is between -1 mV and 4.2 mV from -40 °C to 85 °C across all process corners. The proposed BIST system is suitable for go/no-go test during high volume manufacturing test and evaluating the DLDO quality as well. The droop detector can assist DLDO architectures in recovering from transient events, because it can monitor output direction cycle by cycle and signal when the maximum droop is reached with one clock cycle delay. Additionally, the BIST system can be used for other analog voltage measurements with minor modifications, such as DLDO reference voltage. Future research will focus on leakage cancellation of the described design.

6. References

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