Augmenting ESD and EOS Physical Analysis with Per Pin ESD and Leakage DFT

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Abstract

Based on technical and functional evaluation of high volume products returned from customers, Electrostatic Discharge (ESD) and Electrical Overstress (EOS) induced damages are the two significant causes of customer return in recent times. These customer returns are expected to rise as silicon scales down, as devices are becoming more susceptible to EOS. With ESD diodes ubiquitously being used as the protection device for IC Input/Output (I/O) pin, there is a lack of on-die test structures to validate these circuits automatically. Concerned by zero defect targets and high EOS failure rate from customers, there is an increasing need to define new test methods and techniques that are able to reproduce EOS failure, improve IC robustness against EOS events and isolate EOS and ESD failures. This paper proposes Design for Test (DFT) techniques that can be used to augment physical analysis used to screen EOS and ESD failures.

Keywords

ESD, EOS, Leakage, Diode, Charge pump, DFT

1. Introduction

Zero defect program based mostly on automotive, health, aerospace and military markets push the electronic industry to spend millions of dollars to increase product quality and reliability performances and consequently reduce Part Per Million (PPM) rates coming from customer complaints. According to the Industry Council on ESD Target Levels, damage signatures from EOS are the leading reported cause of returns in integrated circuits and systems that have failed during operation [1]. As per electronic IC supplier, the most common issues related to these customer returns are ESD classified failures caused by human body [2], machine or tool discharge events and also standalone charged IC discharge events that may occur during IC manufacturing phases and in electronic board assembly lines. Solutions to this problem are hindered by a prevailing misconception in the electronics industry that insufficient robustness to ESD is a primary cause of EOS.

It is difficult to make a clear distinction between EOS and ESD failures based on the electrical failure modes and signatures. There are many physical analysis [3] approaches that have been studied that can lead to accurate root cause identification. In addition, the reduction in lifetime with ESD and EOS damage will need new methods to screen for latent damage.

In this paper, we present DFT methods that can be categorized into ESD test technique and "no touch leakage" measurement technique. These techniques can augment the physical analysis and can provide a better insight into the failure mechanisms and assist in production test defect screening. Such techniques can provide valuable inputs to the designer in improving the ESD protection as well as in making the correct layout for specific devices. Only by gathering as much information as possible and comprehending them holistically can a sound conclusion on whether the failure cause is EOS or ESD related be reached. In Sections 3 and 4 of this paper, we address ESD Diode DFT technique and in Section 5 we address multiple Pad Leakage DFT techniques.

2. Background

I/O pins on any chip are susceptible to electro-static charging events during manufacturing process or by human contact. This may lead to charge build up on device gates which can cause electrical breakdown of the device gate. Specially designed diode protection circuits are needed to provide a low resistance discharge path from I/O pad to ground or power supply so that underlying IO is not impacted. Testing of these ESD diode structures are carried out by externally applied stress on IO pad. There is no known on-die test structure today which can automatically check the pins in production manufacturing environment. Figure 1 shows a typical CMOS I/O buffer with ESD diode protection circuit.

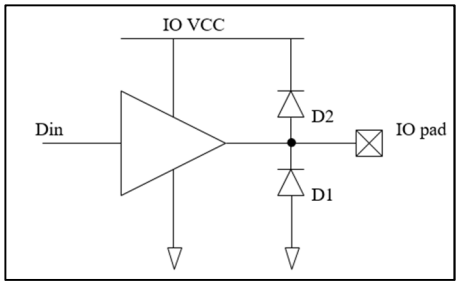

Figure 1: ESD Protection Diode for a Typical CMOS Output Buffer

Main obstacle to designing on-die test structure is the need for additional power supplies. By the very nature, ESD diodes do not get activated when pad voltage is within supply range. So a supply above "I/O power supply" and lower than I/O ground supply is needed to check on the structural integrity of these diodes, which is costly in terms of silicon area and associated test platform cost. In the next section, we present a test circuit technique which works with existing power supplies and with little area overhead.

3. Per Pin ESD DFT Operating Principle

The per-pin ESD DFT test operates in two test modes - one for checking ESD protection diode tied between pad and ground (referred to as D1 diode in Figure 1) and another for checking protection diode between pad and I/O power supply (referred to as D2 diode). Figure 2 shows the schematic view of ESD diode test circuit. When D1 test mode is enabled (EnD1test is set High), I/O pad voltage is driven to a negative

voltage below ground using a charge pump circuit, which uses a charging capacitor (C_{PD1}) and a test clock (CLK). With each clock transition, charging capacitor pumps incremental charge to the load capacitor. Load capacitor (C_L) is simply the I/O pad capacitance. C_{PD1} capacitor is chosen to be a much smaller size than C_L to keep the area smaller. Number of cycles needed to charge C_L will be dependent on the size of C_{PD1} and the test clock frequency.

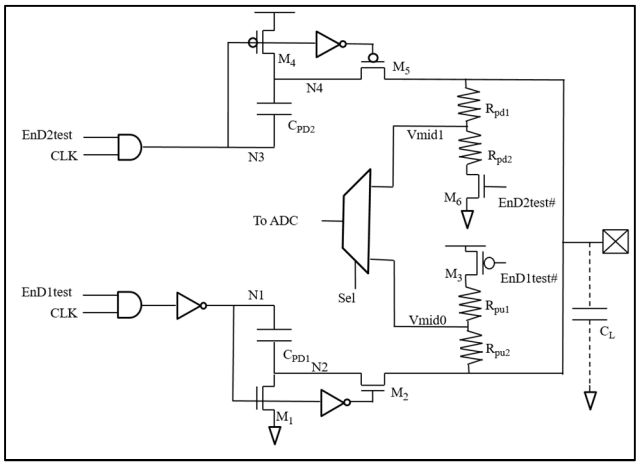

Figure 2: Schematic View of ESD Diode Test Circuit

During D1 test mode, when CLK phase is low, charging capacitor C_{PD1} will be charged to +VCC (N1 to +VCC and N2 to ground through enabled M_1 pulldown device). On the rising edge of the CLK, N2 will transition to minus VCC and during high phase of CLK, M_1 pulldown device will be off and M_2 pass gate switch will turn on discharging the load capacitance. Thus in every clock cycle, I/O pad capacitance will slowly decrease and eventually be pushed towards minus VCC. Figure 3 shows the equivalent circuit during D1 test mode. If after N cycles I/O pad is at V_N voltage, then after the N+1 cycle, the pad voltage V_{N+1} will be determined by the following charge sharing equation:

$$V_{N+1} = \{(C_{PD1} * (-VCC) + C_L * V_N)\} / (C_{PD1} + C_L)$$

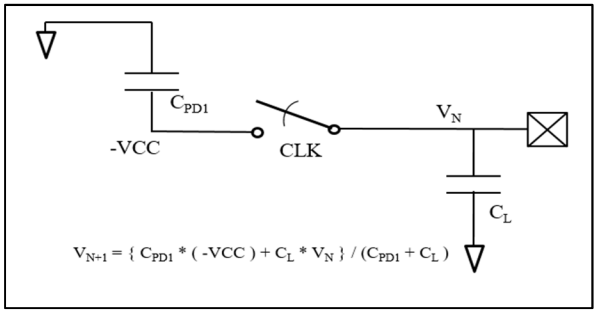

Figure 3: Charging Capacitor Equivalent Circuit

In the presence of robust ESD diode between pad and ground, the negative voltage on the pad will forward bias D1 diode and all the charging current will be shunted through it. This will limit pad voltage to be close to the forward bias voltage (Vfb) of the protection diode. However, any structural or physical integrity issue on the diode, such as hard and soft open or short, sets the pad voltage away from the Vfb. Pad voltage is then level shifted to the nominal signal voltage range between 0 and VCC through pull up resistors R_{pu1} and R_{pu2} to facilitate final voltage detection. Since the range of possible pad voltage is between minus VCC to 0V, the values of R_{pu1} and R_{pu2} can be chosen accordingly so that the level shifted output, Vmid0, falls in the normal signal range of 0 to VCC for all cases. Vmid0 signal can then be passed to a shared ADC circuit for further digital processing, so that the integrity of ESD diode and its connection to ground rail could be assessed. D2 diode testing is done in a similar fashion. During D2 test mode, charge pump circuit pulls the pad towards 2*VCC with every clock cycle. When CLK phase is low, charging capacitor C_{PD2} is charged to VCC (N3 is 0V and N4 is set to VCC through enabled M_4 pullup device). Rising edge of CLK forces node N4 to 2*VCC and during high phase of CLK, M_4 is turned off and M_5 is turned on, thus incrementally charging the pad to a higher voltage, according to following equation:

$$V_{N+1} = \{(C_{PD2} * (2*VCC) + C_L * V_N)\} / (C_{PD2} + C_L)$$

In presence of ESD diode, pad voltage will be limited to VCC+Vfb. Pad voltage is then level shifted back to a voltage level between 0 and VCC range using pull down resistor stack. The level shifter output, Vmid1 signal, is then selected by 2:1 mux and passed to ADC.

4. Per Pin ESD DFT Results and Discussion

Figure 4 shows the expected behavior of ESD diode DFT circuit in three cases; A) ESD diodes are operating within normal range, B) ESD diodes or accompanying I/O has been damaged and are excessively leaky and C) ESD diodes are not present or are completely damaged.

In case A, charge pump will drive the pad voltage to minus Vfb or VCC+Vfb depending on D1 or D2 test mode respectively. During case B, current pumped during a test clock cycle will not be able to overcome the excessive leakage through ESD diode and pad voltage will be stuck to the ground in D1 test mode or stuck to power supply in D2 test mode. In case C scenario, charge pump will push the pad to minus VCC or 2*VCC.

Due to process variation and accompanying I/O leakage variation, Vfb will modulate around a mean value for all healthy ESD diodes on the chip, shown as shaded region in Figure 4. These range of Vfb values will be translated to a specific range of values at ADC output. Post silicon characterization defines a clear band for expected ADC output values corresponding to the combination of ESD diodes and accompanying I/O buffer. Any value outside of this range is a suspect for anomaly due to excess leakage or ESD depending on whether it is below or above the expected range. For healthy ESD diode, pad voltage will only go one diode drop above the supply or below the ground. This voltage stress will only be there for a few test clock cycles, depending on ADC speed and test clock frequency, while we are testing these diodes. For bad ESD diode cases, voltage can go up to 2*VCC but in these cases, part has already been compromised.

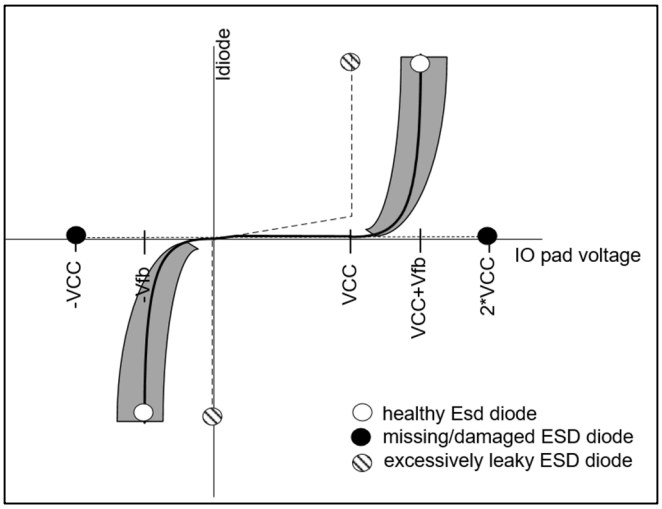

Figure 4: IO Pin Voltages during Per Pin ESD Testing

The Per Pin ESD DFT technique can screen for ESD Diode connectivity and also potential excess of leakage. This technique cannot quantify the amount of pad leakage or ESD compliance. Other methods are needed to identify the pad leakage on I/O's and assess compliance requirement. Section 5 describes three pad leakage testing methods.

5. Pad Leakage DFT

The existence of latent ESD failures in CMOS integrated circuits has been addressed by several studies and Design of Experiments and it continues to be a controversial subject [4][5]. A latent failure is defined as a time-dependent failure that occurs under certain use condition as a result of an earlier exposure to ESD or EOS that does not result in an immediate detectable failure.

These latent defects are sometimes called "walking wounded" devices. The risk of walking wounded product is becoming more prevalent with shrinking technology. Integrated circuits exposed to ESD damage have experienced increased leakage currents while still maintaining complete functionality. The relationship between the leakage current level and latent failure depends on the nature and magnitude of the ESD damage. In order to screen these walking wounded devices, leakage test during production test, system level test as well as board level test at OEM test sites have been effective methods.

The two primary types of latent ESD damage are trapped charge in the gate and drain to substrate junction damage. Pad leakage current increase is due to the latter. Since the input protection circuitry consists of diodes, typically the ESD damage is located in the input protection diode rather than the actual input transistors.

As shown in Figure 5, traditional leakage tests are performed by connecting each pin under test to a functional tester channel, while performing a DC measurement using per-pin PMU (Parametric Measurement Unit). The first step is to pre-condition each pin to tri-state. Then, all pins are forced to one of the supply rails and the current sourcing from or sinking to each pad is measured. If the current through any of the pads exceeds the specification, the corresponding pad is declared as leaky.

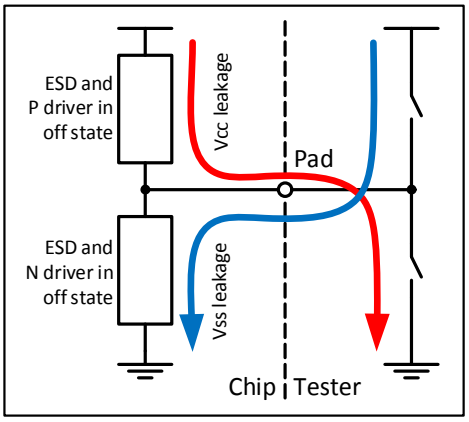

Figure 5: Connected Pad Leakage Test

Pad connectivity to tester channels is becoming increasingly problematic for high speed I/O's, hence there is a need for a no-touch test method for all DC parametric tests including leakage. There are three DFT-based methods that have been used for No Touch Leakage (NTL) test: DC bias, RC decay and Indirect Connect DC Test (ICDCT) to save on tooling costs associated with package pin exceeding the available module channel for direct touch testing or the need for relays.

In DC bias method [6], as shown on Figure 6, a current is applied to the pad through a resistor with a known value to pull-up or pull down the pad, while the drivers are tri-stated. The leaker resistors are implemented as very small PMOS and NMOS devices. The pad voltage, which is proportional to the leakage current through the selected leaker, is compared to a pre-defined Vref through a comparator. The output of the comparator is sampled after a few clock cycles and is used as the test response.

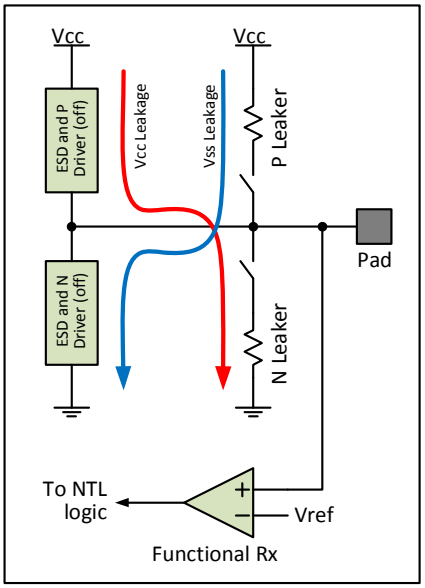

Figure 6: DC Bias Pad Leakage DFT

In RC decay method [7], as shown in Figure 7, the leakage is tested by measuring the charge/discharge time constant of the pad. First the pad is pre-charged to Vcc or Vss. Then it is tri-stated and the parasitic capacitance on the pad discharges

through the resistance (leakage) of the driver or ESD under test. A high leakage (low resistance) on the pad discharges and changes state much faster than a low leakage (high resistance) on the pad. As in the DC Bias technique, the functional receiver is re-used as a comparator to sample the pad voltage at a certain pre-determined time. The difference here is that it must be sampled at a specific time when the pad is expected to be still close to the start value if the leakage is within specification.

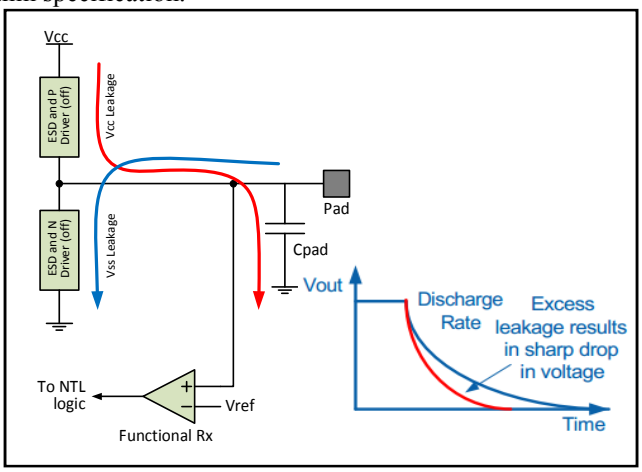

Figure 7: RC Decay Pad Leakage DFT

In ICDCT method, as shown in Figure 8, tester forces the voltage through a high precision resistor on the controllability pin and senses the voltage back at the observability pin. The difference between source and sense voltages with respect to a known resistance is translated into leakage current.

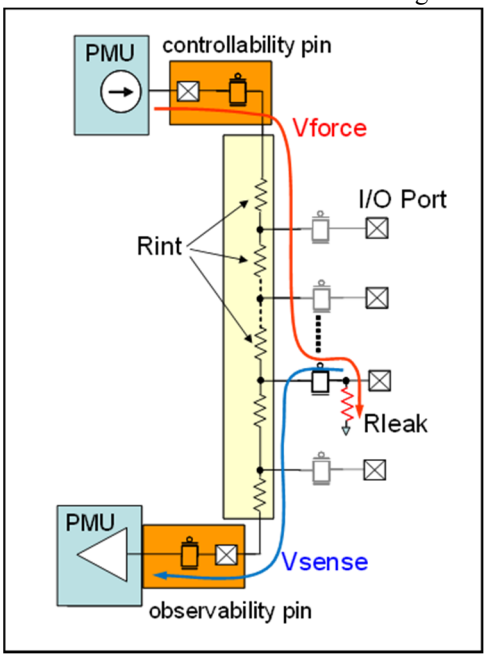

Figure 8: ICDCT Pad Leakage DFT

Table 1 shows a comparison of the various NTL DFT methods implemented in high volume products. DC Bias DFT depends on the absolute value of the impedance of small devices, making it quite unfriendly to PVT variations. The other two methods are preferable in most cases. RC decay NTL has good potential for accuracy, but requires substantial DFT logic and careful design. ICDCT provides the best accuracy but cannot always be implemented due to possible constraints with availability of analog test pins. Also, in some cases its distributed nature imposes a challenge in I/O floorplan. For this reason, ICDCT is preferable for small low pin count interfaces, such as PCIe.

Table 1: Comparison of NTL Methods

DFT Method	Pros	Cons
DC bias	• On die solution • Results in terms of voltage • No need for high-speed clock • Modular implementation	• Moderate PVT robustness and Accuracy • Sensitivity to comparator accuracy
RC decay	• On die solution • Results in terms of charge/discharge time • Modular implementation	• Moderate PVT robustness and Accuracy • Sensitivity to comparator accuracy • Accuracy depends on a high-speed clock
ICDCT	• Mostly PVT insensitive • High accuracy • Low circuit and logic overhead	• Sensitive to control vs observe routing mismatch • Added leakage due to mux/pass gate/drivers • Requires dedicated control & observe pins • Distributed implementation with global routing • Requires an ADC to make it a BIST

6. Conclusion

Only by gathering as much information as possible and comprehending them holistically, can a sound conclusion on the real failure cause of EOS/ESD damage of IC circuits be reached. The DFT methods presented in this paper augment needed Physical Analysis to reveal the true identity of their source.

The on-die "Per pin ESD DFT circuit" provides a mechanism to automatically test the integrity of each ESD diode on the chip in production manufacturing. In the case of failing pins, circuit also provides initial insight on the nature of ESD diode failure which helps in directing the further failure analysis work.

EOS/ESD can cause noticeable increases in pad leakage current while maintaining full functionality. This increased

leakage current can be an indication of latent damage. No Touch Leakage DFT offers the possibility for a simple screening procedure for these latent defects. Depending on IO circuit type and needed resolution, NTL DFT choice can be evaluated based on the work presented here.

7. References

[1] Industry Council on ESD Target, White Paper 4 “Understanding Electrical Overstress – EOS Industry Council on ESD Target Levels”, Aug 2016.

[2] JEDEC standard. Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM). JESD22-A114, 2007.

[3] Tung Chih Hang, Cheng Cheng Kou, M.K. Radhakrishnan, Natarajan M Iyer “Physical Failure Analysis to Distinguish EOS and ESD Failures” Proceedings of IPFA 2002, Singapore, pp 65-69.

[4] W. D. Greason, Z. Kucerovsky, and W. K. Chum, "Latent Effects Due to ESD in CMOS Integrated Circuits: Review and Experiments," IEEE Trans. on Industry Applications, vol. 29, p. 88, 1993.

[5] W. D. Greason and K. W. K. Chum, "Characterization of Charge Accumulation and Detrapping Process Related to Latent Failure in CMOS Integrated Circuits," IEEE Trans. on Industry Applications, vol. 30, p. 350, 1994.

[6] Anne Meixner, Akira Kakizawa, Benoit Provost, Serge Bedwani, “External Loopback Testing Experiences with High Speed Serial Interfaces”, 2008 IEEE International Test Conference.

[7] T.R. Arabi et al., “A JTAG based AC leakage self-test”, Symposium on VLSI Circuits, pp. 205-206, June 2001.