A Bi-Memristor Synapse with Spike-Timing-Dependent Plasticity for On-Chip Learning in Memristive Neuromorphic Systems

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Abstract

Memristors are nanoscale devices that have recently been proposed for use as a synapse in brain-inspired computing systems. In this paper, we present a synapse architecture that utilizes two memristors to implement a non-volatile synaptic weight that can be configured as both positive and negative. The weight of the proposed synapse has an inherent exponential-like dependence on the change in the memristance of the devices, a property that we have capitalized to implement spike-timing-dependent plasticity (STDP) for on-chip learning in spiking neural networks. We discretize the neuron's spike in time and voltage and show that learning rate can be controlled by the clock frequency used. We show that by modulating the duty cycle of the clock, we can alleviate the detrimental effects of switching rate mismatch in the devices. We also simulated a 3 × 3 crossbar structure and presented the weight updates observed therein, hence demonstrating the feasibility of a crossbar with our synapse. We evaluated the energy consumption per spike of our approach and compared it with those in literature.

Keywords

Memristor, Synapse, On-chip learning, Spike-Timing-Dependent Plasticity

1. Introduction

Biological neural networks possess high parallel processing power owing to the massive interconnectivity of their neurons [1] that is in stark contrast with the sequential information processing in traditional von Neumann machines. Neuromorphic systems are a computing paradigm that draw inspiration from biological nervous systems. They consist of an ensemble of very large scale integration (VLSI) circuits that mimic the dynamics of information processing in biological neural networks.

Silicon neurons are analog and/or digital circuits that emulate the behavior of biological neurons. A review of these implementations can be found in [2]. Synapses are circuits that provide the "weighted" interlink between neurons and have been implemented using resistors, capacitors and floating gates. However, as outlined in [3], these implementations fail to provide the desired characteristics of a non-volatile synaptic weight that can be programmed precisely and is amenable for on-chip learning. Recently, a nanoscale device known as the "memristor" has been shown to be suitable as a synapse in neuromorphic systems [4, 5].

Memristors are two terminal devices first theorized by Leon O. Chua in 1971 [6] as the missing fourth fundamental circuit element. In 2008, HP Labs demonstrated memristance property in a passive two terminal nanoscale device [7]. Memristors are nanoscale devices whose resistance can be tuned by controlling the voltage flux flowing into it, hence making them suitable for use as synapses, whose weight in this case is represented by the conductance of the memristor. Moreover, by adjusting the flux levels, their conductance can be modulated to implement spike-timing-dependent plasticity (STDP), a synaptic learning mechanism that has been shown to exist in biological systems [8]. Additionally, their non-volatility and nanoscale feature size enables a crossbar implementation, thus providing a high density in addition to the (desirable) high connectivity between the neurons [9]. The next section summarizes some of the existing approaches to the use of memristor as a synapse and the techniques employed for their learning.

2. Related Work

In [4] the memristor was presented as a synapse connecting a pre- and a post-neuron. Using time division multiplexing, pulses were generated in the neurons to perform long term potentiation (LTP) and long term depression (LTD). However, this implementation needs an overhead circuit for width modulated pulses' generation and a communication between the pre- and post-neurons to keep track of each other's firing events. Authors in [5] have exponentially modulated the width of the pulse applied to the memristor for STDP. This technique also has the same issues as outlined above. In [10] and [11], authors have implemented STDP with a multi-voltage level waveform and a capacitive discharge based waveform, respectively. All of these techniques can only realize an excitatory (positive weight) synapse and have not implemented an inhibitory synapse (negative weight).

In [9], the authors have achieved STDP for a memristor-based synapse by meticulously shaping the neuron's spike waveform. However, excitatory and inhibitory synapses here are differentiated by the firing spike shape, which is a neuron artifact, something that is not inherent in the synapse itself. A similar idea was proposed in [12], wherein configuration bits in the neuron determine the sign (positive/negative) of the incoming current and thereby, the sign of the synaptic weight.

Authors in [3, 13] have presented a memristor based bridge shaped synapse capable of implementing both positive and negative synaptic weights. However, the focus here was not on STDP. In addition, it required a differential amplifier to convert the weighted voltage at the synapse into a current, for summation at the neuron. A dual crossbar configuration was presented in [14] to implement positive and negative weights. However, this scheme uses a dedicated summing amplifier at each column of the crossbar and no neuron spiking based STDP was shown therein.

Authors in [15] have presented a twin-memristor synapse and have presented on-chip learning techniques for it. However, this method has the drawback of having a feedback from the post-neuron to the pre-neuron and a dedicated CMOS circuit was used for learning phase, thus overriding the density advantage associated with using memristors.

Overcoming the issues persisting in the existing synapses in literature, we propose a bi-memristor synapse structure in conjunction with a discretized neuron spike to achieve STDP for on-chip learning in spiking neural networks. The key contributions of this paper are as follows:

1) The proposed bi-memristor configuration can realize both positive and negative weights by virtue of the relative conductance of the memristors.

2) The proposed synapse's effective conductance has an intrinsic exponential-like dependence on the memristance change of each device, thus making it suitable for STDP.

3) We show that by using neuron spikes that are discretized in voltage and time, the STDP behavior can be carefully controlled. The clock frequency used here directly affects the steepness of STDP based learning.

4) We show that by changing the clock's duty cycle, we can remedy the effects of switching rate mismatch in the devices.

3. Memristor Model

The memristor model used in this work is an empirical model developed in [16] and fitted against experimental data extracted from HfOx devices manufactured in-house at SUNY Polytechnic Institute [17]. This model captures the three main characteristics experimentally observed in transition metal oxide memristors, which are: (1) the existence of a threshold below which the change in the resistance is negligible. (2) A nonlinear dependence between the applied voltage and the change in the resistance. (3) Plateauing of the resistance as it approaches either high resistance state (HRS) or low resistance state (LRS). Equations (1) and (2) describe the model:

$$\frac{dM}{dt} = \begin{cases} -C_{LRS}\left(\dfrac{V(t)-V_{tp}}{V_{tp}}\right)^{P_{LRS}} f_{LRS}(M(t)), & V(t) > V_{tp} \\ C_{HRS}\left(\dfrac{V(t)-V_{tn}}{V_{tn}}\right)^{P_{HRS}} f_{HRS}(M(t)), & V(t) < V_{tn} \\ 0, & otherwise \end{cases} \quad (1)$$

Where C is a fitting coefficient, V_{tp} and V_{tn} are the positive and negative thresholds, respectively, and P_{LRS} and P_{HRS} are control parameters that govern the nonlinearity of the model. $f_{LRS}(M(t))$ and $f_{HRS}(M(t))$ are window functions that capture the resistance plateauing near the boundaries and can be described as follows:

$$f((M(t)) = \begin{cases} \dfrac{1}{1+\dfrac{\theta_{LRS}LRS - M(t)}{\beta_{LRS}(HRS-LRS)}}, & V(t) > V_{tp} \\ \dfrac{1}{1+\dfrac{M(t)-\theta_{HRS}HRS}{\beta_{HRS}(HRS-LRS)}}, & V(t) < V_{tn} \end{cases} \quad (2)$$

Where β and θ are two fitting parameters. Fig. 1 depicts the I-V sweeps for both the experimental data and the model used.

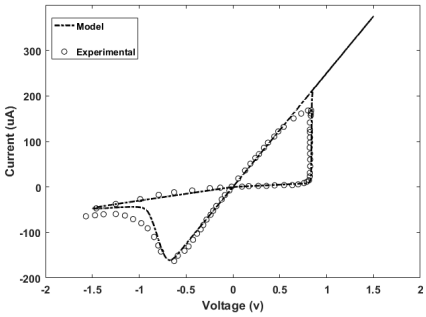

Figure 1: I-V plots for the model used here versus experimental data.

4. The Bi-Memristor Synapse

The proposed bi-memristor synapse consists of two memristors connected between a pre-neuron and a post-neuron as shown in Fig. 2(a). When the pre-neuron fires, switches S1 and S2 close, thus biasing the nodes 1 and 2 with the neuron's firing spikes, but with opposite polarity. During the accumulation phase in the post-neuron, switches S3 and S4 are open, while S5 and S6 are closed, providing the connection between the neurons as shown in Fig. 2(b). During this phase, the net current flowing into the neuron is

$$i = i_{M_p} - i_{M_n} = (G_p - G_n)\, V_{spike} \quad (3)$$

Hence, the weight of the synapse, which is proportional to its effective conductivity, is given by

$$G_{eff} = G_p - G_n = \frac{1}{M_p} - \frac{1}{M_n} \quad (4)$$

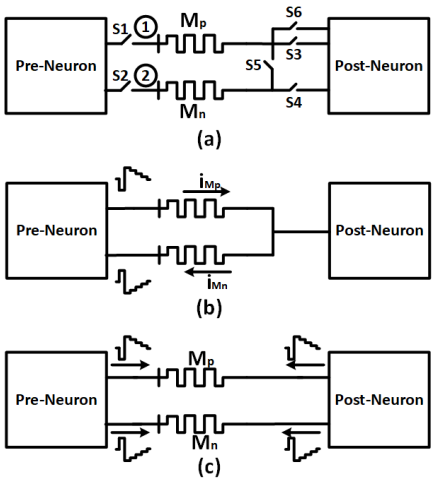

Figure 2: (a) The proposed bi-memristor synapse providing the connection between the pre- and post-neuron (b) The synaptic connection while the post-neuron is accumulating (c) The synaptic connection when the post-neuron fires.

When the membrane voltage (V_{mem}) in the post-neuron exceeds its threshold, the neuron fires, thereby entering a phase known as its refractory period, wherein any incoming current does not affect V_{mem}. During this phase, switches S5 and S6 open, while S3 and S4 close, thus disconnecting the two memristors at the post-neuron's end. The post-neuron provides feedback spikes during this phase as shown in Fig. 2(c). The relative timing of the occurrence of these spiking events determines the net voltage applied across the memristors, as depicted in Fig. 3. The closer they occur in

time, the higher the voltage difference across the memristors and hence a larger memristance change ΔM.

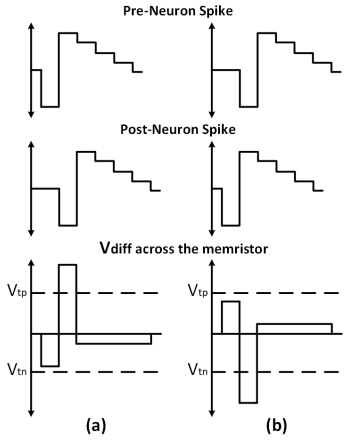

Figure 3: (a) The pre-neuron spiking before the post-neuron, leading to LTP (b) The pre-neuron spiking after the post-neuron, leading to LTD.

It may be noted from Fig. 2(c) that the potential difference across the devices is of opposite polarity during an LTP/LTD event while the devices themselves are physically aligned with the same polarity. This implies that the change in memristance will be in opposite directions for them. Hence, for the case of an LTP event, the new effective conductance, G'_{eff} is given by:

$$G'_{eff} = \frac{1}{M_p - \Delta M} - \frac{1}{M_n + \Delta M}$$
$$= \frac{1}{M_p\left(1 - \frac{\Delta M}{M_p}\right)} - \frac{1}{M_n\left(1 + \frac{\Delta M}{M_n}\right)}$$
$$= \frac{1}{M_p} - \frac{1}{M_n} + \Delta M\left(\frac{1}{M_p^2} + \frac{1}{M_n^2}\right) + \Delta M^2\left(\frac{1}{M_p^3} - \frac{1}{M_n^3}\right)\ldots$$
$$= G_{eff} + \Delta M\left(G_p^2 + G_n^2\right) + \Delta M^2\left(G_p^3 - G_n^3\right)\ldots$$

Hence, the change in the conductance after an LTP event is given by $G'_{eff} - G_{eff}$ as:

$$\Delta G = \Delta M\left(G_p^2 + G_n^2\right) + \Delta M^2\left(G_p^3 - G_n^3\right)\ldots \qquad (5)$$

Similarly, for an LTD event, the change in conductance is given by:

$$\Delta G = -\left[\Delta M\left(G_p^2 + G_n^2\right) - \Delta M^2\left(G_p^3 - G_n^3\right)..\right] \qquad (6)$$

Therefore, the weight change function for the bi-memristor synapse resembles the series expansion of the exponential function, wherein the variable is ΔM. As described in Section 3, the change in the memristance ΔM for our model is a polynomial function of the voltage applied across the device, which can be represented in a simplified format as $\Delta M = kV^p$, where k is a constant determined by the memristor's model parameters. Hence, (5) can be written as:

$$\Delta G = k_1 V^p + k_2 V^{2p} + k_3 V^{3p} + \cdots \qquad (7)$$

Equation (7) implies that ΔG has an exponential-like dependence on V. Hence, by varying V linearly with the time difference Δt $(= t_{post} - t_{pre})$ between the spiking events of the neurons, ΔG can be made to be exponentially dependent on Δt, which is the requirement of exponential STDP [9]. The following section describes the neuron circuit that we have designed for use with this synapse.

5. Spiking Neuron Circuit

Fig. 4 shows the block diagram of the neuron circuit we have designed for use with our bi-memristor synapse. It operates in two modes, namely, accumulation and refractory (firing) period. During the accumulation mode, switches S3 and S4 are open while S5 and S6 are closed. This provides a current summing node at the input to the integrator Op Amp, wherein currents from both the memristors are summed and charge is accrued on the node mem giving it a potential V_{mem}. V_{mem} is compared with a threshold (reference) voltage V_{th} using a comparator. When V_{mem} surpasses V_{th}, the comparator output triggers the spike generator circuit, apart from closing S3 and S4 and opening S5 and S6. This leads to the disconnection of both the memristors, thus allowing the propagation of feedback spikes of opposite polarity to the memristors in the synapse preceding the neuron.

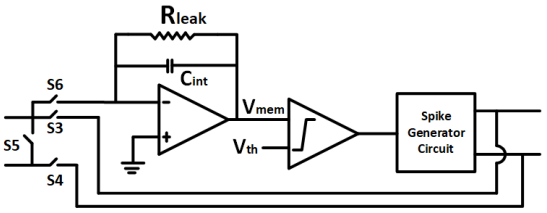

Figure 4: The leaky integrate and fire neuron along with the spike generator circuit.

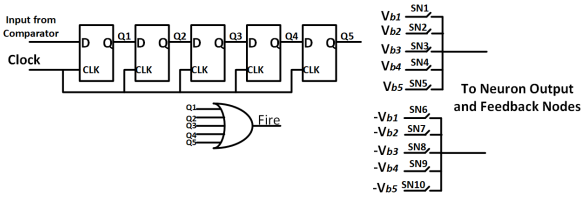

Figure 5: Spike generator circuit that produces the discretized-voltage spike.

The spike generator circuit is shown in Fig. 5. It consists of five flip-flops that are controlled by a global clock. The first flip-flop captures the spike trigger from the output of the comparator. The latched pulse then propagates through the rest of the flip-flops at each rising clock edge. The output of each flip-flop is used to close switches that provide a certain voltage level as the feedback to the memristors in the preceding synapse and as the neuron's spike to the succeeding synapse. The action of each flip-flop output on the switches and the voltage bias provided on the spike is given below in Table 1. Note that these biases are linearly graded, and can be generated by voltage division from the supply rails.

Table 1: The effect of the flip-flop outputs on the switches activated and the corresponding outputs provided on each output/feedback node of the neuron.

Flip-Flop Output	Switch Action	Output Voltage
Q1	SN1, SN6	Vb1, -Vb1
Q2	SN2, SN7	Vb2, -Vb2
Q3	SN3, SN8	Vb3, -Vb3
Q4	SN4, SN9	Vb4, -Vb4
Q5	SN5, SN10	Vb5, -Vb5

6. Learning Behavior of the Proposed Synapse

To characterize the learning behavior of the proposed bi-memristor synapse, we have performed simulations in Cadence's Virtuoso environment using Spectre as the simulator. The CMOS circuits in the neuron were built using IBM's 65nm process design kit and the memristor model was written in Verilog-A with the key parameters set as: $P_{LRS} = P_{HRS} = 3$, $LRS = 5K\Omega$, $HRS = 50K\Omega$, $t_{swp} = t_{swn} = 1\mu s$, $V_{tp} = 750mV$, $V_{tn} = -750mV$ [17].

In order to simulate the synapse, the setup shown in Fig. 6 has been used. Here, the synapse S2 is setup with a high positive weight such that when the neuron N2 is artificially triggered, the accumulation is enough for the neuron N3 to fire, thus fixing its temporal occurrence. Then, the timing of the spike of neuron N1 is adjusted to obtain various cases of learning for S1. Fig. 7 shows the STDP behavior of the synapse. It is seen that this graph bears a close resemblance to the STDP in biological systems proposed in [8].

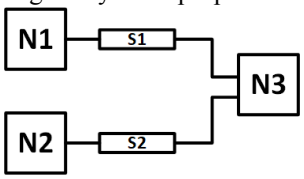

Figure 6: The synapse-neuron setup for characterizing the proposed synapse through simulations.

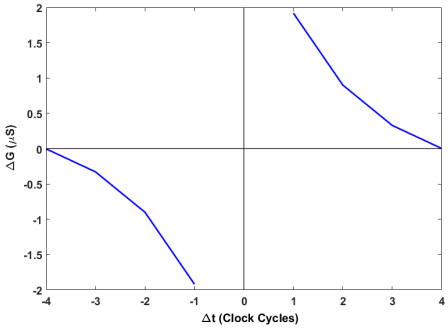

Figure 7: Simulated STDP behavior of the proposed synapse.

The simulations shown in Fig. 7 were performed for a synapse weight of 0, which implies $M_p = M_n$. From (5) and (6), it can be noted that the magnitude of weight change is a function of the current weight (the coefficients depend on G_p and G_n) of the synapse implying that our synapse implements multiplicative STDP [9]. For our synapse, as the weight becomes more positive, M_p decreases whereas M_n increases. From (5), it can be predicted that ΔG increases with weight (W) for LTP with a given ΔM. Also, (6) predicts that the magnitude of ΔG increases with weight (W) for LTD as well. This behavior has been simulated and plotted in Fig. 8.

A direct consequence of the clocked nature of our neuron's spike is the control that can be achieved over the weight updates for STDP. As the clock's time period increases, the pre- and post-neuron's spikes overlap for a longer period, resulting in a larger ΔM. From (5) and (6), it is observed that as ΔM increases, higher order terms in the series expansion become significant, resulting in a steeper STDP curve as illustrated in the simulation results shown in Fig. 9. Conversely, it can also be seen that as the clock frequency increases, the STDP behavior becomes linear. This can also be deduced from (5) and (6). As ΔM becomes smaller, higher order terms' significance reduces, and the expression can be approximated as $\Delta G = \left(G_p^2 + G_n^2\right) \Delta M = k\, \Delta M$. This behavior is evident from the simulations shown in Fig. 9.

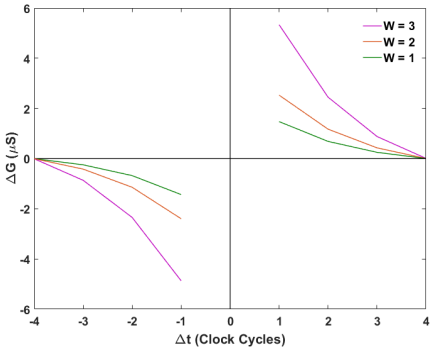

Figure 8: STDP dependence on the current weight of the synapse.

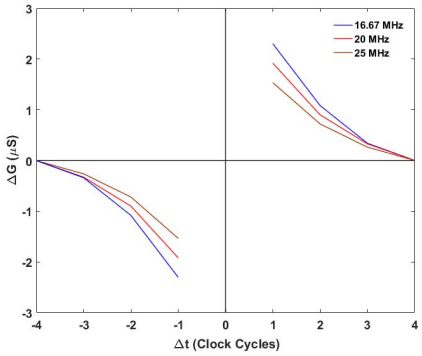

Figure 9: STDP dependence on the clock frequency for the proposed synapse.

7. Memristor Switching Rate Mismatch

The proposed bi-memristor synapse utilizes the switching of the memristors in the direction of increase as well as decrease. Both of these effects contribute to the change in the synapse's weight. However, due to the fundamentally distinct nature of resistive switching in either direction in memristors, their switching rates can vary up to two orders of magnitude [17, 18, 19]. This results in the drastic change in conductance of one of the memristors, as it reaches its extreme resistance without attaining any intermediate values. Thus, the synaptic weight change in this case will not be a strong function of Δt since one of the memristor switches drastically irrespective of the flux applied across it, hence dominating the contribution for weight change. This is evident from the simulations we performed on our synapse (Fig. 10) with the switching time parameters set as $t_{swp} = 10ns, t_{swn} = 1\mu s$. It can be observed that the STDP behavior in this case is crippled.

In order to remedy the effect of switching rate mismatch, we propose to use a duty cycle modulated clock in the neuron. This duty cycle modulation is achieved by using the current starved programmable delay circuit from [20], wherein a reference voltage determines the duty cycle of the output clock signal. This duty cycle modulated clock is logically ANDed with the control signals from the flip-flops that control the switches SN1-10 in Fig. 5. Hence, by reducing the

time for which the feedback signal is provided by the post-neuron, we reduce the effective flux supplied to the memristors, which helps reduce the drastic change of memristance and hence brings the STDP behavior closer to the one observed with matched switching rates.

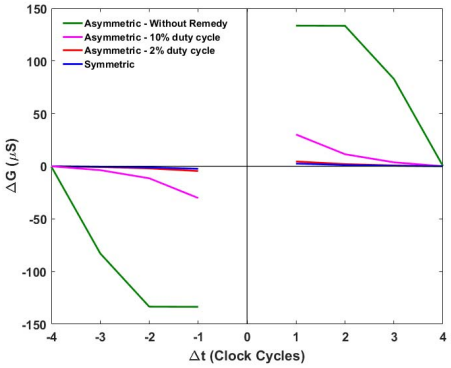

Figure 10: STDP behavior of the proposed synapse with asymmetric switching rates in the memristors. It is seen that as the duty cycle of the clock reduces, the STDP curve is closer to the ideal case of symmetric switching rates.

8. A 3 × 3 Crossbar Based on the Proposed Synapse

In order to test and demonstrate the feasibility of our proposed synapse design for use in a crossbar based neuromorphic approach, we built a 3 × 3 crossbar with our synapse and neuron as shown in Fig. 11. Here, the neurons N1-N3 are the input neurons, while N4-N6 are the output neurons. We use the convention $S_{i,j}$ to denote the synapse connecting the input neuron N_i with the output neuron N_j. The initial weights of the synapse are shown in Table 2.

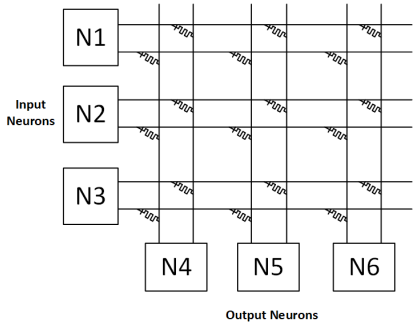

Figure 11: A 3 × 3 crossbar configuration using the bi-memristor synapse.

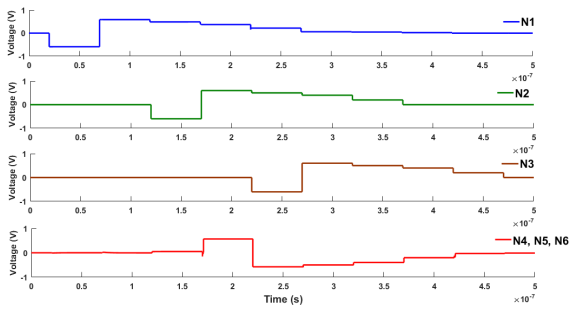

Figure 12: Spiking events of the neurons in the crossbar

The input neurons are provided an artificial trigger, such that they fire as shown in Fig. 12. Since the synapses in the first row are set to a high positive weight, their charge accumulation on the output neurons results in their firing as shown in Fig. 12. Since all the input and output neurons have fired, we have measured the weight updates for each synapse.

It can be seen from Table 2 that synapses in the first row and the second row undergo potentiation while the ones in the third row are depressed. This is because N1 and N2 fire before the output neurons, while N3 fires after the output neurons fire. Also, since the fire of N2 is closer to that of output neurons, ΔG_{eff} for the second row synapses is higher. These simulation results indicate that the proposed synapse and the neuron are amenable for a crossbar implementation with on-chip learning, which is highly desirable for memristive neuromorphic systems [9].

Table 2: Effective conductance of the synapses in the crossbar, showing their conductance changes.

Synapses	$G_{eff\_initial}$(μS)	ΔG_{eff}	G_{eff_final}(μS)
$S_{1,1}, S_{1,2}, S_{1,3}$	77.77	+0.31	78.08
$S_{2,1}, S_{2,2}, S_{2,3}$	0.0	+1.339	1.339
$S_{3,1}, S_{3,2}, S_{3,3}$	0.0	-1.366	-1.366

9. Discussion and Conclusion

In order to gauge the power scenario of our implementation, we have measured the current consumed by the neuron per synapse. The results are tabulated in Table 3.

Table 3: Energy consumption of the proposed system

Phase of the Neuron	Energy per spike time (pJ)
Idle (No input/output spike)	9.816
Accumulation	10.928
Spiking	12.76

In the literature, some groups have reported their energy metrics. Authors in [21] have reported that each synapse consumed 36.7pJ for learning for a resistance range of 70Ω to 670Ω. In [22], the energy consumption was 11pJ to 0.1pJ for a resistance range of 1kΩ to 1MΩ. It can be seen from Table 3 that our energy values are comparable to that in literature. Also, it must be noted that these values were evaluated with a resistance rage of 5kΩ to 50kΩ and a spike time limited to 50ns. With higher resistance values and smaller clock periods (higher frequencies), the values are expected to decrease, since the power consumption in a given phase of the neuron remains the same.

In conclusion, in this paper we have presented a synapse structure that can implement both an excitatory and an inhibitory action. We have shown mathematically, the exponential-like learning behavior of this structure and have verified this through simulations. Further, we have shown that by discretizing the neuron spike in time, we can control the learning behavior and remedy the effects of switching rate mismatch in memristors. We have also demonstrated learning in a 3 × 3 crossbar with our synapse. These results indicate that our synapse can be used to implement spiking neural networks with STDP based on-chip learning.

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