Parasitic-Aware g_m/I_D-Based Many-Objective Analog/RF Circuit Sizing

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***Abstract* - Accurate parasitic consideration in analog/RF circuit synthesis becomes more essential since layout-dependent effects become more influential in the advanced technologies. In this paper, a g_m/I_D-based circuit sizing method, which takes into account both device intrinsic parasitics and interconnect parasitics, is proposed as the first stage of a hybrid sizing optimization. In the second stage, a many-objective evolutionary algorithm is applied to refine the sizing solutions. The proposed methodology has been utilized to optimize multiple performances of an analog dynamic differential comparator and a RF circuit in the advanced CMOS technology. The experimental results have exhibited high efficacy of our proposed parasitic-aware hybrid sizing methodology.**

I. Introduction

In 28nm and below CMOS technologies, five key challenges, including double patterning, layout-dependent effects (LDE), interconnect layers, design rules, and device complexity and variation, are identified for custom and analog designs [1]. The impact of LDE gets increasingly severe, which calls for LDE to be accurately modelled within parameterized cells (Pcells) and close cooperation to be performed between circuit designers and layout designers. Before stepping into the LDE problem, considering that if without a trustable methodology that can reflect the sizing optimization problem with the primary second-order effect, parasitics, the optimization that directly targeting on LDE would be less convincing. Therefore, this paper proposes a transconductance over drain current (g_m/I_D) based method that can meet this requirement to build up an accurate parasitic-aware sizing framework for analog and RF integrated circuits in the nanometer technology.

The previous works that perform automatic layout-aware synthesis can be classified into four categories, which are stochastic-based, deterministic-based, analytical-based, and g_m/I_D-based techniques. Lourenço *et al.* [2] proposed a floorplan-aware analog IC sizing methodology that uses stochastics in the sizing kernel. However, since the parasitic estimation is conducted with the help of designers' knowledge, the generation of a complete layout may be required in the worst case. In addition, their semi-manual generation of floorplan template as well as the used old NSGA-II as the sizing engine have room for improvement. As one example of deterministic approach, Habal and Graeb [3] proposed a method that uses nonlinear optimization with numerical simulation. Because of the used various device layout styles for various placement optimization associated with simulated annealing (SA)-based industrial-level routing tool, and integral field solver for parasitic estimation, the whole process is slower than usual. The CPU time was reported to be 8 times of a traditional circuit sizing process.

For most analytical-based approaches, solving speed and reusability are highly praised. However, they are always under the debate of controversial accuracy matter on problem modelling, for instance, the geometric programming (GP) [4] of this kind. In addition, it is also debatable on how much effort is involved to develop the problem models for analog circuits. The concept of g_m/I_D, which has been suitably adopted in retargeting and sizing problems, is based on the theory that g_m/I_D is solely dependent on node voltage V_{GS} regardless of geometrical sizes. By extending the g_m/I_D theory on sizing domain, we have proposed a new symbolic-based sizing methodology that has conquered the problem of modelling accuracy and modelling effort existing in general analytical-based approaches.

The g_m/I_D mechanism was firstly proposed by Silveira *et al.* [5]. Jespers [6] demonstrated its implication on circuit sizing problem. In early works like [7], designer intervention was heavily required to estimate g_m/I_D values. In [8], SA was utilized to vary MOSFET length (L) and g_m/I_D as free variables with frequent reference to the g_m/I_D curve, resulting in a less designer-intervened approach. In [9], bias information rather than the g_m/I_D parameter is set as variables and a small-scale look-up table (LUT) is built to find the aspect ratios. In [10], operating points are solved from a group of topology-based bias constraints modelled in a linear programming (LP) problem. This replaces the SA perturbations and real simulations called in the SA process [8] in order to reduce the running time. Nevertheless, these works normally neglect the consideration of an important fact that the parameters of g_m/I_D and g_d/I_D as well as device intrinsic parameters are strong functions of V_{DS} and L for sub-100nm technologies. In addition, although the interconnect parasitics have nonlinear nature, they are often simplified and solved by a LP solver in the previous works.

In our proposed two-stage sizing flow, the first stage is called the parasitic-aware g_m/I_D-based sizing framework. It aims at solving a quick global solution that will be imported as an initial elite solution into a second stage sizing refiner which is implemented by a many-objective evolutionary algorithm (many-OEA) called, Theta-Dominance-based Evolutionary Algorithm (θ-*DEA*) [11]. The significance of θ-*DEA* relies on its capability to not only preserve the diversity by maintaining the structural strength from the NSGA-III, but also promote the convergence by borrowing the fitness evaluation scheme from the MOEA/D. In addition, another reason of adopting the second EA stage is to fix fitting errors from the adopted curve fitting technique introduced in Section II and modelling errors between the estimation model and real circuit behavior.

The main contributions of our work are summarized as below.

1) The proposed parasitic-aware g_m/I_D-based analog/RF

circuit sizing framework can reflect technology variation by discarding the conventional inaccurate current equation, which proves to be an accurate analytical-based approach, and is technology retargeting friendly. As another improvement, no LUT is involved.

2) The involved curve-fitting technique can accurately reflect the intrinsic parasitics. The complex interconnect parasitics that depend on device geometry and an optimized floorplan are modelled in non-linear symbolic expressions by using [12]. Since the expressions of parasitics from both parts can be expressed by g_m/I_D parameters, they can be compatibly integrated in the problem modelling. Therefore, the accuracy of parasitic estimation is assured in the first sizing stage.
3) In our second sizing stage, the employment of the sophisticated many-OEA rather than multi-objective EA (MOEA) is a pioneering practice to be the state-of-the-art in the analog EDA domain.
4) Finally, the proposed two-stage methodology inclusive of the g_m/I_D-based sizing framework and the *θ-DEA* sizing refiner proves to be a flexible hybrid sizing approach. The flow can stop at any early stage when the solution is satisfying thanks to the job decomposition between the stages.

The rest of this paper is organized as follows. Section II introduces the proposed g_m/I_D–based sizing framework as the first sizing stage. The *θ-DEA* used in the second sizing stage is discussed in Section III. Section IV describes the modelling of parasitics with floorplan optimization. Experiments and analysis are conducted in Section V. Section VI concludes this work.

II. Proposed Parasitic-aware G_M/I_D–based Sizing Framework

A. Preliminaries

The transconductance generation efficiency, g_m/I_D ratio is defined in [5],

$$\frac{g_m}{I_D} = \frac{1}{I_D}\frac{\partial I_D}{\partial v_G} = \frac{\partial(\ln I_D)}{\partial v_G} = \frac{\partial[\ln\left(I_D/(\frac{W}{L})\right)]}{\partial v_G} , \quad (1)$$

which shows the g_m/I_D ratio is independent of MOSFET width over length, i.e., W/L. Also, the large signal current, I_D, is proportional to W/L for MOSEFTs working in both saturation and triode regions. So I_{DN}, the normalized I_D, defined as $I_D/(W/L)$, is independent of W/L as well. The sizing result is finally achieved via,

$$\frac{W}{L} = \frac{I_D}{I_{DN}} = \frac{I_D}{I_{D_{REF}/(W_{REF}/L_{REF})}} , \quad (2)$$

where the parameters with "$_{REF}$" are obtained from simulations on a unit-size MOSFET by sweeping node voltages. According to the definition of g_m and its approximation equations, the g_m/I_D ratio only relates to the node voltages of V_{GS}, V_{DS}, and V_{TH}. Therefore, the g_m/I_D, I_{DN}, and a set of node voltages of a MOSFET are all one to one corresponded. Once I_D and any of the three parts are available, the aspect ratio can be determined.

The drain conductance to current ratio, g_d/I_D is also proportional to L for a long channel transistor because it can be inversely determined by the early voltage, $(V_{EA})^{-1}$. The intrinsic parasitic capacitance C_{ij} relates to device geometry (i.e., $W*L$), where i and j can be any of the drain, source, gate or bulk nodes. I_D is proportional to W/L and so,

$$\frac{C_{ij}}{I_D} = L^2 C_{others} , \quad (3)$$

where C_{others} reflects other effects which include oxide capacitance and gate overlap capacitance. Therefore, with a given L, C_{ij}/I_D can be independent of transistor sizes as well.

B. Parasitic-Aware g_m/I_D-based Circuit Sizing Framework

In the initialization of this sizing framework, firstly, L is estimated according to the given technology and general analog circuit design knowledge. A group of variable ranges of V_{gs} and V_{ds} for all MOSFETs as well as an initial bias condition in the target circuit need to be decided. They can be coarsely supplied by a zero-knowledge designer as for example, 250mV to 850mV of V_{gs} for a CMOS 65nm NMOS with 1V supply, and be set by the median values of the ranges respectively. However in this work, we use a LP to solve a bias determination problem, which is modelled with a list of topology-dependent linear constraints with respect to bias conditions like in [9], and apply user-defined percentage to extend the definite bias conditions into the variable ranges of V_{gs} and V_{ds}. These settings in this initialization step would configure the variable space and provide a starting point.

The objective in the problem modelling requires to be minimized via,

$$obj = c_1 \sum_{i=1}^{s} \frac{\left(\frac{g_{m_i}}{I_{D_i}}\right)_{I_{ss}}}{\left(V_{GS_i} - V_{TH_i}\right)} + c_2 \sum_{j=1}^{t} intDist_j + c_3 I_{ss} V_{DD}, \quad (4)$$

where the user-defined parameters of c_1, c_2, and c_3 are the normalized weighting factors for sum of device sizes, sum of interconnect distances, and power consumption. s and t are the number of MOSFETs and the number of interconnect sections between any two devices respectively, and $intDist_j$ is the distance for each interconnect.

In order to formulate the bias constraints on the whole circuit, linear inequalities of voltage and current depending on circuit topology can be built up, which are reflected by relationships between the free variables (i.e., V_{DS} and I_D) and power components (i.e., V_{DD} and I_{SS}) respectively. The constraints on operating region of each MOSFET are reflected by a group of relationships between node voltages, threshold voltage, and thermal voltage when the subthreshold region is considered.

Next, all the performance equations are expressed as functions of g_m/I_D, g_d/I_D, and C_{ij}/I_D as well as node voltages, and further transformed to inequalities with respect to specifications,

$$f_s(V_{GS}, V_{DS}, \frac{g_m}{I_D}, \frac{g_d}{I_D}, \frac{C_{ij}}{I_D}, I_D) \leq \text{ or } \geq \ Spec._s , \quad (5)$$

where C_{ij} normally refers to C_{gs}, C_{ds}, and C_{db}. g_m/I_D, g_d/I_D, and

C_{ij}/I_D can be expressed in terms of node voltages as well as I_{DN} which will be introduced in the following paragraph. Therefore, W/L of each transistor can be found, according to (2), once the corresponding node voltages and bias currents are solved, and then W is determined given L.

For sub-100nm technologies, the transistor characteristics of g_m/I_D, g_d/I_D, C_{ij}/I_D and I_{DN} are seriously affected by V_{DS} and L in addition to the main dependence on V_{GS}. The relationships between the characteristics and the two variables (i.e., both V_{GS} and V_{DS}) are reflected by simulation and then are fitted into nonlinear symbolic expressions. The unit size transistors with fixed W and varying L under controlled biased voltages applied amongst all four nodes are used to conduct the simulation experiment. In our practice for the CMOS 65nm technology, W is 1μm with L changing from 60nm to 600nm. Both of V_{GS} and V_{DS} vary from 50mV to 950mV.

After importing the simulation data to Matlab, a nonlinear curve fitting toolbox is resorted to perform the fitting reflected by,

$$g_k = f(V_{GS}, V_{DS})_k|L \ , \tag{6}$$

where g_k is any of the $\frac{g_m}{I_D}, \frac{g_d}{I_D}, I_{DN},$ or $\frac{C_{ij}}{I_D}$ for a given L. It provides a significant improvement in accuracy over the conventional large signal square-law current equation, the estimation of g_d/I_D in long-channel condition, and the calculation of device intrinsic parasitics from any other non-numerical-simulation based models including from the textbook. In addition, there is no involvement of LUT search, which is totally different from the previous works. Finally, the modelled nonlinear programming problem is solved within one single execution by the Matlab interior point optimizer-nonlinear solver (IPOPT-NL).

The solution from this round of optimization does not include any interconnect parasitics and is referred to as parasitic-free sizing optimization. We decompose the sizing task by firstly having this parasitic-free optimization followed by a parasitic-aware optimization with the update of capacitance and resistance introduced via (7). The obtained sizes associated with bias conditions and the implied variable ranges from this parasitic-free optimization are used as a starting point and would help configure the solution space for the following parasitic-aware optimization that is a harder problem.

$$R_{total} = ((\frac{g_d}{I_D})I_D)^{-1} \ op \ R_{int} \ ,$$
$$C_{total} = ((\frac{C_{ij}}{I_D})I_D) \ op \ C_{int} \ , \tag{7}$$

where R_{total} and C_{total} are the total resistance and capacitance, R_{int} and C_{int} are the interconnect portion for one electrical net, which will be introduced in Section IV, and *op* is the parallel or serial operator dependent on the connection type.

In addition to (7), we also include parasitic constraints according to sensitivity analysis in the proposed parasitic-aware optimization in order to prevent performance degradation caused by variation of certain influential parameters (e.g., g_m/I_D or g_d/I_D of some MOSFETs), which is originally stemmed from the disturbance of interconnect parasitics. Given the previous parasitic-free sizing solution verified in a simulation environment, the sensitivity study is conducted through varying resistance or capacitance at a net and then measuring the relationship among node voltage changes, the changes of influential parameters, and performance degradation.

Finally, the solution solved by the deployed IPOPT-NL from the parasitic-aware optimization can reflect size adjustments based on the previous parasitic-free solution. Along with the whole sizing framework, the challenging sizing problem with technology-dependence in terms of device characterization as well as intrinsic parasitics, and the second-order interconnect parasitics are broken down via the optimization decomposition. In addition, the involved simulation and curve fitting are technologies and tools dependent but the proposed methodology is not subject to changes of them, and so the proposed g_m/I_D-based sizing framework is applicable for retargeting tasks. Lastly, the success of the sizing task with parasitic awareness is based on the large likelihood that a parasitic-aware sizing solution point is promisingly located near a parasitic-free solution point. So we adopt an EA-based second stage sizing optimization in order to consolidate the quality of the sizing result from the first stage.

III. Second-stage EA Sizing Optimization

In the first stage optimization, fitting errors and modelling error are inevitable. We employ a numerical-simulation involved evolutionary algorithm to refine the optimization with full accuracy in the second sizing stage, which matches our consolidation purpose concerning the sizing quality. However, for any EA-based application, it is often costly to search in a large solution space, and it is especially true for our application since the repeated numerical simulations take much time. Therefore, we introduce the g_m/I_D elite solution that implies a localized variable ranges for configuring reasonable search space by using the following strategy. To be clear, the free variables in the g_m/I_D sizing stage are voltages and currents in (5) and the device sizes (i.e., W and L) are obtained via (2) once the NLP problem is solved. However, the sizes are directly to be the free variables (called chromosome-variables hereafter) in the second EA sizing stage.

A user-specified percentage (100% by default) is attached to each size value obtained from the g_m/I_D elite solution to provide the upper and lower bounds. Then a step size has to be determined for enumerating possible discrete values within the elite-implied variable range accordingly. In our practice, 10nm and 5nm were used by default as the step sizes for W and L respectively. Special care should be given to the inductor since the relationship between its device properties (e.g., Q factor and inductance) and geometric parameters (e.g., radius, width, and turns) are highly discontinuous and nonlinear. In contrast, without any clue of the g_m/I_D elite solution, any EA method may be obligated to set wider variable ranges in order to avoid missing any potential optimal solutions, which would cause hardship in the subsequent search and optimization.

Our selection criteria of EA to conduct the second-stage sizing optimization depend on whether the algorithm can utilize the locality inherently existing inside problems, which helps smooth the search, and whether it can deliver multiple performance with desirable balance. For our adopted *θ-DEA* [11], firstly, the included simulated-binary-crossover scheme

can efficiently mutate the variables in a random way, and it inherently realizes a self-adaptive idea for controlling variables, which properly utilizes or explores the locality. Secondly, it demonstrates its advances as a many-OEA that outperforms NSGA-II as a MOEA in applications with more-than-three objectives. In detail, an important idea, cluster or niche, which was used in NSGA-III is inherited to *θ-DEA*. It is used to map the complex high-dimensional solution space of a complicated real problem to a unit solution space under the control of uniform distribution. Then the *θ-DEA* attempts to convert the selection criteria from basing on regular nondominated sorting of direct performance to a nondominated sorting of a function evaluation result. This function that is very similar to the aggregation function used in MOEA/D has a penalty parameter, θ, to control the selection pressure making it so-called θ-dominance. This function works as a cost indicator, which avoids involving with direct performance, with well-balanced stress regarding diversity and convergence.

IV. Parasitic-awareness in g_M/I_D and EA-based Sizing

In this section, we introduce how to obtain layout information which is necessary to accurately reflect interconnect parasitics, and how to calculate and integrate the parasitics into the proposed two-stage hybrid sizing method.

A. Floorplan Optimization and Global Routing

Interconnect relationships among all modules representing all devices in a circuit have to be identified in order to perform any calculation of interconnect parasitics. Interconnection information in early design stage is normally derived from a floorplan that includes placement and global routing. On one side, providing a fixed floorplan template for each specific circuit would lose flexibility and generality. On the other side, enumerating all device layout styles and placement combinations [3] is too complex and time consuming. Most placers or floorplanners take device modules as the input, which are defined by concrete geometry sizes, however, the sizes are the target rather than given.

In our g_m/I_D-based sizing stage, the parasitic-free sizing solution provides a group of decent sizes to be utilized as geometry modules for the floorplanner. The modules that facilitate the device layout style and limit the placement combination possibilities presumably do not alert the usability of the final optimized floorplan due to the locality assumed between the parasitic-free sizing solution and the parasitic-aware solution. In the practice, the adopted floorplanner that is right inserted between the two sizing optimization processes is similar to [13]. It takes a list of modules as input, transfers the modules' connection information into B*-tree representation, uses SA-driven engine to perturb the B*-tree structure in order to consider various placement styles, and finally converges to one B*-tree chain, which is a compact candidate floorplan.

Since we want to deploy and maintain a robust and tractable floorplan template used in both the g_m/I_D–based first stage and the second EA stage, the following considerations in terms of reasonable signal flows, resemblance to topology, and implementation status of constraints and objectives (e.g., matching and area) are used to constrain the search for a robust floorplan. The Manhattan distance between two nodes (i.e., the center coordinates of modules) is used to perform the global routing and to obtain the distance of shortest path in a symbolic form for the selected floorplan.

B. Calculation and Integration of Interconnect Parasitics

After the global routing, the interconnect relationship is clear, and the interconnect distance between any two MOSFETs is expressed by geometry parameters including finger number, technology parameters, and certain other user-specified parameters. Next, we use the analytical model [12] which declares to have less-than-10% estimation errors in calculating the interconnect parasitic capacitance for diverse technologies. The interconnect parasitic resistance, R_{int}, can be calculated with given sheet resistivity and the thickness of the interconnect layer, both as technology-dependent constants. All of the adopted parasitic models are in simple nonlinear form, which can be easily integrated into the proposed g_m/I_D-based sizing framework via (7).

The integration of interconnect parasitics into the EA sizing stage is even more straightforward as follows. By preserving the optimized floorplan and the global routing, the symbolic interconnect expressions are functions of sizing variables (i.e., EA chromosome-variables) directly. After applying the same parasitic models mentioned above, the calculated interconnect capacitance and resistance are present on important electrical nets complementary to a pure schematic-level netlist. With respect to the intrinsic parasitics that are modelled by $(C_{ij}/I_D)*I_D$ in the first g_m/I_D stage, they already have been considered by just including the foundry provided models in the netlist. Therefore, the second EA sizing stage with simulation-level accuracy remains to be parasitic-aware.

V. Experimental Results

In this paper, we have conducted experiments on two circuits in order to justify the proposed methodology. Fig. 1(a) depicts a dynamic comparator called differential-pair comparator, and Fig. 1(b) depicts a cascode common-source LNA working at 5.6GHz both in the CMOS 65nm technology.

A. g_m/I_D Modelling with Parasitic-Awareness

We firstly demonstrate the key part of the g_m/I_D modelling for the comparator example as follows. As the comparator is latch based and driven by clock signals, it has minimum power consumption and is also faster than any gain-based comparator. The propagation delay of the latch, t_{prop}, as a target performance, is expressed in terms of the final high and low output voltages (i.e., V_{oh} and V_{ol}),

$$t_{prop} = \tau_l ln\left(\frac{V_{oh}-V_{ol}}{2\Delta V_{in}}\right) , \quad (8)$$

where ΔV_{in}, which is always less than V_{oh} - V_{ol}, is the difference between the two latch output voltages before the latch is enabled. τ_l is the latch time constant that can be specified via,

$$\tau_l = \frac{C_{out}}{(g_m/I_D)_7 I_{D7}} , \quad (9)$$

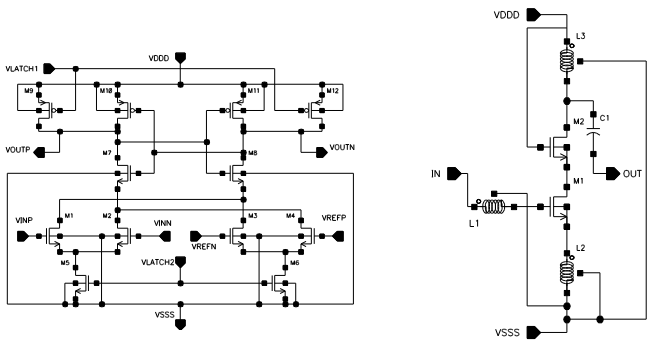

Fig. 1. Circuit diagrams for a): Dymanic differential comparator and b): Cascode common source LNA with source degeneration

where C_{out} is the total capacitance at the positive ($C_{out,p}$) and negative ($C_{out,n}$) output nodes. These capacitances are,

$$C_{out,p/n} = (\frac{C_{db}}{I_D})_{7/8} I_{D7/8} + (\frac{C_{db}}{I_D})_{10/11} I_{D10/11} + (\frac{C_{gs}}{I_D})_{11/10} I_{D11/10} + (\frac{C_{gs}}{I_D})_{8/7} I_{D8/7} + C_{int,p/n}, \quad (10)$$

where the slash symbol represents the meaning of "OR", and $C_{int,p/n}$ is the interconnect capacitance that can be modeled in a symbolic way by using the optimized floorplan described in Section IV. Finally, by considering $C_{int,p/n}$ via (10) into (9), and into (8), interconnect parasitics are finally considered in the performance expression in the g_m/I_D problem modelling.

Once the modelled sizing problem is solved by the NLP solver, sizes as well as bias information are clear. Also by verifying the solution in the simulator, DC bias information is also available. Table I depicts the DC point differences of the latch device M7 among the one reported by the simulator (i.e., the reference), the one reported by the NLP solver, and the one calculated by traditional equations. Observed from Table I, there is a good convergence of node voltages while a moderate difference of g_m between the reports from the first two columns. This is because the value calculated from the fitted equation is from a single device simulation, which can be different from its DC performance in a real circuit simulation. Nevertheless, thanks to the introduction of g_m/I_D parameter, which has less estimation error of 16.3%, g_m with such a difference of 30.8% can be avoided to be directly involved in our modelling.

For the report by using traditional equations, the node voltages as well as V_{TH} and μ are unknown. Even though by assigning accurate values from the simulation conditions to these unknown terms and considering the channel length modulation effect, the estimated current still has a huge error of 84.1%. In addition, the acquired g_m/I_D of 59.88 is impossible

Table I. DC Point Differences among the Verified Solutions by the Simulator, the NLP Solver and the One from Traditional Estimations.

NMOS M7	Simulation DC point	NLP solved DC Point	Diff. (%)	Tradi. Estim.	Diff. (%)
V_{GS} (m)	470.6	474.6	0.8	-	-
V_{DS} (m)	470.2	463.5	1.4	-	-
g_m (μ)	600.9	415.6	30.8	420.4	30.0
I_D (μ)	44.02	36.36	17.4	7.02	84.1
g_m/I_D	13.65	11.43	16.3	59.88	77.2

as it should not be over 33 for an 110n NMOSFET in our experiment at CMOS 65nm. Therefore, if the traditional estimation equations are used in any modelling approach, plenty of tweaking efforts are expected, not to mention that those necessary technology-dependent parameters are hard to be symbolically expressed. Most of them even depend on device geometry (i.e., the objective of sizing task) and hence is harder to utilize.

B. g_m/I_D-θ-DEA Hybrid Sizing

From the experimental data in Table I, it is clear that these differences cannot be completely eliminated in our proposed g_m/I_D sizing stage. This may be due to certain fitting errors and/or modelling errors, so the solution from the g_m/I_D sizing stage is sub-optimal. The concatenated EA sizing stage would conduct optimization by simulating the circuits with full accuracy, which relaxes the concern of sub-optimum. In each experiment, five schemes are compared from Scheme-0, the standalone g_m/I_D sizing method, to Scheme-4, our proposed g_m/I_D-*θ-DEA* sizing method configured with small search space where the evolutionary population size * maximum generation number = 32 * 20. Without any elite solution as guidance information, the standalone *θ-DEA* has to search in a large space with the configuration of 56 * 40 reflected by Scheme-3. To compare the performance with the single-objective optimization methods, Scheme-1 that reflects a conventional evolutionary algorithm on analog circuit sizing [14] is set with the large configuration whereas Scheme-2 that imitates an idea from a layout-aware sizing work [15] is set with the small configuration thanks to our supplied g_m/I_D elite information.

10 runs are performed for Schemes-1 to 4. A minimization-based cost function from [16] is used, which unifies the metrics for comparison between single-objective methods (i.e., S. in Tables II and III) and many-objective methods (i.e., M. in Tables II and III). The success rate (i.e., SR) that stands for the ratio of specification-satisfied solutions over a whole population is used in order to avoid unaccountable data because the *θ-DEA* would include infeasible corner solutions due to the nature of systematic distribution of reference points. Nevertheless, due to the convergence feature for single-objective methods, infeasible data should be included for report, and so the conventional meanings of average (i.e., Average-cost) and standard deviation (i.e., Std.) hold for single-objective methods in Tables II and III. Finally, the solution with the smallest cost value is selected as a representative for reporting real performance. The experiments were performed on an 8-core Intel Xeon CPU E5-2650 @ 2.00GHz. The *θ-DEA* sizing engine was implemented in C++, and the circuit performance used in the cost function was verified by the Cadence Spectre.

In Table II, the propagation delay is one of the most important characters for the comparator circuit, and the "+Os." and "–Os." are short for positive and negative overshoot in Table II. Firstly, the single-objective methods generally cannot deliver good solutions that can pass the specification, even at the cost of large evolutionary resources and run time reflected by Sch-1. The best-cost in Sch-2 improved from 0.496 (i.e., based on Sch-0) to 0.483 due to the integration of g_m/I_D elite,

Table II. Settings and performance of the Differential Comparator

Schemes	g_m/I_D	Single-objective Methods		Many-objective θ-*DEA* Methods	
	Sch-0	Sch-1 [14]	Sch-2 [15]	Sch-3 Large Config.	Sch-4 This work
S./M.: Best-cost	0.496	0.707	0.483	0.267	0.224
M.: Average-cost	-	-	-	0.320	0.284
M.: Success-Rate	-	-	-	30.77%	82.14%
S.: Average-cost	-	0.712	0.513	-	-
S.: Std.	-	0.005	0.021	-	-
Run Time (mins)	3.16s	28.27	12.15	37.72	12.52
Specification	**Performance (from the Representative Solution with the Smallest Cost)**				
Delay < 250ps	152.5	279	320	175	108
+Os. < 350mV	183.0	220	20	11	37
-Os. < 150mV	53.3	57	13	10	20

but at a wrong direction because the cost is the only metric in such a single-objective approach. However, influenced by the advance of θ-*DEA*, the representative solutions from both Sch-3 and Sch-4 passed the specification. In addition, the high success rate of 82.14% and low run time of 12.52 minutes of our proposed Sch-4 benefited from the integration of g_m/I_D elite, which indicates a wise localized search.

In the LNA example, the performance of S22 (i.e., -10.10) from Sch-0 just passed the specification due to the complexity nature of this RF circuit. With the help of the g_m/I_D elite in Sch-2, the best-cost improved only a little from 0.814 to 0.813, but the high average-cost of 2.649 and standard deviation of 1.654 exhibit a chance for further improvement inside a promising search space implied by the g_m/I_D elite solution. Whereas for Sch-1, the evolution almost converged after 23.85 minutes but focused at a poor corner (i.e., best-cost of 1.058). Because for the single-objective EA, without any guidance from the elite knowledge, it is not guaranteed to locate a good region and it is hard to escape from certain poor localizations due to the discontinuousness and nonlinearity of LNA mentioned in Section III. However, multiple reference regions are distributed in the beginning of the θ-*DEA* method to avoid all individuals in a population being trapped in bad regions, demonstrating the success of the optimization for both Sch-3 and Sch-4. The reasonably confined search space by the g_m/I_D elite in Sch-4 proves a favorable time efficiency over Sch-3.

Table III. Settings and performance of the Low Noise Amplifier

Schemes	g_m/I_D	Single-objective Methods		Many-objective θ-*DEA* Methods	
	Sch-0	Sch-1 [14]	Sch-2 [15]	Sch-3 Large Config.	Sch-4 This work
S./M.: Best-cost	0.814	1.058	0.813	0.787	0.731
M.: Average-cost	-	-	-	0.838	0.807
M.: SR	-	-	-	5.36%	50.00%
S.: Average-cost	-	1.058	2.649	-	-
S.: Std.	-	0.0003	1.654	-	-
Run Time (mins)	3.17s	23.85	9.94	32.26	10.89
Specification	**Performance (from the Representative Solution with the Smallest Cost)**				
Gain > 15dB	21.21	18.75	20.05	21.45	20.47
NF < 2.5dB	2.04	2.15	2.08	2.06	1.90
S11 < -10dB	-13.45	-5.26	-13.52	-15.56	-17.08
S22 < -10dB	-10.10	-14.88	-10.74	-10.20	-11.80

VI. CONCLUSIONS

In this paper, an efficient parasitic-aware two-stage g_m/I_D-θ-*DEA* circuit sizing methodology for high-performance analog and RF circuits has been presented. It adopts the g_m/I_D concept and curve fitting technique to model the parasitic-aware sizing problem in NLP form in the first stage and then concatenates a sophisticated many-objective evolutionary algorithm optimization to conduct a sizing refinement. The second EA stage that involves numerical simulations for accuracy compensation benefits from the g_m/I_D elite solution for a smaller and more focused search space. We demonstrated the application of the proposed methodology to a Comparator and an LNA. The sizing results from our proposed Scheme-4 with small cost and small run time have shown the efficacy of our proposed methodology associated with its introduced novelty, flexibility, and reliability.

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