Body-Biasing Assisted Vmin Optimization for 5nm-Node Multi-Vt FD-SOI 6T-SRAM

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Abstract

This work proposes a body-biasing technique to optimize V_{min} of the 6T-SRAM based on 5nm-node multi-V_t FD-SOI devices. Accounting for the process variation, the operating voltage, V_{min}, is estimated at 6-sigma yield. By properly selecting the back bias, the lowest V_{min} is achieved for each of the three operation modes: high-performance, standard and low-voltage modes. In high-performance mode, the optimized V_{min} is reduced to 0.491 V at back bias of 0.2 V. The proposed technique offers a design flexibility for optimizing the SRAM performance and yield by adjusting the back bias without complicated process technology requirements.

Keywords

FD SOI, 6T-SRAM, body biasing

1. Introduction

A body-biasing technique to optimize V_{min} of the 6T-SRAM based on 5nm-node FD-SOI devices [1] using TCAD [2] and macro modeling is demonstrated. The conceptual schematic of the FD-SOI device is shown in Fig. 1. The transistor is designed with channel length (L_G) = 11.6 nm, effective channel length (L_{eff}) = 9.3 nm, EOT = 0.6 nm, buried oxide thickness (T_{BOX}) = 10 nm, off-current (I_{Off}) = 100 nA/µm at V_{DD} = 0.77 V. In addition, we use an undoped channel to simplify the process and a highly-doped substrate to reduce the substrate resistance. We calibrate an analytical macro-model developed in [3] to predict 6T-SRAM yield and performance, including I_{DS}-V_{GS} characteristics, read static noise margin (SNM) and write current. The macro-model utilizes a simpler analytical transistor I-V model to predict the 6T-SRAM performance based on key parameters calibrated to device-level TCAD simulation. We demonstrate the accuracy of the calibrated I-V macro-model for the two cases in Figs. 2(a) and (b). The method of 6T-SRAM yield estimation for FD-SOI devices is developed as an extension to A.E. Carlson's [3] and C. Shin's [4] works.

2. Substrate doping and V_B dependency for V_t

The V_t of FD-SOI is adjustable by back bias (V_{GB}) [5]. For n-type FET, a positive voltage (Forward Back Bias) applied in the substrate can make the V_t lower. On the other hand, a negative voltage (Reverse Back Bias) applied in the substrate can increase V_t. Oppositely, a positive voltage applied in the substrate will make the V_t higher for p-type FET. Figure 3 shows the I_{DS}-V_{GS} curves for n- and p-channel FD-SOI devices at different back biases. We can observe the shift of the curves from forward bias $|V_B|$ = 0 V to $|V_B|$ = 0.77 V. It suggests that we can make use of this feature into circuit design to get a needed threshold condition. Figure 4 shows V_t variation at different back biases for both n- and p-channel FD-SOI MOSFETs, and it illustrates a V_t window of 107 mV for n-channel FET and a V_t window of 108 mV for p-channel FET by modifying its back bias from V_{DD} to ground in a fixed device structure.

The V_t variation at different substrate doping levels from $N_{D,sub} = 1\times10^{19}$ cm^{-3} to $N_{A,sub} = 1\times10^{19}$ cm^{-3} is demonstrated in Fig. 5, and a V_t window of 126 mV controlled by doping when back bias is 0 V is observed. Nevertheless, there is a significant gap in the figure from the substrate doping N_A = 1×10^{17} cm^{-3} to N_A = 1×10^{19} cm^{-3} because the substrate interface (box-substrate) is depleted in this doping range, and it makes the band bending harder to be changed in the front surface of the silicon film. The large V_t variation in a highly-doped substrate is made use of for the following designs.

3. SNW and I_W of 6T-SRAM

The SRAM cell stability determines the soft error rate and the sensitivity of the memory to process tolerances and operation condition. The stability as expressed by the static-noise margin for read [6] and write current for write [7] has been investigated intensively for the SRAM cells. Due to limited cell area for both read and write requirements, it is a trade-off between static-noise margin (SNM) and writeability of the 6T-SRAM.

An analytical macro-model developed in [3] can predict SNM and I_W very efficiently after calibrating the model to I-V data for each single transistor of 6T-SRAM, and the tool allows us to evaluate the 6T-SRAM without intensive TCAD computation. As shown in Figs. 6 and 7, the read transfer characteristics and write N-curves predicted by the macro model agree with the TCAD results..

4. Yield estimation

A cell sigma can be defined for read static noise margin (RSNM) and write current (I_W) under certain process variations. The metric is assumed to be Gaussian distribution and is expressed by the mean divided by standard deviation for each of the transistors. The cell sigma is sought at the minimum value of the standard deviation for any combinations of variation sources which can cause a read or write failure. The process-induced variation in channel width, gate length and V_t variation are the factors accounted for in the cell sigma. And we assume Gaussian distribution with 3σ = 10% of the nominal value for each variation source, e.g. 3σ of L_G = 1.16 nm in our work.

As expected, the technology against random variations such as gate line-edge roughness and random dopant shall be improved from generation to generation. Given that each of the variation sources follows Gaussian distribution with 3σ = 10% of its nominal value at 5nm technology node, the six-sigma yield for both read and write operations is required for SRAM of large capacity.

5. V_{min} optimization technique

The features of FD-SOI devices are used to design the 6T-SRAM in three different modes: standard mode (SD), high-performance mode (HP) and low-voltage mode (LV). Each of

them is controlled by its back bias. In standard mode (SD), we want to balance SNM and writeability. None of the two features is outstanding. That is why we name it "standard". When the application requires a robust write function, we can decrease the α ratio (PU:PG) to switch the design to high-performance mode, which is aimed at write capability, by controlling the back bias. Therefore, an improved write current is achieved for the HP mode without any additional tuning on the process technology. Likewise, in LV mode, which is aimed at the condition of lowest $V_{B,PU}$, we must get an outstanding SNM using a large β ratio (PD:PG).

The substrates of the SRAM transistors are applied with a back bias (V_B) independently. By adjusting V_B, the SRAM characteristics will be transferred because of different electric characteristics of the transistors. In these 6T-SRAM designs, we need extra areas comparing with conventional SRAMs to add controlling circuits for modifying the back bias in the substrates of transistors. To decrease the area cost for SRAM, a shared body as well as a shared substrate beyond the buried oxide are used in PG and PD transistors. To achieve the three different modes for different demands, $V_{B,PU}$ is fixed at 0 V, 0.37 V and 0.77 V for LV, SD and HP modes, respectively. $V_{B,PG}$ and $V_{B,PD}$ are adjustable in each mode for the dynamic design and optimization. The two biases, $V_{B,PG}$ and $V_{B,PD}$, are connected for ease of the shared substrate. All combinations of the back bias in PU, PG and PD substrate are listed in Table 1 and shown in Fig. 8. The predicted yields of read SNM as well as write current for SD mode are shown in Figs. 9 and 10. When $V_{B,PD}$ and $V_{B,PG}$ are set to 0.77 V, to make the yield more than 6 sigma the V_{DD}'s must be higher than 0.569 V and 0.413 V for read and write, respectively. The other lowest V_{DD}'s in different bias conditions for each mode are listed in Table 2 to 4. By analyzing the yield estimation, the V_{min} of SRAM can be projected and optimized.

In a conventional SRAM circuit design, V_{min} is a very important parameter, which is defined as the minimum operation voltage based on 6-sigma yield for both read and write. For example, in the SD mode with $V_{B,PD}/V_{B,PG}$ at 0.77 V, we have to choose 0.569 V to be the V_{min} because the yields are more than 6 sigma for both read and write when the V_{DD} is at least 0.569 V, as shown in Table 2. This work also proposes a dynamic SRAM design in which we can change $V_{B,PG}/V_{B,PD}$ from 0 V to 0.77 V to get the lowest V_{min}. For instance, if we want to target the read function in SD mode, $V_{B,PG}/V_{B,PD}$ would be connected to 0 V, and the minimum operation voltage is about 0.409 V for read yield, as shown in Table 2 to 4. When the SRAM performs a write operation, $V_{B,PG}/V_{B,PD}$ would be connected to 0.77 V, and the minimum operation voltage is 0.413 V for write yield. Therefore, the lowest operation voltage V_{min} for both read and write yields in this mode is 0.413 V. Following the similar methodology, we can get V_{min} = 0.413 V in LV mode and 0.473 V in HP mode. However, for circuit design perspective, the back bias range should be limited to $V_{min.}$ In other words, the bias range of $V_{B,PG}$ is not allowed to exceed V_{min}. As shown in Fig. 11 to Fig. 13, V_{min}'s in LV, SD and HP operation modes are 0.473 V, 0.436 V and 0.464 V, respectively. The bias range condition and the V_{min}'s in dynamic SRAM design of the three modes are listed in Table 5. In LV mode, $V_{B,PG}/V_{B,PD}$ is fixed at 0.77 V. In SD mode, $V_{B,PG}/V_{B,PD}$ is in the range from 0.233 V to 0.668 V. In HP mode, $V_{B,PG}/V_{B,PD}$ is in the range from 0 V to 0.334 V. Besides the dynamic SRAM design, we also demonstrate an optimization technique for minimizing V_{min} at a fixed $V_{B,PG}/V_{B,PD}$. The minimum V_{min} in each mode is determined by the intersection of V_{DD} at 6 sigma for read and write yields. The star symbols in Fig. 11 to Fig. 13 show the minimum V_{min} at a fixed $V_{B,PG}/V_{B,PD}$. In LV mode, the minimum V_{min} is same as that of the dynamic design. In SD mode, the optimized V_{min} is 0.471 V at $V_{B,PG}/V_{B,PD}$ = 0.76 V. In HP mode, the optimized V_{min} is 0.491 V at $V_{B,PG}/V_{B,PD}$ = 0.20 V. All the minimum V_{min}'s are listed in Table 6.

6. Conclusion

The V_{min} optimization technique for the 6T-SRAM using 5nm-node multi-V_t FD-SOI devices has been demonstrated. By properly selecting the back bias, the lowest V_{min} is achieved for each of the three operation modes: high-performance, standard, and low-voltage modes using a dynamic or a fixed back bias. The optimized V_{min}'s of using a fixed back bias $V_{B,PG}$ in LV, SD and HP operation modes are 0.473 V, 0.482 V and 0.491 V, respectively. The V_{min}'s of the dynamic SRAM design can be achieved at 0.473 V, 0.436 V and 0.464 V in LV, SD and HP operation modes, respectively. The proposed back-biasing technique is flexible and can be integrated with conventional multi-V_t FD SOI technology.

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References

[1] International Technology Roadmap for Semiconductors, 2013.

[2] Sentaurus Devices, User Manual, Synopsys Inc. Mountain View, CA, USA, Mar. 2013.

[3] A. E. Carlson, "Device and circuit techniques for reducing variation in nanoscale SRAM," Ph. D. dissertation, Dept. EECS Univ. California Berkeley, CA, pp. 21-61, 2008.

[4] C. Shin, "Advanced MOSFET designs and Implications for SRAM scaling," Ph. D. dissertation, Dep. EECS Univ. California Berkeley, CA, pp. 23-27, 2011.

[5] H.-K. Lim and J.G. Fossum, "Threshold voltage of thin-film silicon-on-insulator (SOI) MOSFET's," *IEEE Trans. Electron Devices*, vol. 30, pp. 1244-1251, Oct. 1983.

[6] E. Seevinck, F. J. List, and J. Lohstroh, "Static-noise margin analysis of MOS SRAM cells," *IEEE Journal of Solid-State Circuits*, vol. 22, no. 5, pp. 748-754, 1987.

[7] Q. Chen et al., "Critical current (I_{CRIT}) based SPICE model extraction for SRAM cell," in *Proc. 2008 IEEE International Conference on Solid-State and Integrated-Circuit Technology*, pp. 448-451.

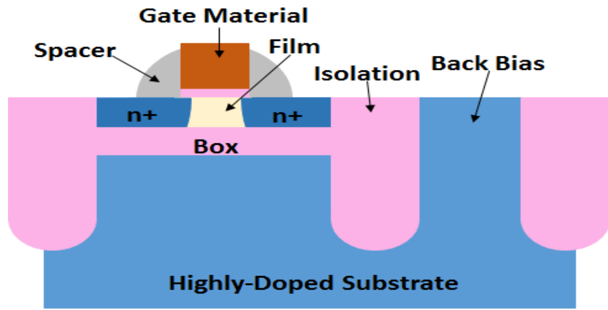
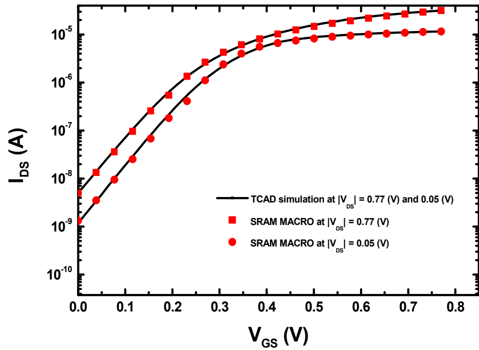
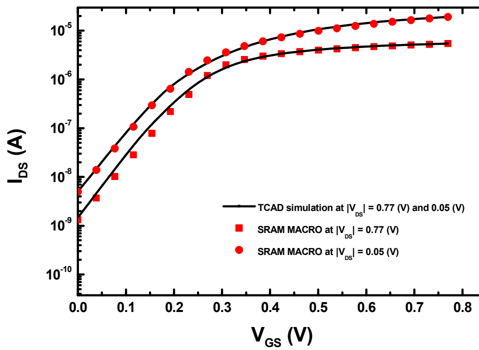


Figure 1. Conceptual schematic of FD-SOI (not to scale)



(a)



(b)

Figure 2. Simulated I_{DS}-V_{GS} curves for (a) n- and (b) p-channel FETs at V_B = 0.77 V using TCAD simulation and macro-model. The voltages in (b) are shown in absolute values for comparison.

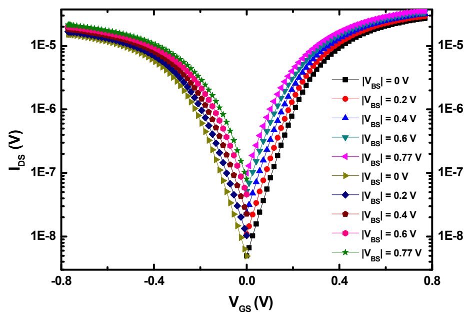


Figure 3. I_{DS}-V_{GS} curves for n- and p-channel FD-SOI devices at different back biases

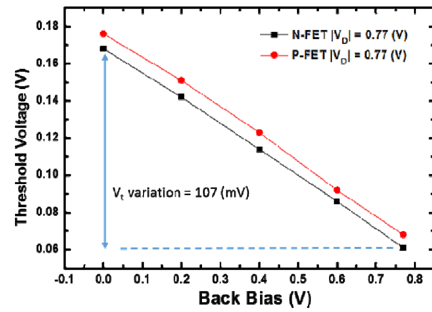


Figure 4. V_t variation in different back biases for both n- and p- channel devices.

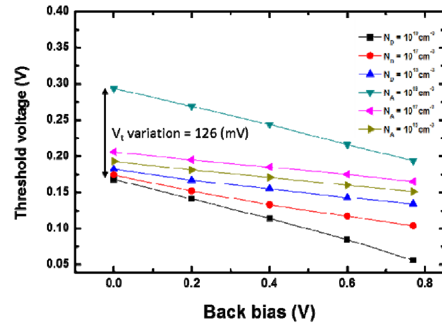


Figure 5. V_t variation in different substrate doping levels.

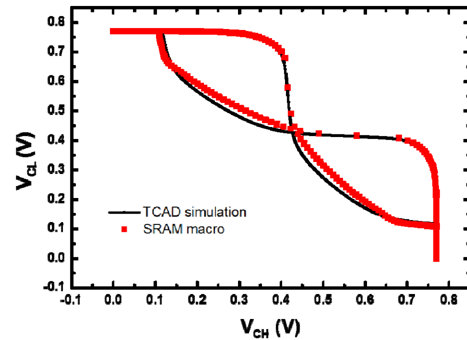


Figure 6. TCAD- and model model-predicted read voltage transfer characteristics for the 6T-SRAM cell

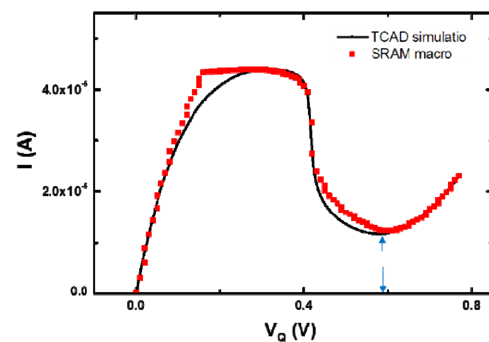


Figure 7. TCAD- and macro model-precited write N-curves for the 6T-SRAM cell

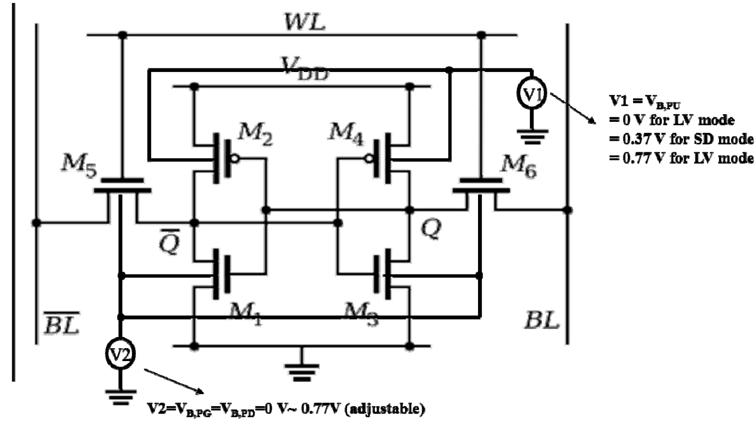


Figure 8. The 6T SRAM circuit schematic with the bias conditions for the three modes.

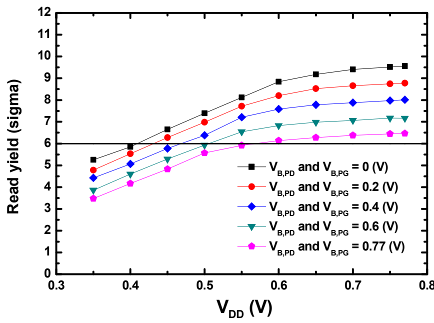


Figure 9. The read yield estimations in SD mode at different $V_{B,PD}$'s and $V_{B,PG}$'s.

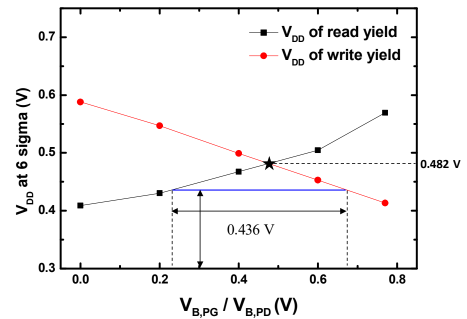


Figure 12. V_{DD} at 6 sigma in SD mode at different $V_{B,PD}$'s and $V_{B,PG}$'s.

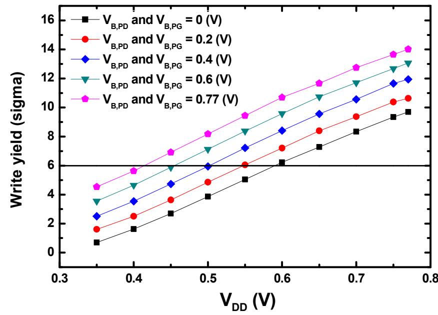


Figure 10. The write yield estimations in SD mode at different $V_{B,PD}$'s and $V_{B,PG}$'s.

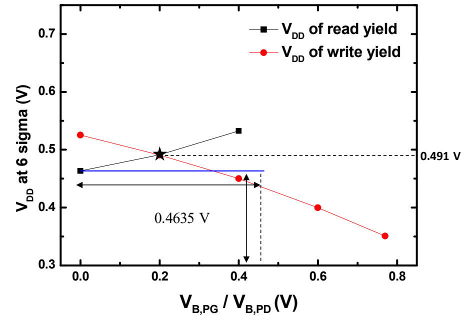


Figure 13. V_{DD} at 6 sigma in HP mode at different $V_{B,PD}$'s and $V_{B,PG}$'s.

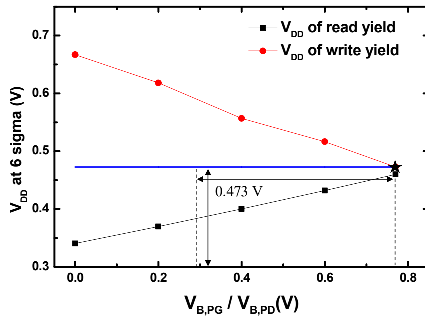


Figure 11. V_{DD} at 6 sigma in LV mode at different $V_{B,PD}$'s and $V_{B,PG}$'s.

Table 1. The back bias combinations of the three modes.

	LV	SD	HP
$V_{B,PU}$ (V)	0	0.37	0.77
$V_{B,PG}$ (V)	0~0.77	0~0.77	0~0.77
$V_{B,PD}$ (V)	0~0.77	0~0.77	0~0.77

Table 2. The V_{DD}'s at 6 sigma at different $V_{B,PG}$'s ($V_{B,PD}$'s) in SD mode.

	$V_{B,PG}$ = 0 (V)	$V_{B,PG}$ = 0.2 (V)	$V_{B,PG}$ = 0.4 (V)	$V_{B,PG}$ = 0.6 (V)	$V_{B,PG}$ = 0.77 (V)
Read	0.409	0.430	0.467	0.505	0.569
Write	0.588	0.547	0.499	0.453	0.413

Table 3. The V_{DD} at 6 sigma at different $V_{B,PG}$'s ($V_{B,PD}$'s) in LV mode.

	$V_{B,PG}$ = 0 (V)	$V_{B,PG}$ = 0.2 (V)	$V_{B,PG}$ = 0.4 (V)	$V_{B,PG}$ = 0.6 (V)	$V_{B,PG}$ = 0.77 (V)
Read	0.341	0.370	0.400	0.432	0.460
Write	0.667	0.618	0.557	0.516	0.473

Table 4. The V_{DD}'s at 6 sigma at different $V_{B,PG}$'s ($V_{B,PD}$'s) in HP mode.

	$V_{B,PG}$ = 0 (V)	$V_{B,PG}$ = 0.2 (V)	$V_{B,PG}$ = 0.4 (V)	$V_{B,PG}$ = 0.6 (V)	$V_{B,PG}$ = 0.77 (V)
Read	0.464	0.491	0.532	N/A	N/A
Write	0.526	0.491	0.450	0.400	0.351

Table 5. The minimum V_{min}'s in dynamic design for the three modes.

	LV	SD	HP
$V_{B,PU}$ (V)	0	0.37	0.77
$V_{B,PG}$ / $V_{B,PD}$ (V)	0.770	0.233~0.668	0~0.334
V_{min} (V)	0.473	0.436	0.464

Table 6. The minimum V_{min}'s at a fixed $V_{B,PG}$ ($V_{B,PD}$) for the three modes.

	LV	SD	HP
$V_{B,PU}$ (V)	0	0.37	0.77
$V_{B,PG}$ / $V_{B,PD}$ (V)	0.770	0.476	0.200
V_{min} (V)	0.473	0.482	0.491