On the Write Energy of Non-Volatile Resistive Crossbar Arrays With Selectors

Albert Ciprut, Eby G. Friedman
University of Rochester, Rochester, NY USA
E-mail: aciprut@ur.rochester.edu

Abstract

Crossbar arrays based on non-volatile resistive devices such as resistive RAM and phase change memory have become an important technology due to the applications to memory systems. The energy consumption of integrated circuits has become a primary issue due to thermal constraints in high performance systems and limited battery time in mobile and IoT applications. In this paper, the energy efficiency of a crossbar array of a one-selector-one-resistor (1S1R) configuration during a write operation is explored for the $V/2$ and $V/3$ bias schemes. The characteristics that affect the most energy efficient bias scheme are demystified. The write energy of a crossbar array is modeled in terms of the array size, number of selected cells, and the nonlinearity factor. For a specific array size and selector technology, the number of selected cells during a write operation can affect the choice of bias scheme. Moreover, the effect of leakage current due to partially biased unselected cells is explored.

Keywords

Crossbar array, non-volatile, resistive memory, RRAM, bias scheme, write energy, selector, nonlinearity factor

1. Introduction

The energy consumption of integrated circuits (ICs) has typically been limited by the thermal design power (TDP) envelope of high performance microprocessors and the battery size of mobile devices. It is therefore crucial to enhance energy efficiency to improve robustness and mobility. In particular, the write energy of a resistive crossbar array dissipates significant energy [1]. Non-volatile resistive crossbar arrays such as resistive random access memory (RRAM) and phase change memory (PCM) have gained importance in memory applications due to the scalability, non-volatility, and small area while providing CMOS compatibility [2]— [4]. The area of a cell for an RRAM crossbar array can be as small as $4F^2$, where F is the minimum feature size of a technology node [5]. These arrays can be placed within the metal layers, supporting cell placement above the CMOS logic, further reducing area. Moreover, a crossbar array can be configured as a logic gate, providing a path to non-von Neumann in-memory computing [6]. To enable this capability, however, the energy consumption of a crossbar array should be within practical limits.

The energy consumption of a crossbar array during a write operation depends upon the bias scheme, typically a $V/2$ or $V/3$ bias scheme [7], [8] (see Section 2). While most of the work described in the literature considers the $V/2$ bias scheme [1], [9], the advantages of one bias scheme over the other are not clear in terms of energy efficiency. Furthermore, the $V/2$ scheme is often claimed to be a more energy efficient bias scheme then the $V/3$ bias scheme [2], [10]. In this paper, the write bias schemes are compared from an energy efficiency point of view for 1S1R crossbar arrays with bipolar selectors. It is shown here that the bias scheme that provides the highest energy efficiency depends upon several parameters such as the nonlinearity factor of the selectors, size of the array, and number of selected cells during a write operation. Simple closed-form expressions that model the write energy of an array in terms of these parameters are provided for the case when the interconnect resistance is negligible. It is important to note that most of the existing work described in the literature does not consider the implications of multibit operation on the energy consumption of an array. In [1] and [9], the power consumption for multibit operation is considered; however, only for the $V/2$ bias scheme. In this work, the effects of multibit operation on the energy efficiency of different bias schemes are explored for the first time. Moreover, the effects of leakage current on energy consumption are discussed. In Section 2, the bias schemes during a write operation are reviewed. In Section 3, models of the energy consumption are described. In Section 4, some conclusions are offered.

2. Write Operations

The two types of write bias schemes, $V/2$ and $V/3$, are shown in Fig. 1.

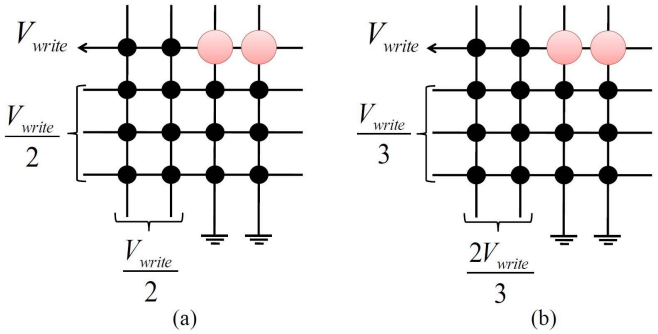

Figure 1: Bias schemes for a two bit write operation, (a) $V/2$ bias scheme, and (b) $V/3$ bias scheme.

For the $V/2$ bias scheme, the selected wordline is connected to the write voltage while the selected bitlines are grounded. The unselected wordlines as well as bitlines are biased to half of the write voltage. Similarly, for the $V/3$ bias scheme, the selected wordline is connected to the write voltage while the selected bitlines are grounded. The unselected wordlines are biased at one third of the write voltage whereas the unselected bitlines are biased at two thirds of the write voltage. The voltage drop across the unselected cells along the selected wordline and selected bitlines, also called the half-selected cells, are therefore biased at one half of the write voltage for the $V/2$ bias scheme. For the $V/3$ bias scheme, this voltage

decreases to one third of the write voltage. More importantly, the cells on the unselected wordlines and bitlines are at zero voltage for the $V/2$ bias scheme and at one third of the write voltage for the $V/3$ bias scheme, resulting in a large number of cells leaking current when the $V/3$ bias scheme is applied.

The leakage current of the unselected cells depends upon the nonlinearity factor of the selector. The bipolar selector is placed above a resistive cell to form a nonlinear I-V characteristic. A selector with higher nonlinearity factor further decreases the current of the cell when biased below the threshold voltage of the selector [11]. The leakage current due to the partially biased unselected cells can therefore be suppressed, decreasing the IR drops and supporting larger array sizes [12]. The nonlinearity factor of a selector is the ratio of the current passing through a selected cell to the current passing through a half-selected cell. The nonlinearity factor of the $V/2$ and $V/3$ bias schemes are, respectively,

$$K_{V/2} = \frac{I_{cell}(V_{write})}{I_{cell}(V_{write}/2)} = 2 \times \frac{R_{on@V_{write}/2}}{R_{on}}, \quad (1)$$

$$K_{V/3} = \frac{I_{cell}(V_{write})}{I_{cell}(V_{write}/3)} = 3 \times \frac{R_{on@V_{write}/3}}{R_{on}}, \quad (2)$$

where $I_{cell}(V_{write})$, $I_{cell}(V_{write}/2)$, and $I_{cell}(V_{write}/3)$ are, respectively, the current passing through the cell when the cell voltage is equal to the write voltage, one half of the write voltage, and one third of the write voltage, R_{on}, $R_{on@V_{write}/2}$, and $R_{on@V_{write}/3}$ are, respectively, the cell resistance during an on-state when the cell voltage is equal to the write voltage, one half of the write voltage, and one third of the write voltage. The leakage current therefore depends upon the bias scheme which is related to the nonlinearity factor. The nonlinearity factor $K_{V/3}$ of a one-selector-one-resistor (1S1R) device is typically on the order of 10^3 to 10^4, whereas $K_{V/2}$ is below 10^2 [11], [13]— [17]. The choice of bias scheme can therefore greatly affect the energy consumption.

3. Energy Models

In this section, a model of the energy consumption of the $V/2$ and $V/3$ bias schemes is provided, demonstrating, in Section 3.1., the use as a design guideline for choosing the proper bias scheme. Moreover, the effect of the nonlinearity factor on the choice of bias scheme is explored in Section 3.2. The impact of the leakage current on the total energy consumption is explored in Section 3.3.

To provide an intuitive closed-form expression that models the energy consumption of a crossbar array, the interconnect resistance is assumed to be negligibly small. Although this assumption is not always practical in large arrays, it permits the effects of the critical parameters on the energy consumption such as the nonlinearity factor, size of the array, number of selected cells, and bias scheme to be captured while retaining simplicity and providing intuitive expressions. An array with an equal number of rows and columns is considered. The selected devices are modeled based on VTEAM [18] considering linear switching, and the remaining devices are modeled as resistors. The switching devices are considered to be symmetric with equal on/off threshold voltages and equal set/reset times. Based on these considerations, the energy consumption of a crossbar array for the $V/2$ and $V/3$ bias schemes are, respectively,

$$E_{V/2} = V_{write} \frac{I_{on}}{K_{V/2}} \frac{(Nn + N - 2n)}{2} t_{sw} + nE_{sw}, \quad (3)$$

$$E_{V/3} = V_{write} \frac{I_{on}}{K_{V/3}} \frac{(N^2 - n)}{3} t_{sw} + nE_{sw}, \quad (4)$$

where V_{write} is the write voltage, I_{on} is the cell current when biased at the write voltage during the on state, N is the number of rows and columns, n is the number of selected cells, t_{sw} is the switching time, and E_{sw} is the switching energy consumption of the selected device,

$$E_{sw} = \frac{V_{write}^2}{R_{off} - R_{on}} \ln\left(\frac{R_{off}}{R_{on}}\right) t_{sw}. \quad (5)$$

R_{on} and R_{off} are, respectively, the cell resistance during the on and off states. Note that the second term in (3) and (4) are the switching portion of the total energy consumption due to switching the selected cells whereas the first term is due to the leakage current of the half-selected and unselected cells.

The closed-form expressions are in good agreement with SPICE, exhibiting an average error of 0.28% and a maximum error of 4.5%, as shown in Fig. 2.

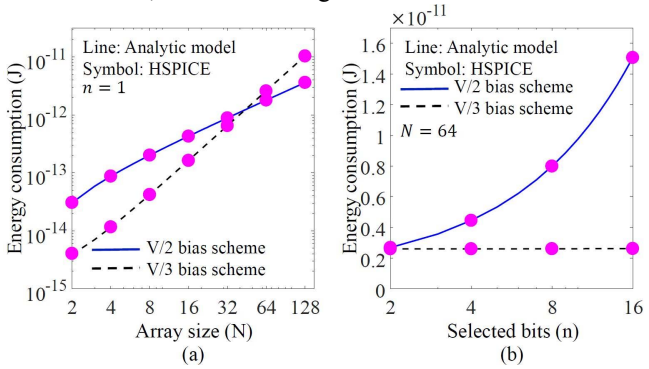

Figure 2: Energy consumption of a crossbar array with respect to (a) array size, and (b) number of selected cells, assuming $R_{on} = 10^4\ \Omega$, $R_{off} = 10^7\ \Omega$, $K_{V/2} = 10$, and $K_{V/3} = 150$.

The energy consumption scales differently with respect to the array size for different bias schemes. The $V/2$ bias scheme follows a linear trend whereas the $V/3$ bias scheme scales superlinearly with array size ($\sim N^2$). Moreover, while the energy consumption for the $V/2$ bias scheme is strongly dependent on the number of selected cells, the $V/3$ bias scheme is constant for large arrays ($N \gg n$). The effect of n on the energy consumption for different array sizes is illustrated in Fig. 3. The increasing number of selected bits per write operation significantly adds to the energy consumption of the $V/2$ bias scheme. The $V/3$ bias scheme remains relatively constant for large array sizes. This

behavior is due to the increasing number of half-selected cells for the $V/2$ bias scheme with increasing n. In contrast, for the $V/3$ bias scheme, the variation in the number of unselected cells become negligible as n increases if the size of the array N is much larger than n.

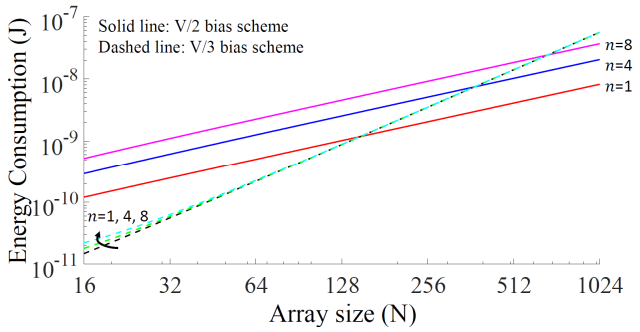

Figure 3: Effect of the number of selected cells on the energy consumption of a crossbar array for the $V/2$ and $V/3$ bias schemes, assuming $R_{on} = 10^4\ \Omega$, $R_{off} = 10^7\ \Omega$, $K_{V/2} = 20$, and $K_{V/3} = 1{,}000$.

One method to decrease the energy consumption is by using selectors with higher nonlinearity factors. A higher nonlinearity factor decreases the leakage current of the unselected cells, improving the ability of the selector to isolate the switching cell from the rest of the unselected array. The effect of the nonlinearity factor on the energy consumption is shown in Fig. 4.

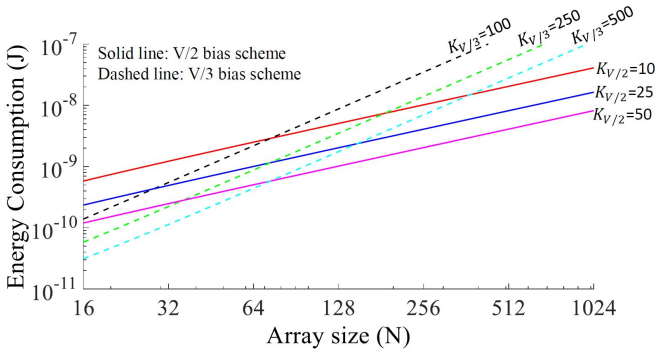

Figure 4: Effect of the nonlinearity factor on the energy consumption of a crossbar array for the $V/2$ and $V/3$ bias schemes, assuming $R_{on} = 10^4\ \Omega$, $R_{off} = 10^7\ \Omega$, and $n = 4$.

Note that with increasing nonlinearity factor, the energy consumed during both bias schemes decreases since (3) and (4) are, respectively, inversely proportional to $K_{V/2}$ and $K_{V/3}$.

3.1. Energy Efficient Bias Scheme

Depending upon the array size, one bias scheme is more efficient than the other bias scheme. The number of selected cells during a write operation may however alter the most energy efficient bias scheme, as shown in Fig. 5. Note that the line of intersection between the two bias schemes (where $E_{V/2}$=$E_{V/3}$) spans a range of array sizes (N =128, 256 and 512) depending upon the number of selected bits. Since the $V/2$ bias scheme scales with the number of selected cells as opposed to the $V/3$ bias scheme which remains relatively constant, the line of intersection bends for different values of n.

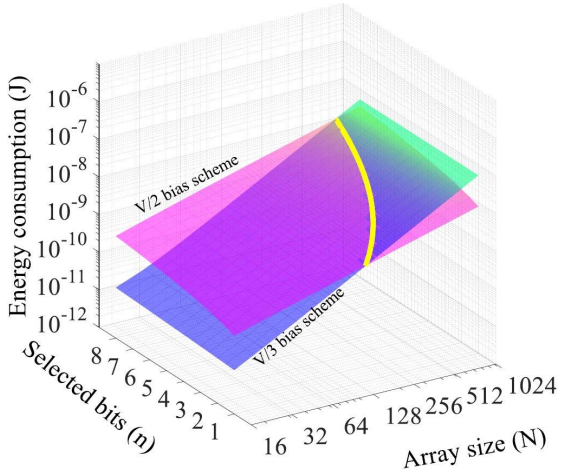

Figure 5: Comparison of the energy consumption in terms of the array size and number of selected cells for the $V/2$ and $V/3$ bias schemes, assuming $R_{on} = 10^4\ \Omega$, $R_{off} = 10^7\ \Omega$, $K_{V/2} = 20$, and $K_{V/3} = 1{,}000$, $V_{write} = 4$ volts, and $t_{sw} = 100\ ns$.

The extra energy due to an incorrect choice of bias scheme can waste significant power during a write operation. The ratio of the energy consumption between the two bias schemes is shown in Fig. 6.

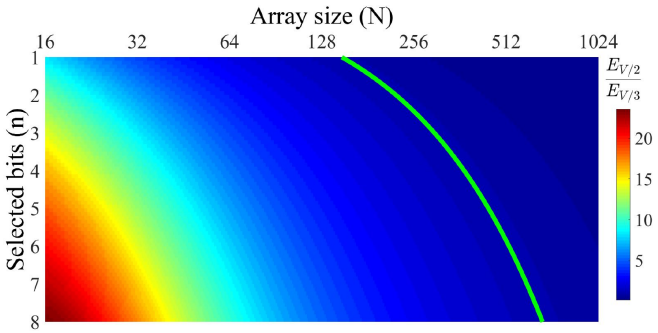

Figure 6: Energy savings of the $V/3$ bias scheme as compared to the $V/2$ bias scheme assuming the same parameters listed in Fig. 5. The solid line is the contour where the energy consumption between the two bias schemes is equal.

The right side of the contour is the region where the $V/2$ bias scheme is more efficient than the $V/3$ bias scheme, and the left side is where the $V/3$ bias scheme is more efficient than the $V/2$ bias scheme. Since increasing the number of selected cells consumes more energy for the $V/2$ bias scheme for low n, the $V/2$ bias scheme remains more energy efficient over a wider range of array sizes. In contrast, for high n, the $V/3$ bias scheme is more energy efficient over a wider range of array sizes. The write energy can be as much as 5x lower for a 128 x 128 array and 10x lower for a 64 x 64 array using the $V/3$ bias scheme with eight selected bits. For large arrays, however, since the number of cells leaking current during the $V/3$ bias scheme scales with N^2, the $V/2$ bias scheme can

consume as much as 7x lower energy for an array size of 1024 x 1024 with single bit operation.

The interconnect resistance changes the location of the contour (see Fig. 6) where the energy for both bias schemes is equal. Since the leakage current due to the half-selected cells for the $V/2$ bias scheme is significantly greater than the leakage current through the cells biased at one third of the write voltage, the IR drops are greater for the $V/2$ bias scheme [12]. Thus, the voltage drop across the selected cells for the $V/2$ bias scheme is smaller as compared to the $V/3$ bias scheme. The switching time of the selected cells for the $V/2$ bias scheme is therefore longer, increasing the energy consumption [18] and resulting in the $V/3$ bias being more energy efficient. This effect is more pronounced with larger IR drops, resulting in slower switching times.

3.2. Impact of Nonlinearity Factor

The bias scheme affects the total leakage current due to the difference between the nonlinearity factors and the number of leaking cells. While the size of the array as well as the number of selected bits affect the choice of energy efficient bias scheme, the difference between the nonlinearity factors ($K_{V/2}$ and $K_{V/3}$) determines the range of N and n at which the two energy consumptions, $E_{V/2}$ and $E_{V/3}$, become equal. For instance, if one nonlinearity factor is much greater than the other nonlinearity factor, the bias scheme that provides the higher nonlinearity factor will be the most energy efficient bias scheme for a wide range of N and n. By setting $E_{V/2}$ and $E_{V/3}$ equal, the ratio of the two nonlinearity factors, $K_{V/2}$ and $K_{V/3}$, is a function of the array size and number of selected cells. Based on this equality, for the $V/3$ bias scheme to be more energy efficient than the $V/2$ bias scheme, the following condition must be satisfied,

$$\frac{K_{V/3}}{K_{V/2}} \geq \frac{2}{3}\frac{N^2 - n}{Nn + N - 2n}. \qquad (6)$$

Note that for negligible parasitic interconnect resistance, (6) is a function of the size of the array and number of selected cells. The variation of $K_{V/3}$ to satisfy (6) is shown in Fig. 7.

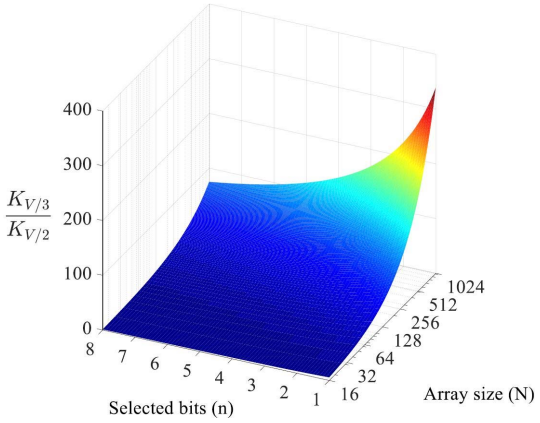

Figure 7: Ratio of the nonlinearity factors $K_{V/3}$ to $K_{V/2}$ to maintain equal energy consumption for the $V/2$ and $V/3$ bias schemes in terms of the array size and number of selected cells.

The $V/3$ bias scheme is more energy efficient if $K_{V/3}$ is at least two orders of magnitude greater than $K_{V/2}$ for array sizes up to 1024 x 1024 with six selected bits or an array size up to 256 x 256 with a single selected bit.

3.3. Write Pulse Width

The pulse width to successfully program the selected cells depends upon the switching time of the cells. While shorter pulses may produce write failures, extended pulse widths may consume excessive power, degrading the energy efficiency. Due to the significance of the leakage current of the unselected cells, it is crucial to accurately set the pulse width with high precision. For large arrays, the leakage current portion of the total energy dominates, making the switching energy E_{sw} negligible, as shown in Fig. 8.

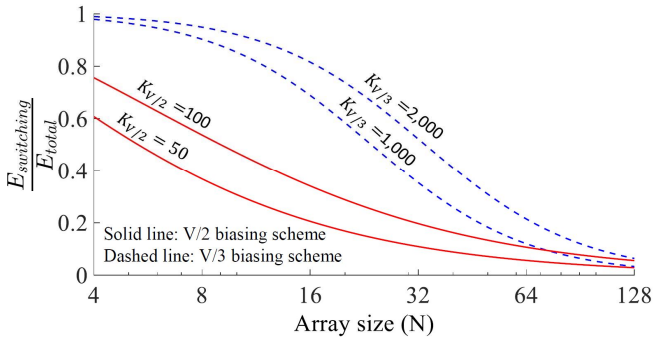

Figure 8: Ratio of the switching energy to the total energy in terms of the array size, $R_{on} = 10^4\ \Omega$, $R_{off} = 10^6\ \Omega$, n =4, $V_{write} = 4$ volts, and $t_{sw} = 100\ ns$.

Note that the switching energy for the $V/3$ bias scheme is a larger portion of the total energy as compared to the $V/2$ bias scheme. This difference is due to the smaller leakage current for the $V/3$ bias scheme due to the larger nonlinearity factor, $K_{V/3}$. Similarly, a higher nonlinearity factor reduces the leakage energy, resulting in the switching energy being more pronounced and exhibiting greater energy efficiency. The switching energy is less than 10% of the total energy for array sizes exceeding $N = 128$.

To lower the energy due to leakage currents, the pulse width is set as precisely as possible, sufficient to switch the selected cells. This excess energy due to leakage currents requires write termination circuitry to isolate the write voltage from the array once successful switching is achieved. While write termination techniques have been adopted for resistive cells based on STT-MRAM due to the stochastic nature of switching [19], a similar approach in RRAM based 1S1R crossbar arrays can be useful to save energy since an over extended write pulse can significantly reduce the energy efficiency due to the large leakage current.

4. Conclusions

The energy consumption of a 1S1R crossbar array for two bias schemes, $V/2$ and $V/3$, for optimal energy efficiency is discussed. Intuitive closed-form expressions that model the

energy consumption in terms of the nonlinearity factor, size of the array, and number of selected cells, assuming negligible interconnect resistance, are presented. The most energy efficient bias scheme depends upon the size of the array as well as the number of selected cells during a write operation. The energy consumed during both bias schemes scales differently. The $V/2$ bias scheme is more energy efficient for large arrays. As the number of selected cells increases, however, the $V/3$ bias scheme achieves greater energy efficiency. The $V/3$ bias scheme provides higher efficiency, decreasing the energy consumption by an order of magnitude for a 64 x 64 array with eight selected cells. As the array size increases and the number of selected cells decreases, the energy benefits of the $V/3$ bias scheme diminish. For the $V/3$ bias scheme to be as energy efficient as the $V/2$ bias scheme for large arrays ($N > 128$), $K_{V/3}$ should be two orders of magnitude greater than $K_{V/2}$. The appropriate choice of bias scheme can save an order of magnitude of energy. A higher nonlinearity factor significantly decreases the energy consumption by suppressing leakage currents within the half-selected and unselected cells. The switching energy is a negligible portion of the total energy for large arrays ($N > 128$). To prevent excess energy consumption due to leakage currents, write termination circuitry is needed to prevent over extended write pulses. Future work will focus on integrating the interconnect resistance into the energy models to capture the effects of IR drops on the switching time of the selected cells and the energy consumption of the crossbar array.

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