A Modified Method of Logical Effort for FinFET Circuits Considering Impact of Fin-Extension Effects

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Abstract

For the transistor sizing of multistage digital circuits with predictable delays, the relationship between the effective input capacitances of all the stages and the stage size ratios must be known. Effective capacitances of the FinFET logic gates are strongly dependent on transition times at their input-output nodes and are, therefore, not directly proportional to the stage size, as opposed to conventional transistors. Due to this, the methods developed for transistor sizing of planar logic circuits are not valid for FinFET logic circuits. Though this effect is not present in highly gate-drain overlapped FinFET devices, their performance is highly compromised (higher power consumption and larger delay).We propose a modification of the existing logical effort based delay model for FinFET inverter chain that considers the above-mentioned characteristics of FinFET devices. We also discuss branching loads and transistor sizing of non-critical paths in this paper. We observe that our FinFET sizing scheme leads to a significant reduction in inverter chain delays. We observe that error in estimation of delay (not considering the transition time dependency) in a two stage FO4 inverter chain is 31.8% and 15.3% respectively (from mixed-mode TCAD simulations).

Keywords

delay, FinFET, FinFET inverter chain, logical effort, transition time

1. Introduction

FinFETs are replacing planar MOSFETs since they suppress short channel effects due to their higher gate control over the channel, and also due to their relatively planar compatible process technology[1], [2]. Sizing of FinFET logic cells is a challenging issue due to the discretized device width and anomalous behavior of terminal capacitances[3]. The method of Logical Effort (LE) is a simple way to decrease the simulation based trial and error, early in the design flow by specifying the appropriate number of stages and the transistor sizes for the logic gates in a path to achieve minimum delay [4].An extension of the LE method for FinFET circuits is given by [3]in all of the sub-threshold, near-threshold, and super-threshold regimes. However, they assume that the effective capacitances are directly proportional to the number of fins connected in parallel(A large width FinFET is realized by using multiple fins in parallel [5]). However, it has been reported that the effective input capacitance of a FinFET logic gate is not a function of the Number of Fins (NF) alone; It is a strong function of the gate's terminal transitions due to fin extension effects [6]. In order to apply circuit design methods such as LE, the relationships of a logic gate's effective input capacitance and gate size must be known. The effective capacitance and resistance of a FinFET device are strongly influenced by the parasitics of its extension regions. An incorrect estimation of parasitics and effective capacitances causes inaccurate estimation of delay[7].

Effective terminal capacitances of a FinFET logic gate are highly dependent on transition times at its input-output nodes due to a strong gate controlled modulation of the carrier concentration in the low doped parts of the fin extension. The part of the outer fringing capacitance originating from the gate fringing field lines that terminate in the low doped region of the extension is thus transition time dependent[6].This fin-extension effect (bias dependent fin-extension capacitances) must be captured in FinFET logic gate delay models and in circuit design methodologies. In the sub/near-threshold region, an empirical model for gate sizing of FinFET circuits was developed in [8]by specifying the drain current as a Look-Up-Table (LUT) function of terminal voltages. A delay optimization framework for discrete gate sizing of FinFET circuits is also proposed in [8]. It is assumed in [8] that the output load capacitance is given in terms of the number of fins of the output (fan-out) stage of a gate. However, the dependence of the terminal capacitances on terminal voltages due to the fin-extension effect is not yet captured. Thus, an output capacitance is not known in terms of NF, as required in the approach of [8]. A circuit design/sizing method would be useful if it can lead to a given load capacitance being driven with minimum delay. A transistor sizing methodology based on FinFET's Number of Fins (NF) therefore needs an NF-Capacitance relation which takes terminal transition times into account. This is important because the dependence of effective capacitances on transition times and driver-load size ratio originating from the fin-extension effect is significant, as explained in [9].

An empirical Current Source Model (CSM) based logic cell modeling method given by [10] develops an analogous model for each logic gate using independent current sources and equivalent capacitances, the values of which are pre-described for various combinations of input-output voltages and stored in CSM LUTs. The output waveforms are also characterized w.r.t given input voltage waveforms using pre-described LUTs. A linear curve fitting was carried out in order to relate the driving currents and parasitic capacitances to different node voltage levels and fitting parameters were stored in LUTs[10]. However, it was assumed that the influence of bias voltage on parasitic capacitances is comparatively lesser than that on the driving current. In addition, this LUT based approach lacks physical insights and

require computational resources for usage. This approach can't also be used to predict the optimum sizes (NFs) of FinFETs in a multi-stage logic circuit; it can only be used to predict the delays once the sizes are affixed. Therefore, an efficient FinFET circuit design calls for adaptation of a physics based delay estimation method, after taking cognizance of the issues with fin-extension effect. This method should also let us estimate the sizes of FinFET logic gates for minimizing delays.

We organize the rest of our paper as follows: in Section II we describe the simulation setup. In Section III, we introduce logical effort model extension for sizing FinFET circuits considering the transition time dependency of effective capacitances. In section IV, we verify the assertions of logical effort model and finally in Section V, we conclude the paper.

2. Simulation setup

This work is done using 2-D Sentaurus TCAD [11] mixed-mode simulations and its equivalent Verilog-A model based SPICE simulations. Appropriate physical models to account for the ionized impurity scattering, carrier-carrier scattering, the effect of lateral and perpendicular field dependence of carrier mobility, velocity saturation, non-local field effects and carrier quantization effects [11] are used in our TCAD simulation setup. We calibrate our TCAD simulation setup by matching the device I-V characteristics with the measured results in Fig. 1(a) [6]. The device threshold voltages (V_{th}) are matched with ITRS 2013 [12]by tuning the gate work function. Table I shows the device and technology parameters. Drive currents are consistent with earlier reported data[13]. We find in Fig. 1(b) that the carrier concentration of our 2D device matches well with that obtained for different cross-sections of fin height of a 3D device. Therefore, we use 2D simulations without sacrificing the accuracy. Doping of the S/D pads is constant ($2\times10^{20}cm^{-3}$) with Gaussian doping profiles in the source/drain (S/D) extension with a doping gradient σ_L (3nm/decade). We calibrate our LUT based Verilog-A model by matching the device I-V characteristics with TCAD results as shown in Fig. 1(c).

3. A Modified Method of Logical effort for sizing FinFET circuits

The input/parasitic capacitances of a FinFET logic gate (or inverter) are strong functions of its input transition time and fan-out (FO) load, as shown in Fig. 2(a) and Fig. 2(b). To avoid this, which is being caused by fin-extension effect, several researchers use a highly gate overlapped FinFET device structure such as in [14, 15]. However, the latter device architecture (doping density of source-drain pad, fin extension regions and channel as 2e20 cm^{-3}, 1e20 cm^{-3} and 1e17 cm^{-3} respectively, as reported in [16]) leads to an increase of 19% in the delay of a two stage inverter chain, as discussed in [14]. In this section, we develop a modified method of LE which considers the effects shown in Fig. 2(a) and Fig. 2(b) while not compromising speed by using a highly overlapped device architecture.

In the classical (planar CMOS) method of LE, the delay of a logic gate is a linear function of the ratio of its output capacitance C_{out} and input capacitance C_{in}, provided the ratio of input and output transition times is kept constant. The coefficients of this linear function are technology dependent constants. This leads to a conclusion that the delay of an inverter chain is minimized when C_{out}/C_{in} of all the stages is equal [4]. However, the effective values of input and output terminal capacitances are variable with C_{out}/C_{in} itself in a FinFET inverter chain, as discussed in [9] and shown in Fig. 2.

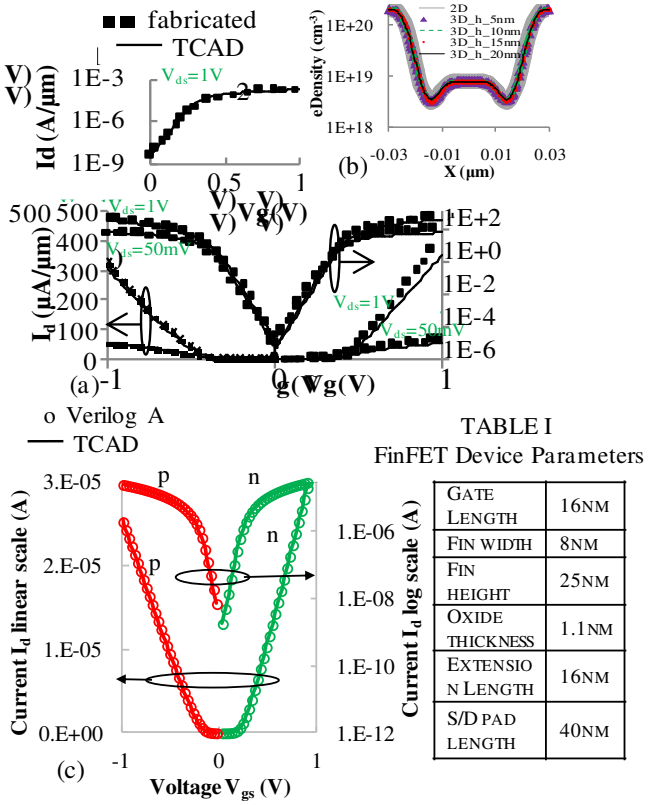

Figure 1: (a) Calibration of TCAD models with experimental data at L_G=75nm and (inset) for L_G=25nm[6]. (b) eDensity along the channel and Fin at different cross-sections of fin height of a 3D device (V_g=0.6V, V_d=0V). (c) Calibration of our Verilog A model by matching the device I-V characteristics with TCAD data.

TABLE I
FinFET Device Parameters

Gate Length	16nm
Fin width	8nm
Fin height	25nm
Oxide thickness	1.1nm
Extension Length	16nm
S/D pad length	40nm

Therefore, the classical method of LE is not directly applicable to FinFET circuits. However, we observe that the delay versus NF ratio (stage ratio ρ) of two consecutive stages (NF_n/NF_{n-1}) is a straight line (Fig. 3(a)) when the ratio of input and output transition times is kept constant (Eqn. (1)).

$$d = g\left(\frac{NF_n}{NF_{n-1}}\right) + p_{inv} \quad (1)$$

This can be explained as follows, by considering the Extension Transistor Induced Capacitance Shielding phenomenon (ETICS[1]) due to the fin-extension effect: The effective input and output capacitances of a FinFET logic gate are dependent on transition times of their terminal voltages Fig. 2(c-d) unlike the conventional transistors. Effective input

[1]ETICS is explained in [6]as: The FinFET Drain Extension's (DE's) electron density is a strong function of the inverter's input and output voltage values. Therefore, the inverter's input and parasitic (output node) capacitances are determined by the extent to which it's input and output transitions "overlap" with a high DE electron density.

and output capacitances of a FinFET logic gate are functions of gate size (*NF*) and the crossover point of input and output voltage transitions. This crossover point remains constant for a given ratio of input and output transition times. This is because the increase in output discharge for a given increment in input voltage would be balanced by an in increase in total output capacitance which is proportional to the transition time. For a given ratio of input and output transition times, there is a one-to-one correspondence between the values of input and output voltages (Please refer to Fig. 3(b), ratio of input and

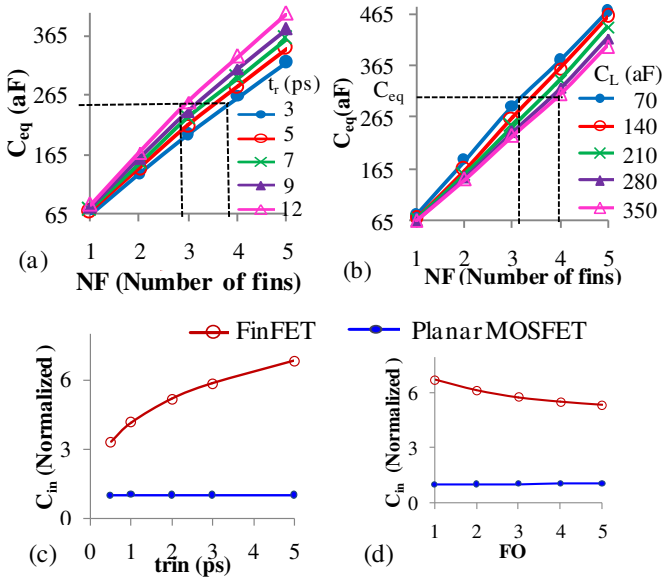

Figure 2: Relation between the equivalent input capacitance of a FinFET inverter and the size of the inverter (number of fins *NF*) for (a) different transition times at the input and, (b) different FO loads C_L at the output obtained using 2D Sentaurus TCAD mixed-mode simulations. (c) Variation of effective input capacitance of FinFET/Planar MOSFET inverter with input transition time (for FO1) and (d) FO (for t_{rin}=5ps).

output transition times remains constant (0.66) with stage ratio (*NF* ratio)). Therefore, from the explanation of ETICS in [6], we surmise that the input and parasitic capacitances of a FinFET inverter would not change if the ratio of input and output transition times ($t_r$out/$t_f$in) is kept constant while changing the FO load. In other words, if $t_r$out/$t_f$in is kept constant, the input capacitance of a stage is proportional to its size (*NF*).Hence, all the conclusions and the method of LE are valid for FinFET circuit design if the stage and total electrical efforts are defined in terms of the *NF* ratio of stages (these "efforts" are defined in [4]) and capturing the ETICS effect in the "electrical effort" component of the basic LE model. As we explain further in this paper, this can be accomplished if the final load capacitance to be driven could be expressed in terms of an equivalent number of fins.

In the conventional method of LE [4], it is assumed that the values of all the rising and falling transition times are equal (t_r = t_f) throughout the inverter chain. However, in case of FinFETs, matching the drive strength of n and p devices, as explained in [17], is usually not possible due to the discretization of the device width. Therefore, for a FinFET inverter chain (Fig. 4) with its n and p devices having different drive strengths, we get unique values of t_r and t_f if we keep stage ratio constant (Table II). Logical effort delay model based method considering unequal rising and falling input voltage transitions to minimize total average delay of the inverter chain for a FinFET inverter as the final load with a number of fins NF_n is similar to the formulation of the classical LE of [4].For rising (falling) input transitions, the total delay of the inverter chain is denoted as D_r (D_f).The total average delay (D_r+D_f)/2 is minimized when the stage ratio $\frac{NF_m}{NF_{m-1}}$ of each stage is equal[4].For rising (falling) input transitions, the average delay D_r (D_f) of the inverter chain is (derived using an approach similar to [4]:

$$\frac{(D_r+D_f)}{2} = \frac{1}{2}\left[\left(\frac{NF_2}{NF_1}\right)(\tau_r+\tau_f) + \left(\frac{NF_3}{NF_2}\right)(\tau_r+\tau_f) + \left(\frac{NF_4}{NF_3}\right)(\tau_r+\tau_f) + \cdots + \left(\frac{NF_m}{NF_{m-1}}\right)(\tau_r+\tau_f) + \cdots + \left(\frac{NF_n}{NF_{n-1}}\right)(\tau_r+\tau_f) + \sum_1^n (P_r + P_f)\right] \quad (2)$$

Where, τ_r and τ_f are slopes of Fig. 3(a) for input rising and falling transitions, respectively. The symbol P_r and P_f denote the inverter's parasitic delay for input rising and falling cases, respectively, which are the corresponding Y-intercepts in Fig. 3(a). Here, D_r and D_f could be unequal due to unequal drive strengths of n and p devices.

Here, the product of all the terms $\prod_{m=1}^{m=n}\left(\frac{NF_m}{NF_{m-1}}\right)(\tau_r+\tau_f)$ is constant and $\sum_{m=1}^{m=n}\left(\frac{NF_m}{NF_{m-1}}\right)(\tau_r+\tau_f)$needs to be minimized, which is similar to the formulation of the classical LE of [4]. Therefore, the total average delay$(D_r + D_f)/2$ is minimized when the stage ratio $\frac{NF_m}{NF_{m-1}}$ of each stage is equal. We will verify this in later subsections using TCAD simulations.

The entire logical effort formulation described above (Eqn. 2) is based on the number of fins NF_n of the load stage. Whereas, the buffer's load could, in general, be specified in terms of the capacitance C_L. Further, in this section, we discuss our method to find an equivalent NF_n for a given C_L while considering the transition time dependence of the input capacitance of an inverter with an equivalent NF_n. The main challenge with this is to determine for a given load C_L the corresponding inverter NF_n, while ensuring that both have an equal (input) transition time.

As discussed earlier in this paper, the stage ratio needs to be constant in a chain for minimum delay. For a given constant stage ratio, the rising and falling transition times are unique throughout the chain as shown in table II. For a constant stage ratio, each stage finds an effective load capacitance proportional to the stage's size due to the unique in-out crossover point as discussed earlier in this section using Fig. 3(b) (because of the one-to-one correspondence of an inverter's input and output voltage transitions for when $t_r$out/$t_f$in is kept constant). Hence, a given voltage transition at the input of every stage of the inverter chain produces a unique voltage transition at the output. In other words, a constant stage ratio ensures a constant ratio of effective load capacitance to drive strength for each stage.

For the sizing of an inverter chain with a given stage ratio, we first find the values of unique transition time (t_r (t_f)) for rising (falling) input. For this, we design a mixed-mode TCAD experiment of a three stage inverter chain Fig. 5(a). Varying

the rising transition time ($t_r$in) at the input of the inverter Inv_2, we get a relation between $t_f$out and $t_r$in as shown in Fig. 5(c). Similarly, varying the falling transition time ($t_f$in) at the input of the inverter, we get a relation between $t_r$out and $t_f$in. The intersection of these two curves when plotted as in Fig. 6(a) would give the unique transition times for a given stage ratio. To get a realistic input transition (not an ideal ramp) we vary the input transition of the Inv_2 by varying the ramp input of the Inv_1. For a given stage ratio, the elements of the set (t_f, t_r) thus obtained, are the unique transition times in the inverter chain, and are functions of only the stage ratio (*NF* ratio).

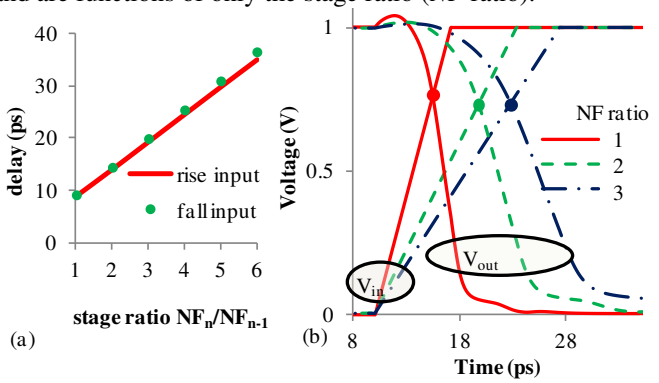

Figure 3: (a) Relation of the total delay of a three stage inverter chain with stage ratio (b) Input and output voltage transitions of Inv_1 of Fig. 4 for various *NF* ratios of all the consecutive stages obtained using TCAD simulations.

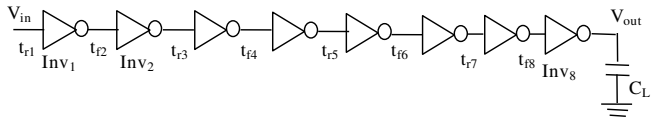

Figure 4: An 8 stage inverter chain showing equal transition times at alternate stages, simulated using our TCAD-calibrated Verilog-A FinFET model.

Table II: Unique transition times in odd/even stages of the8 stage inverter chain of Fig. 4 for stage ratio 2

	t_{r1}	t_{r3}	t_{r5}	t_{r7}
$t_{r(odd)}$ (ps)	7.2	7.07	7.24	7.18
	t_{f2}	t_{f4}	t_{f6}	t_{f8}
$t_{f(even)}$(ps)	4.53	5.00	5.09	5.08

Fig. 6(a) shows that these unique transition times t_f and t_r follow a straight line when plotted w.r.t. stage ratio. This is because: Suppose $t_f$in and $t_r$out have values corresponding to the unique set (t_r, t_f) for a given value of ρ for Inv_2 (Fig. 5(c)).When ρ is increased, say $t_f$in (and thus $t_r$out) is increased in such a manner that the one-to-one correspondence between Inv_2's input and output voltage values during transition is maintained, as explained earlier in this section. Therefore, the values of the elements of the unique set (t_r,t_f) increase almost proportionally with stage (NF) ratio.

Thus, if the given final load C_L to be driven can be replaced with an equivalent FinFET inverter having an appropriate number of fins, sizing of FinFET inverter chain can be done using the method described later in this subsection. For example, for an inverter chain with stage ratio ρ = 2, Fig. 6(a) suggests a unique set (t_r, t_f). Fig. 6(b) shows the values of the effective input capacitances of an inverter as a function of NF, with its input transition times corresponding to the unique set (t_r, t_f) for ρ = 2, which is obtained from Fig. 6(a). Thus the equivalent value of NF of an inverter, having an input capacitance equal to a specified load capacitance C_L, can be obtained from Fig. 6(b).For example, if C_L = 600aF and ρ = 2, C_L is replaced by a FinFET inverter with NF_n = 8 and 9 fins for rise and fall input transitions, respectively (from Fig. 6(b)). Inappropriate estimation of *ENF* (Equivalent NF) leads to significant error in the calculation of C_{out}/C_{in} and hence the delay. For example, error in estimation of C_{out}/C_{in} and delay (not considering the transition time dependency) in a two stage FO4 inverter chain is 31.8% and 15.3% respectively (from mixed-mode TCAD simulations).

Now we generalize this method to find the equivalent number of fins of a given load C_L for any given ρ. For a given inverter size *NF*, if we vary ρ (i.e., *NF* of its load stage), the inverter's input capacitance C_{eq} varies linearly with the corresponding values of unique t_r (t_f), as shown in Fig. 7(a).As explained earlier, this is because of the one-to-one correspondence of input-output voltage values when corresponding unique t_r (t_f) is maintained. Since C_{eq} also varies linearly with *NF* for a value of unique t_r (t_f)(or a given ρ), as discussed in Fig. 6(b), the slopes and intercepts of C_{eq} versus unique t_r (t_f) plots vary linearly with *NF* (Fig. 7(b)). Again, this linear (almost proportional) variation of C_{eq} with NF for an inverter with unique t_r (t_f) is due to the one-to-one correspondence of input-output voltage values. From Fig. 7,

$$C_{eq} = m.t_r + C_o \quad (3)$$

As in Fig. 7(b), for a given FinFET technology, the slope m and intercept C_o can be obtained for important values of ρ (or unique t_r (t_f)) for any value of NF. For a given value of C_L and ρ (or unique t_r (t_f)), Eqn. (3) and the linear relationships of m and C_o with NF determine the value of ENF. Thereafter, we can find the size of all the stages of the inverter chain by:

$$NF_{n-1} = \frac{NF_n}{stage\ ratio,\rho} \quad (4)$$

We now discuss the application of our FinFET buffer sizing method in the presence of branching load C_L' (Fig. 8). For a given ρ, we determine the value of ENF for C_L (main path) using the method described above. Next, we find the ENF for C_L', assuming that the branching path is designed with a value of ρ equal to that of the main path. If the number of stages between the node at which branching happens and the final node connected to C_L, is k, number of fins in the main path stage with branching at its input is $ENF_m = ENF(C_L)/(\rho)^k$. If the number of stages in the branching path is chosen to be k_b, $ENF_b = ENF(C_L)/(\rho)^{k_b}$. We define the branching effort b = (ENF_b+ENF_m)/ENF_m (in line with [4]). The value of b can now chosen by choosing the number of inverter stages k_b of the branching path. For example, in Fig. 8, ρ = 2, C_L = 2300aF (ENF = 32) and C_L' = 290aF (ENF = 4). If one wants a b = 2, we need not keep any inverter stages in the branching path and can connect C_L' directly to the branching node. In the next subsection, we verify the method of sizing stages discussed above using TCAD simulations while considering the

transition time dependency of effective capacitances.

1. Equal stage ratio results in minimum delay

From Eqn. (5) and from our discussion earlier in this section, we determine the ideal stage ratio ρ if the number of stages n and load capacitance C_L are specified (we obtain the best value of n later in this paper):

$$\rho = F^{\frac{1}{n}} \text{Where, } F = b.\frac{ENF(C_L)}{NF_{in}} \quad (5)$$

Where, NF_{in} is the number of fins of the first stage of the buffer. Using mixed-mode TCAD and our Verilog-A model based SPICE simulations, we verify our method. The delay of the inverter chain is minimum for equal stage ratio (table III), as we predict in this section. In this table, the first column shows the stage ratio of each stage in a 3-inverter chain.

2. Optimum number of stages for minimum delay

For a given value of load capacitance (i.e., F), we have devised a method to obtain the ideal stage ratio for a FinFET buffer if the number of its stages n is given. This method considers the device's gate's effect on parasitic capacitances.

We now extend the work to obtain an ideal number of stages n for a given C_L and NF_{in}. Using Fig. 7, we first obtain ENF (C_L). We substitute this ENF_n in (2) and equate all stage efforts for the given value of n, as discussed in the previous subsection.

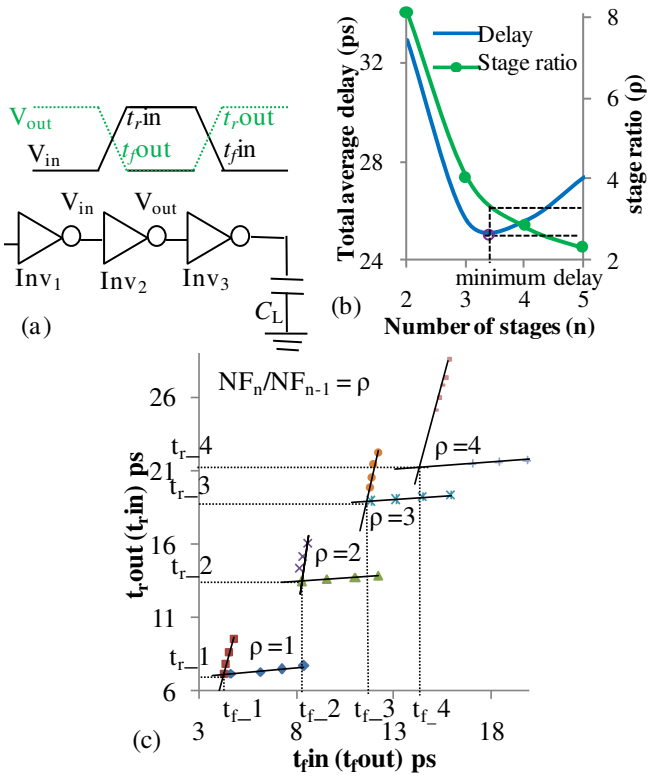

Figure 5: (a) Three stage FinFET inverter circuit. Voltage transitions at the input and output of the Inv_2 (input with rise/fall time $t_r$in/$t_f$in and corresponding output with fall/rise time $t_f$out/$t_r$out) are depicted. (b) Optimization of the number of stages of the inverter chain for minimum delay. (c) Variation of $t_f$out ($t_r$out) with $t_r$in($t_f$in) is plotted, falling/rising transition times are shown in x/y axis respectively. Intersection points are denoted as (t_r, t_f) for a given NF_n/NF_{n-1}.

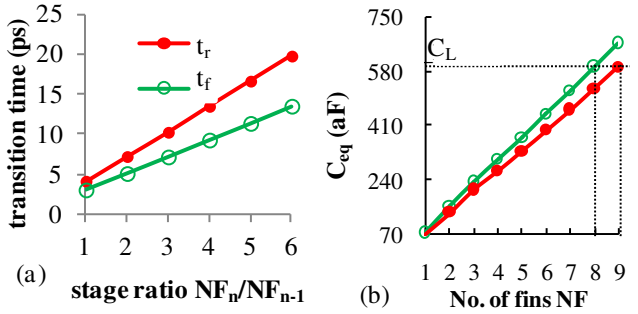

Figure 6: (a) Unique transition times (rising/falling) vary linearly with the stage ratio ρ (b) Relation of the equivalent input capacitance of an inverter with its size (*NF*) for a given ρ, when its corresponding unique input transition time is maintained [here, ρ = 2].

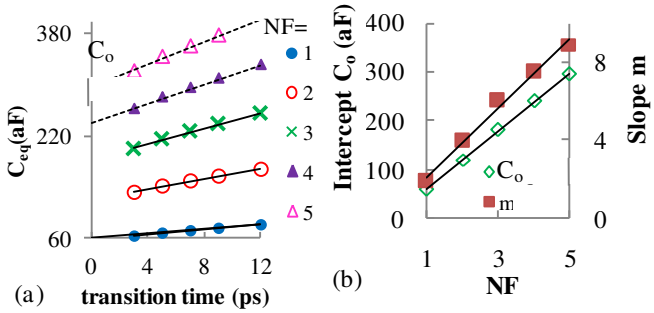

Figure 7: (a)Variation of the equivalent input capacitance of a FinFET inverter (having number of fins *NF*) with unique transition time at its input. For each value of transition time, this is an inverter with a given size (*NF*) which is a part of an inverter chain with corresponding stage ratio, (b) Slope and intercept of the linear trend C_{eq} vs transition time shown in Fig. 7(a) are linearly dependent on *NF*.

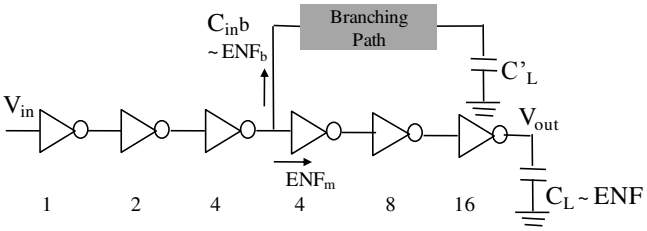

Figure 8: FinFET inverter circuit with branches.

Table III: Delay for a given C_L/C_{in} for different stage ratios of a FinFET 3-inverter chain using TCAD mixed-mode simulations

Stage ration NF_1:NF_2:NF_3	Delay (ps) for rising input	Delay (ps) for falling input	Average delay (ps)
1:2:4	14.76	15.11	14.935
1:1:1	17.01	19.81	18.41
1:3:4	15.13	16.23	15.68
1:5:5	17.24	19.39	18.315
1:4:4	15.74	17.52	16.63
1:1:2	15.07	15.81	15.44

Further, using the approach of [4] for conventional technologies, while replacing $F = b.\frac{C_L}{C_{in}}$ with $F = b.\frac{ENF(C_L)}{NF_{in}}$, we now minimize average buffer delay D = (D_r + D_f)/2 by choosing the optimum value of n. If $\rho = (NF_n/NF_1)^{1/n}$, this

minimization of D with respect to n yields that the ideal value of ρ follows:

$$\rho(1 - \ln(\rho)) + p_{inv} = 0 \quad (6)$$

Here, p_{inv} is the parasitic delay for an inverter in basic delay unit τ (τ is the slope of Fig. 3(a)). Therefore, p_{inv} is the ratio of the intercept and slope of delay versus *NF* plot (Fig. 3(a)). This expression is the same as that obtained in [4]where the stage effort was defined as $\rho = (C_L/C_{in})^{1/n}$ and has a fitting expression for ideal stage effort $\rho = 0.71p_{inv}+2.82$ in Eqn. (6). For our FinFET technology, we obtain the value of $p_{inv}= 0.62$ and therefore $\rho= 3.26$. For a given C_L and NF_{in}, this ideal value of ρ corresponds to an ideal number of stages n. In Fig. 3, the total delay of a three stage inverter chain is plotted with varying stage ratio ρ using mixed-mode TCAD simulations. The transition times are matched throughout the inverter chain for each stage ratio by using the method explained in Fig. 5(c).Finally, to verify our result regarding the ideal value of ρ (or n), we use our mixed-mode TCAD calibrated Verilog-A model based SPICE simulations. For a given load $C_L= 4800$aF we obtain the ideal number of stages and stage ratio as shown in Fig. 5(b). We observe that the minimum of delay with change in stage ratio is very sharp and the optimum number of stages obtained using our method results in a significant reduction in delay.

4. Impact of anomalous transitions on sizing of FinFET inverter chain

The design of an inverter chain with the ideal number of stages would be done for critical paths. We now address the question whether using a very low value of ρ is desirable for non-critical paths (for example, non-critical paths can have all minimum sized inverters).It was observed by our group in [14] that the voltage transitions at the nodes of a FinFET inverter chain are anomalous if the driver inverter finds a small inverter load (FO < 1). These anomalous voltage transitions contain a duration of slowly varying voltage "drag" for a certain duration of time due to the increase in the total gate-drain capacitance of load stage [14]. This increases the transition time and hence the delay of the inverter chain significantly. This is of important concern for the sizing of the non-critical paths where keeping small FOs is the general practice. We verify this through our Verilog-A HSPICE simulations of a five stage FinFET inverter chain as shown in table IV. We find that the delay of the inverter chain in the 2nd case where the 2nd and 4th stage driver inverter find a small stage ratio (1/3) is larger than that in case 1 due to the presence of drag. This signifies that the sizing of the non critical paths without considering this effect may lead to unexpected increase in delay.

Table IV: Impact of anomalous transitions on Delay for a givenC_L/C_{in}

Stage ration NF_1:NF_2… :NF5	Load C_L (aF)	Delay (ps)
1:1:1:1:1	72	15.37
1:3:1:3:1	72	20.47

5. Conclusion

We propose for the first time a modification of the method of logical effort (LE) its delay model considering the transition time dependence of the effective input capacitances in FinFET inverter chains. This is significant as our method allows circuit design using FinFET devices which do not have a highly gate-overlapped source/drain with the latter causing significant reduction of performance. We showed that the method of logical effort is valid for FinFET circuit design if the stage effort is expressed in terms of number of fins *NF* and the load capacitance C_L to be driven can be emulated by an equivalent inverter with an appropriate number of Fins NF_n. We devise a method to determine this appropriate value NF_n for a given C_L. For this, we first demonstrate that for an inverter chain with a constant stage ratio, the FinFET inverter capacitances are proportional to *NF*. This is valid though the capacitances are a function of input/output transition times. We determine the appropriate number of stages for driving a given C_L. We show the validity of our results using TCAD and Verilog-A model based HSPICE simulations. We also consider branching loads in our method. Our method allows a systematic sizing of stages in a large inverter chain, which is important for critical paths. We observe that our FinFET transistor sizing method results in a significant reduction in delays. Finally, we also discuss a lower bound on the stage ratio in non-critical paths so that their delays do not increase significantly.

6. References

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