An ESD Transient Clamp with 494 pA Leakage Current in GP 65 nm CMOS Technology

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Abstract

In this paper, a low-leakage PMOS based transient clamp with a thyristor as a delay element in 65 nm general-purpose (GP) CMOS technology is presented. Simulation results show that the proposed clamp is capable of protecting the circuit core against ±1.5 kV HBM and ±125 V CDM ESD stress by limiting the voltage across it to less than 5 V. The proposed clamp was characterized over PVT conditions with 2200 different combinations to investigate the selectivity to power-on ramp rates. Extensive analysis and measurements demonstrate that the clamp is robust against false triggering and transient induced latch-up. Measurement results show that the clamp is capable of handling 3.82 A, while its leakage is only 494 pA at room temperature. HBM and CDM measurement results show that the proposed clamp passed +3.25 kV and -1.75 kV HBM stresses and +800 V and -550 V CDM stresses.

Keywords

Electrostatic discharge (ESD), power supply clamps

1. Introduction

Electro-Static Discharge is a well-known reliability challenge that impacts Integrated Circuit (IC) yield and reliability. Designing efficient ESD protection circuits has become essential to prevent ESD related yield loss [1]. As the ESD event happens, it balances the charge between two charged objects with opposite polarity and leads to a high current for a very short time. A high current density and/or electric filed can damage conductor, semiconductor and insulator in an IC [2]. The high current density damages the semiconductor devices through thin-film fusing, filamentation, and junction spiking [2]. The high electric field, on the other hand, can cause failure through dielectric breakdown or charge injection [2]. ESD protection for an IC is usually limited by the oxide breakdown, which is approximately 5 V for 65 nm CMOS technology [3]. Therefore, it is important to design ESD protection circuits that are able to prevent these failures. Often ESD protection targets are desirable for a given technology that ensure low losses due to ESD. For 65 nm technology, it is considered to be 1.5 kV HBM protection level [3].

Figure 1 shows the typical chip-level ESD protection scheme in which an ESD power supply clamp is connected between the two power rails under different ESD stresses. The main goal of ESD protection circuits is to provide a low-resistive discharge path between any two pins in the chip. The circuit core is susceptible to ESD damage if only I/Os are ESD protected. As shown in Figure 1, the ESD clamp provides the discharge path for an ESD event that happens between the two power rails (Positive stress at V_{DD} node while V_{SS} node is grounded (PSD-mode), Positive stress at V_{SS} node while V_{DD} node is grounded (NDS-mode)). The power supply clamp is also part of the discharge path for both PS-mode (i.e. Positive stress at I/O node while V_{SS} node is grounded) and ND-mode (i.e. Negative stress at I/O node while V_{DD} node is grounded). As a result, it is important to have an effective ESD power supply clamp across the power supply rails [4].

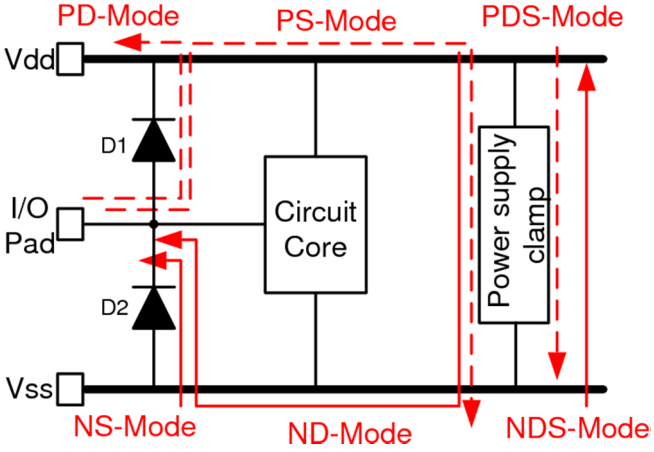


Figure 1: Typical chip-level protection scheme under different ESD stresses.

Under the normal operating condition of the circuit core, the ESD clamp should have a very low-leakage current and should be stable and immune to the power supply noise. In addition, the ESD clamp must effectively react to an ESD event. In recent years, there have been attempts to design different ESD power supply clamps to achieve the characteristics mentioned above. These designs fall under one of two categories: (i) Static clamps and (ii) Transient clamps. The static ESD clamps turn on once the voltage across the supply rails exceeds the triggering voltage and start conducting the current of the ESD event. The transient ESD clamps take advantage of the rapid change in voltage during an ESD event to trigger the clamp using a rise time detector and a delay element to keep the clamping element on during the entire ESD event. The rise time detector network that consists of a resistance and a capacitance is usually set to 40 ns so that it distinguishes between the normal noisy power supply and the ESD event [5]. Several designs have been proposed based on this concept [5], [6], [7]. Transient clamps are able to react fast; however, these circuits must be carefully designed to keep their leakage to minimum [8]. In this paper, an ESD power supply clamp

with a very low-leakage current with fast ESD response is proposed in a general-purpose TSMC 65 nm CMOS technology using thick gate oxide transistor to reduce its leakage. In addition, the proposed clamp was designed to meet the ESD protection level requirement.

2. Proposed ESD power supply clamp

One of the challenges in the design of transient clamps is to implement an optimum delay element that keeps the main transistor on during the entire ESD event. In this paper, an ESD clamp with thyristor delay element is described. A CMOS thyristor can provide a delay from nanoseconds to millisecond range and exhibits low sensitivity to environmental conditions. In addition, thyristor also has low leakage current [9]. The proposed PMOS based ESD power supply clamp with thyristor delay element is shown in Figure 2. The resistance (R_C) was set to 80 kΩ and the transistor (M_C) was sized so that its equivalent capacitance is 500 fF; thus, the time constant of the RC network is 40 ns.

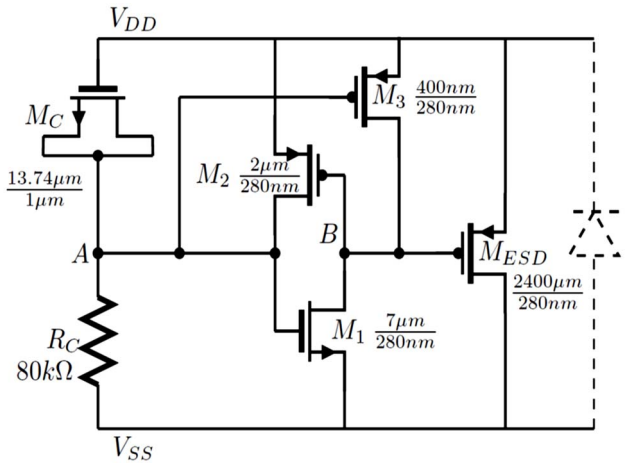


Figure 2: PMOS ESD clamp with thyristor delay element.

2.1. Operation of the proposed clamp

Under normal operating conditions, the capacitor M_C is fully charged and the voltage at node A is low. Thus, the transistor M_3 is on and the voltage of node B is high, which keeps the main transistor (M_{ESD}) off. Under the ESD event, the voltage of node A becomes high; and as a consequence, both transistors of the CMOS thyristor are on, pulling the voltage of node B to V_{SS} and turning on the main transistor (M_{ESD}). Even though the time constant of R_C and M_C is low, the CMOS thyristor works as a delay element and keeps M_{ESD} on for a period of time around 1 µsec. M_{ESD} was sized to ensure that the peak voltage is below 5 V under the + 125 V CDM positive ESD stress. All transistors in the clamp are designed with thick gate oxide transistors. M_1 was designed large enough to discharge node B to ground quickly.

2.2. Design specifications and decisions

Under normal operating conditions, the ESD clamp should have a very low-leakage current as the clamp most of the time operates under normal operating conditions of the circuit core. In addition, the ESD clamp should be immune against latch-up due to noise at the power supply rails or due to ESD event. The latch-up presents the case where the clamp turns on due to noise at the power supply rail or stays on after the ESD stress ends. Under the ESD stress, it is required that the ESD clamp reacts fast to the ESD event and stays on the entire ESD event.

The charged device model (CDM) has the fast rise time of 100 - 500 ps, it is essential for the clamp to effectively react fast to the CDM stress so that the voltage across the clamp is limited to be well below the breakdown voltage of the circuit core ($BVOX_{ESD}$ = 5 V). On the other hand, the entire duration of the HBM stress is approximately 600 - 750 ns; thus, the clamps should remain on for more than 600 ns. To ensure that the proposed designs have adequate characteristics mentioned above, Table 1 presents the specifications those should be met for the proposed design and how they have been met.

Table 1: The specifications to be met for proposed design.

Design Specifications		Criterion	Reason	Criterion met by
Under normal operating condition	Leakage current	Minimum	minimize the impact of ESD clamp	Using thick MOSFET
	Latch up	Immune		Using guard rings
Under ESD stress	V_P (CDM)	< 5 V	To protect core	W_{ESD} = 2400 µm
	Turn on time	Minimum	within ESD window	Proper sizing of M_1 to trigger M_{ESD}
	On-time	> 600 ns	ON for entire HBM	M_1 & M_2 sized to keep M_{ESD} ON

2.3. Design considerations for leakage minimization

The proposed clamp was optimized to have lowest possible leakage current without significantly compromising its ESD protection capabilities. The simulation results show that thick oxide NMOS transistor has the lowest leakage in TSMC 65 nm general-purpose CMOS technology. The thick oxide transistor has a gate oxide that is almost three times the thickness of the normal transistor. The thick gate oxide transistor has a leakage that is four orders of magnitudes lower than the leakage of the thin gate oxide transistor. We chose PMOS thick oxide transistor as the main clamping element despite having slightly higher leakage current compared to its NMOS counterpart as PMOS transistor has 10 - 15 % lower triggering voltage compared to an NMOS transistor of equal dimensions. As a result, PMOS transistor turns on faster than NMOS transistor. The thick oxide NMOS capacitor has the highest capacitance per unit area among the three low-leakage capacitors in TSMC 65 nm general-purpose CMOS technology [10]. Therefore, the thick oxide NMOS implementation was used to realize the capacitance of the RC network.

3. Simulation results

This section presents the carried out simulations to ensure that the proposed clamp meets the targeted ESD protection level and is stable under normal operating conditions of the circuit core.

3.1. HBM ESD stress simulation results

The proposed clamp was simulated under a ±1.5 kV HBM stresses using the HBM test defined in the Military standard (Method 3015.8) [11]. The +1.5 kV HBM was carried out through applying a positive HBM stress to the V_{DD} node of the clamp with grounded V_{SS} node, while the -1.5 kV HBM stress was carried out through applying a positive HBM stress to V_{SS} node of the clamp with grounded V_{DD} node. Figure 3 presents the proposed design under the +1.5 kV HBM stress. It can be seen in Figure 3, the voltage of node A follows the voltage at the V_{DD} node and the thyristor ensures that the V_B remains low to keep the main transistor M_{ESD} on for long enough time to safely discharge the complete ESD stress.

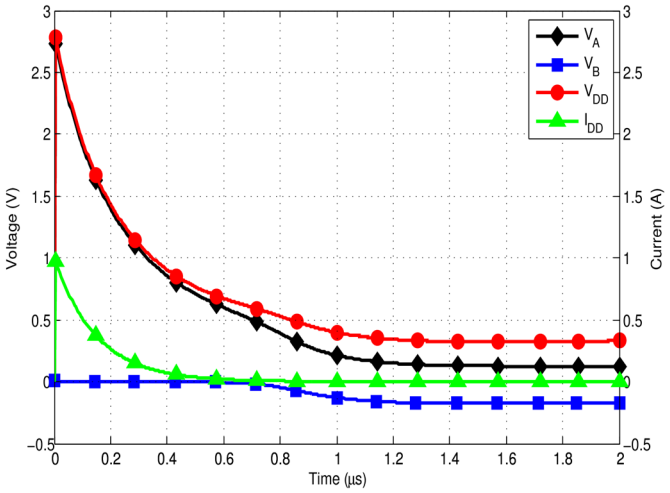


Figure 3: The proposed design under +1.5 kV HBM stress.

The substrate/drain parasitic diode of M_{ESD}, the dashed diode in Figure 2, provides the protection against the negative ESD stresses. The voltage across the clamp was limited to 1.37 V under the -1.5 kV HBM stress; therefore, the clamp is capable of protecting the circuit core against ±1.5 kV HBM stress in both directions.

3.2. CDM ESD stress simulation results

The proposed design was also simulated under a ±125 V CDM stresses. The positive CDM was carried out through applying a +125 V to the V_{DD} node of the clamp with grounded V_{SS} node, while the negative CDM stress was carried out through applying +125 V to V_{SS} node of the clamp with grounded V_{DD} node. Figure 4 shows the proposed design under the +125 V CDM stress in which the peak voltage is limited to 4.9V. In addition, the peak voltage across the proposed clamp was limited to 1.3 V under the -125 V CDM stress; thus, the proposed design is able to protect the circuit core against a ±125 V CDM stress.

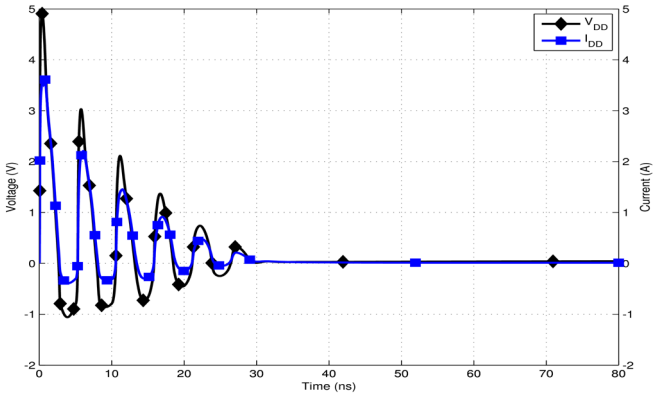


Figure 4: The proposed design under +125 V CDM stress.

3.3. Selectivity to power-on ramp rate

The selectivity to power-on ramp rate simulations was carried out to verify the stability of the proposed clamp under normal operating condition. A voltage with different slew rates and peak voltages were applied to the V_{DD} node with grounded V_{SS} node. The proposed clamp was characterized using different PVT conditions with 2200 different combinations. The voltage at the gate of the clamping transistor (V_B) was monitored; a transition for high to low means that the proposed clamp is triggered. Table 2 presents the PVT parameters and Figure 5 presents V_B as a function of the slew rate of V_{DD}.

Table 2: Parameter used for PVT simulation.

Slew Rate (V/S)	Process corner			V_{DD} (V)	Temp. (°C)
10^5 10^6 10^7 10^8 10^9	SS		SF	1 1.2 1.4 1.6 1.8 2 2.2 2.4 2.6 2.8 3	-40 -20 0 27 50 80 100 120
		TT			
	FS		FF		

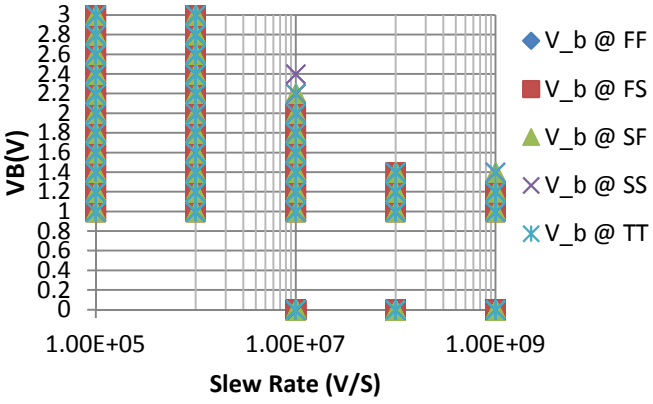


Figure 5: PVT simulation results.

As shown in Figure 5, V_B is always following V_{DD} when the slew rate $\leq 10^6$ V/S. In addition, V_B stays low when the slew rate $\geq 10^8$ V/S and $V_{DD} > 1.4$V to keep M_{ESD} on regardless the temperature and the process corner and that was expected as the slew rate falls in the ESD range (i.e. $\geq 10^8$ V/S). Therefore, the clamp is robust against power supply transients and noises.

4. Measurement results

The proposed design was fabricated in general purpose TSMC 65 nm CMOS technology. The total layout area of the proposed clamp is 75 µm x 47.36 µm. Figure 6 shows the layout of the proposed clamp. This section provides the measurements that were carried out to verify the proposed clamp under both ESD condition and normal operating condition.

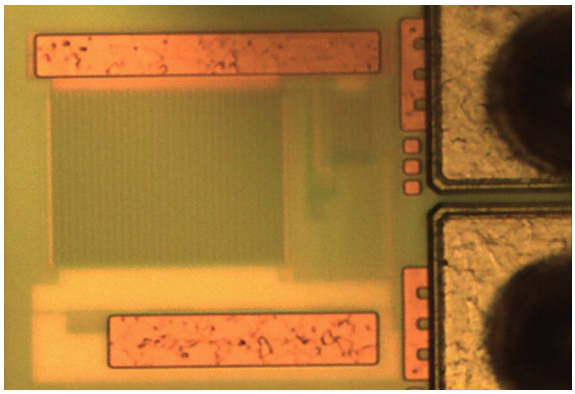


Figure 6: The layout of the proposed clamp.

4.1. ESD performance

4.1.1. Turn-on verification.

The turn-on mechanism of the proposed clamp was verified under both the chip not powered and chip powered conditions. In both cases, a 4 V ESD-like pulse voltage with 20 ns rise time was applied to V_{DD} node with grounded V_{SS} then the voltage across the clamp and the current flows into it were monitored. The voltage before and after applying the pulse was 1 V under the chip powered condition and 0 V under the chip not powered condition. The chip not powered condition measurement was carried out to observe the turn-on efficiency of the proposed clamp. The chip powered condition measurement, on contrary, was carried out to check the latch-up issues [12].

- **Chip not powered:** Under this condition, the pulse width was set to 500 ns. Figure 7 presents measurement results of the chip not powered case. Figure 7 shows that the proposed design stays on for the entire pulse duration. After the pulse ends, the current flow through the clamp returns to zero. The clamp is able to sink approximately 50 mA of current while V_{DD} voltage is clamped to 1.5 V.

- **Chip powered:** A pulse width of 100 ns was used in this case. As shown in Figure 8, the proposed clamp was triggered by the voltage stress and the average current going through the clamp (I_{DUT}) is about 50 mA. However, the proposed clamp is turned off after the stress ends, and the I_{DUT} goes back to the leakage current level. The powered condition confirms that the proposed clamp does not latch-up due to an ESD-like event as it turns off once the ESD-like event ends.

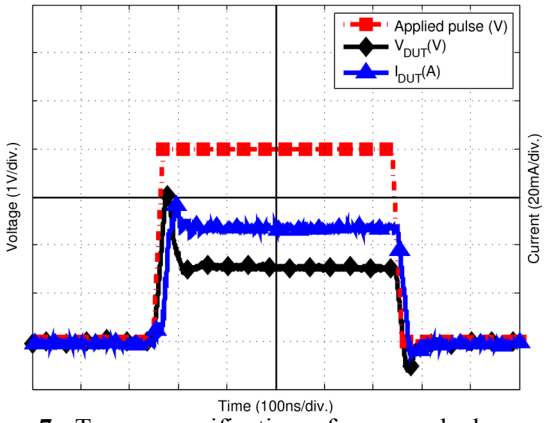


Figure 7: Turn-on verification of proposed clamp under chip not powered condition.

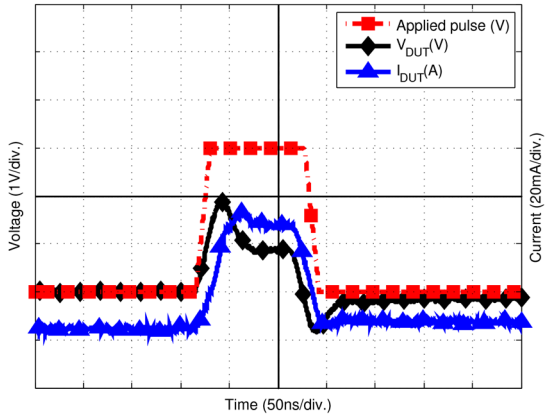


Figure 8: Turn-on verification of proposed design under chip powered condition.

4.1.2. HBM and CDM measurements.

Subsequently, the clamp was also subjected to HBM and CDM testing. These measurements were carried out by Evans Analytical Group (EAG) labs [13] using JEDECJS-001 standard for HBM measurements and the JESD22-C101F for the CDM measurements. For both measurements, the leakage current was traced before and after each ESD stress and the clamp is considered failed if the leakage current was more than 1 µA after the zapping. Positive and negative HBM stresses with 250 V step sizes were applied to the V_{DD} of the proposed clamp while the V_{SS} node was grounded. The clamp passed both +3.25 kV and -1.75 kV HBM stresses, but failed to pass +3.5 kV and -2 kV HBM stresses.

For CDM measurement, the packed chip with the proposed clamp was charged to both positive and negative voltages with 50 V step sizes. Subsequently, for the positive CDM stress, the V_{SS} node is grounded to zap the CDM event. Similarly, for the negative CDM stress, the V_{DD} node is grounded to zap the CDM event. The proposed clamp passed +800 V and -550 V CDM stresses, but it failed to pass +850 V and -600 V CDM stresses.

4.1.3. TLP measurement.

Transmission-line pulse (TLP) testing is one of the most popular methods to test the effectiveness of ESD protection devices and circuits. Figure 9 presents the TLP results of the proposed clamp. The proposed design is capable of handling 3.82 A of current, while its leakage is only 494 pA under 1 V supply at room temperature. As the five volts oxide breakdown of the circuit core transistors sets the limits of the ESD protection for an IC in the GP 65 nm technology, the current at 5 V (I_{5V}) becomes an important figure of merit to compare the proposed design against the-state-of-art ESD power supply clamps. I_{5V} shows the accurate current carrying capability as long as the device failure happens when the voltage is higher 5 V. From Figure 9, I_{5V} of the proposed clamp is 1.6 A, which can result in HBM failure threshold level of 2.4 kV. The proposed clamp has an on-resistance (R_{ON}) of 2.63Ω.

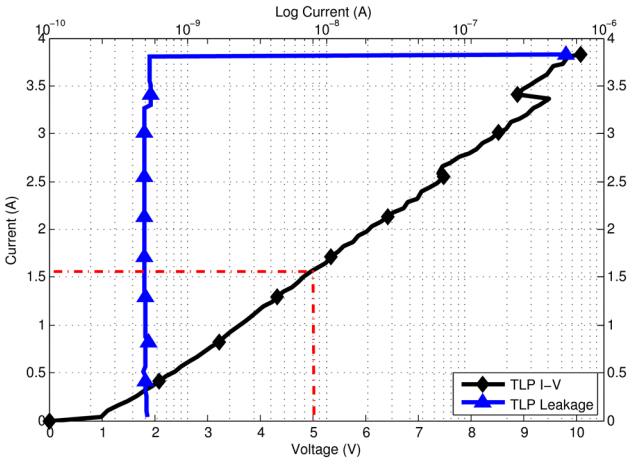


Figure 9: TLP measurement results of the proposed clamp.

4.2. Normal operating condition

4.2.1. Immunity to false triggering.

The clamp was also tested by mimicking the first power-on with a rise time of 100 ns and a voltage peak of 1 V. Both the voltage across the proposed clamp (V_{DUT}) and the current flowing in it (I_{DUT}) were monitored and are shown in Figure 10. It can be seen in the figure that the proposed design does not falsely trigger with the first power-on condition. The clamp does not trigger on as I_{DUT} increases to 600 µA then it goes back to the leakage current level.

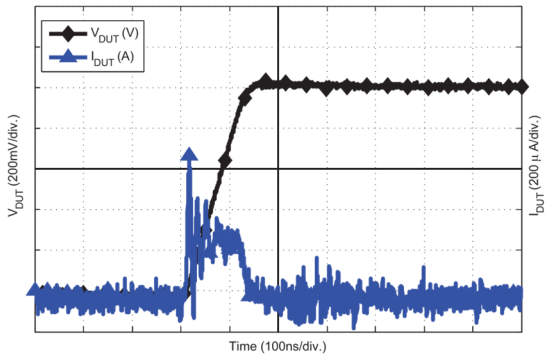


Figure 10: The proposed clamp under a fast power-on condition.

4.2.2. Leakage measurement.

The Pulsar 900 TLP system was used to measure the leakage current, while the ESPEC temperature chamber was used to control the ambient temperature. Figure 11 shows the leakage current of the proposed design as a function of temperature. As the measurement is limited by ESPEC chamber to the maximum temperature of 80ºC, the simulated leakage current of the proposed design is also shown up to 125ºC in the figure. Since the measured and simulated values follow the same trend in the 25ºC to 80ºC range, we expect the simulated values outside this range to be similar to the actual leakage currents. Based on the measurement results, the proposed clamp has a leakage current of 494 pA, and 13.4 nA at 25ºC and 75ºC, respectively.

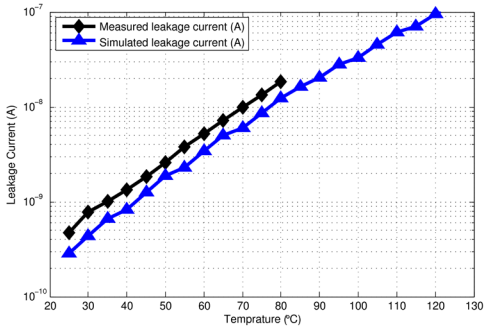
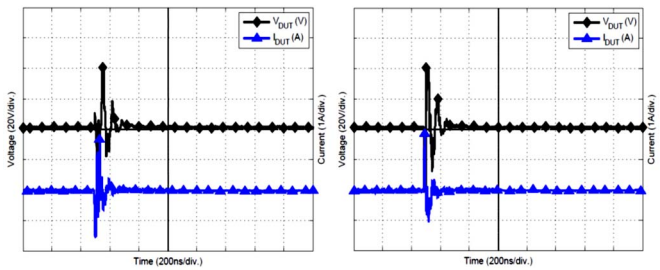


Figure 11: Leakage vs. temperature of the proposed clamp.

4.2.3. Immunity to transient induced latch-up.

Transient-induced latch-up (TLU) test is the technique to investigate the vulnerability of an ESD protection device to the transient noise in the power rails under normal operating condition. The TLU measurement setup at the component-level can precisely simulate the ESD-induced noise on the power rails under system level ESD test [14]. The proposed clamp was biased so that the voltage at the V_{DD} node is 1 V and the noise trigger source is directly connected to the proposed design. Both the voltage across the proposed clamp (V_{DUT}) and the current flowing in it (I_{DUT}) were monitored. Figure 12(a) presents the proposed design under a positive transient-induced latch-up with V_{charge} of +210 V, while Figure 12(b) presents the proposed design under a negative transient-induced latch-up with V_{charge} of -210 V. Figure 12(a) and 12(b) clearly show that the proposed design is robust against latch-up due to transient-induced noise with V_{charge} of ±210 V as the current goes back to the leakage current level once the transient-induced noise ends.



(a) $V_{charge} = 210\ V.$ (b) $V_{charge} = -210\ V.$

Figure 12: The proposed clamp under TLU with different V_{charge}.

Table 3: Comparison of the proposed clamp with state-of-the-art ESD power supply clamps in 65 nm technology.

Design	Area (μm^2)	Clamping element	Leakage current (nA) at				I_{t2} (A)	I_{5V} (A)	R_{on} (Ω)	+ HBM (KV)
			25 ºC	50 ºC	75 ºC	100ºC				
Proposed	3552	PMOS	0.494	2.61	13.4	-	3.82	1.6	2.63	3.25
[7]	5600	PMOS	170	200	270	350	> 3	2	2	> 4
[15]	1051	SCR	1.43	12.6	-	330	2.74	2.1	1.77	5
[16]	1530	SCR	16.2	-	-	-	2.64	1.8	2	5
[17]	2025	SCR	165	-	-	-	2.3	0.6	6.29	3
[18]	765	SCR	80	150	200	600	2.25	1.75	2.66	4

5. Comparison with state-of-the-art ESD power supply clamps in GP 65nm technology

The proposed clamp was compared with the design presented in [7], which was fabricated and tested in low-power 1.8 V 65 nm CMOS technology, and it consists of an RC triggering circuit with an active feedback delay element, while a PMOS transistor was used as the clamping element. The proposed design was also compared with designs presented in [15], [16], [17], and [18], where these designs were fabricated in general-purpose 1 V 65 nm CMOS technology using SCR as clamping element with different triggering circuits to optimize the layout area, the leakage current, or the ESD performance. SCR has been used as the clamping element in the implementation of ESD clamps in scaled technologies owing to its superior current carrying capabilities, and compact size. Table 3 presents a comparison of the proposed clamp with the state-of-the-art ESD clamps. From Table 3, the proposed design has the lowest leakage current compared clamps. In addition, the proposed clamp provides a comparable ESD protection level and on-resistance compared with the state-of-the-art ESD clamps in 65 nm CMOS technology. As thick oxide PMOS was utilized as the clamping element of the proposed design, the layout area of the proposed clamp is larger than the state-of-the-art designs that use SCR as the clamping element. Given PMOS transistor was used as the clamping element in the proposed clamp and that provided a comparable ESD performance, this makes the proposed clamp an excellent alternative when SCR is not an option.

6. Conclusion

In this work, a low-leakage, PMOS based transient ESD power supply clamp with a thyristor as a delay element in general purpose 65 nm CMOS technology is presented. By using thick oxide PMOS transistor, the leakage current of the proposed clamp is only 494 pA at room temperature. The proposed clamp was fabricated and verified using TSMC GP 65 nm CMOS technology. The measurement results demonstrated that the proposed clamp is robust against false triggering and transient induced latch-up. Moreover, the proposed design has comparable ESD protection level to the state-of-the-art ESD power supply clamps proposed in GP 65 nm technology and has the lowest leakage current at room temperature.

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