Enhancing Circuit Operation using Analog Floating Gates

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***Abstract*—Consideration of random device mismatch is an important factor in the design of high performance analog circuits. Floating gate transistors have long been used for digital non-volatile memory applications (such as flash memory), but a variant to this technology using an "analog floating gate" allows for higher precision programming. Analog floating gate devices can address mismatch observed in small geometry analog circuits. Enabling smaller devices to be used allows lower operating currents and higher frequencies. This property is exploited here to compensate for input mismatch and device parameter variations in an Operational Transconductance Amplifier.**

Keywords—Amplifier, Operational Amplifier, OTA, Operational Transconductance Amplifier, AFG, Floating Gate, Analog Floating Gate, CMOS, Memory, Logic

I. Introduction

Correcting for mismatch between matched MOS transistors is a serious challenge to analog circuit designers and in differential amplifiers most commonly manifests itself as an input referred offset voltage. Techniques commonly used to reduce offset voltage include auto-zeroing, correlated double sampling and chopper stabilization [1]. If we cannot simply make the input pair large enough to reduce mismatch physically, we can apply time-zero digital trimming, using laser trimmed or EEPROM devices [2]. Auto-zeroing and correlated double sampling are applied to sampled data systems while chopper stabilization allows continuous-time operation of the amplifier, though usually at a relatively slow maximum frequency.

Here we present a new method for correcting mismatch, using analog floating gate (AFG) devices, while maintaining the frequency performance. In previous work AFG devices have been used for programming mismatch, as a level shifter, and voltage reference [3]. This work showed we can easily replace an input differential pair with AFG devices at the cost of higher capacitance and lower frequency. However, depending on the placement of the AFG devices, complex programming may be required.

Operational transconductance amplifiers (OTAs) are important building blocks for a wide range of electronic circuits. They may replace the conventional op-amp in both first and second-order active filters [4], and can be used in two-quadrant multipliers and for implementing voltage controlled oscillators and filters for audio systems. As a test vehicle they are particularly useful, as they can be made to operate in a balanced condition of voltage and current that makes test of mismatch correction simple. Use of floating gate devices to compensate for mismatch has been studied [5, 6]. These design techniques show the use of floating gate devices in the signal path which increases programming complexity and impacts the bandwidth for the circuit. Some non-conventional techniques [7, 8] focus on low power and low voltage applications, but these have not considered the offset characteristics in the signal path, and also modelling over temperature.

Here, we examine a novel shunt method for using AFG devices as a means to trim input mismatch of an operational transconductance amplifier and measure and compare the performance of the trimmed and no AFG versions of the OTA. We propose an OTA design that uses two AFG devices to compensate for device mismatch and achieve a low mismatch temperature coefficient.

II. Analog floating gate Device

A. Device Concept

The analog floating gate device is similar to a standard MOS transistor, but the circuitry incorporates a second, floating, gate which has no DC electrical contact under normal operational conditions. The floating gate is surrounded by silicon dioxide, creating a potential barrier that prevents the charge stored on the floating gate from leaking off the floating node [9].

Fig. 1 shows the simplified schematic of the analog floating gate device. The floating gate sub-circuit consists of an NMOS or PMOS transistor with its gate terminal connected to the tunnel and control capacitors. This analog floating gate effectively introduces a variable threshold voltage for the output MOS device, which can vary continuously over a wide range of values.

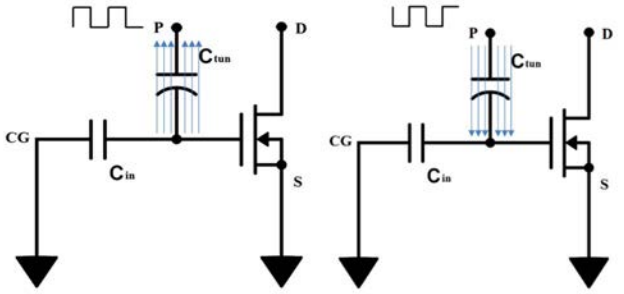
The basic structure of a floating gate memory relies on an insulated poly-silicon layer, the "floating gate". Charge on the floating gate is electrically isolated, hence providing permanent

storage. Charge on the floating gate can be modified through the application of appropriate voltages on a tunnel gate, through the Fowler-Northeim tunneling mechanism. External inputs to the floating gate are capacitively coupled through C_{in} as shown in Fig. 1. Capacitor C_{in} is used as the input to the transistor while C_{tun} is only used for programming. AFG devices can be made to act as tunable, non-volatile, analog.

B. Programming

A series of voltage pulses is applied to programming terminal "P" as indicated in Fig. 1. The AFG memory has similarities to programming a digital flash memory cell, though higher precision is required to guarantee accurate voltage levels.

The application of positive voltage pulses removes electrons from the floating gate, leaving the gate positively charged. This results in a lower effective threshold voltage (V_{th}) of the NMOS device as seen at the node CG.



(a) (b)

Fig. 1. Simplified schematic of the analog floating gate circuitry, showing tunneling mechanism, (a) positive charging, (b) for negative charging

If a negative voltage pulse is applied to the tunnel gate, electrons are added onto the floating gate. This is termed the discharging of the floating gate and results in higher effective threshold voltage of the NMOS device. The current through the MOS device is determined by the voltage on node CG and the charge on the floating gate node. A simple approximation for the change in threshold voltage is given by the equation (1), where Qpoly is the charge on the floating gate and Cpoly is the capacitance seen at the floating gate node.

$$\Delta Vth = \frac{\text{Qpoly}}{\text{Cpoly}} \quad (1)$$

The size of the Cin capacitor determines the voltage precision attainable from programming operation. The larger the capacitor, the more charge is required, and the smaller the possible incremental voltage step. The MOS device dimensions used can impact the AFG operation over temperature, since a longer channel MOS device requires a higher gate voltage for a given current, which results in a lower temperature coefficient for the output current.

The parameters that impact the programming stability of AFG devices are: tunneling oxide thickness, tunneling area, floating gate capacitance, programming time and programming voltages. Using AFG devices results in the possibility of precise threshold voltage trimming in a MOS transistor.

III. Operational Transconductance Amplifier

A. Circuit Analysis

The input offset in an operational transconductance amplifier (OTA) is the result of mismatch and parameter variations between what should be matched devices. Input offset can be either random or systematic. Even with optimum design methods and layout techniques input offset is inevitable due to random variations. A major manifestation of mismatch in an OTA is input offset voltage [10].

The OTA (Fig. 2) consists of an input differential pair M1 and M2 and three current mirrors. It is perfectly balanced amplifier if the two inputs are biased at the same voltages and assuming there is no mismatch, the operating point at OUT is V_{DD}-V_t (PMOS M8 threshold). If we assume a tail current of 10µA, the current flowing through M1 and M2 is 5µA each. Current mirrors M3-M4, M5-M6 and M7-M8 enables the OTA to be balanced at the DC operating point where the current through each transistor is approximately 5µA.

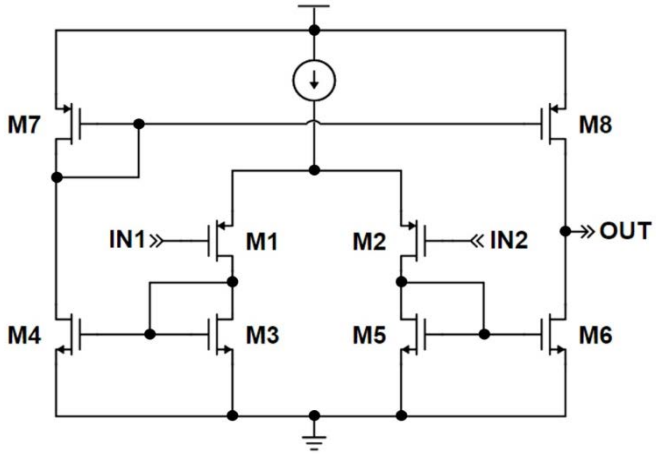


Fig. 2. Schematic of the operational transconductance amplifier, showing the balanced structure of the circuit

B. Mismatch correction circuitrys

As shown in Fig. 3, two AFG devices can be placed as shunt devices. If there is no mismatch on the input pair, these can remain inactive. However, If there is mismatch that needs correction, and say the V_{th} of M1 is less that of M2, for a matched input, the current through M1 would be higher than M2. This can be corrected by passing the excess current through AFG1.This placement of the AFG devices does not cause a reduction in frequency performance or complicate the programming, as would be seen if the AFG devices were included in the input pair. This retention of frequency performance is seen since only the DC path sees a change in current, and capacitance of the AFG drains is the only addition to capacitance.

The AFG devices are programmed to appropriate charge levels in order to shunt the excess or difference currents so that the OTA is balanced. The balanced state of the OTA can be achieved by programming single or both AFG devices.

Choice of appropriate device dimensions for the AFG MOS transistor plays a role in matching over temperature as discussed later in the paper.

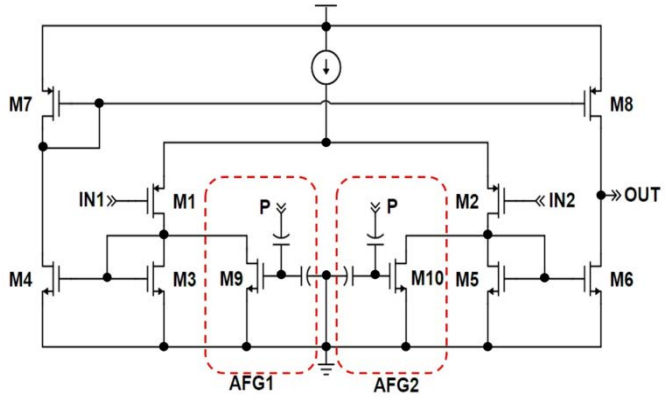


Fig. 3. OTA with AFG devices used to control the balance point of the input pair of the circuit. The OTA devices can be configured to pass current, adjusting the effective Vth difference of the input pair

C. Results

Fig. 4 compares a conventional OTA (solid lines) and an OTA with unprogrammed AFGs (datapoints). The gain, bandwidth and phase of the conventional OTA, and OTA with AFG devices remains virtually identical, showing no significant frequency impact.

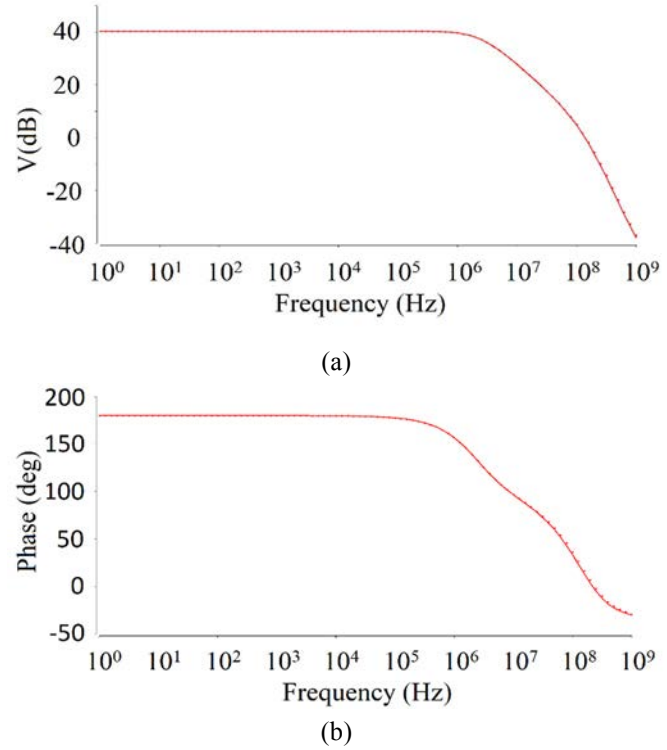


Fig. 4. (a) Gain and (b) phase of OTA with and without the addition of AFG circuitry, with the AFG circuit inactive

This shows the AFG circuitry does not disturb the OTA characteristics.

Temperature sensitivity is also an important metric. We have analyzed the circuit mismatch over temperature in Fig. 5. We assume a constant 15mV input pair offset. By applying different offset currents, in accordance with Table I. This is approximately linear the offset over the automotive temperature range of -40 ºC to 150 ºC.

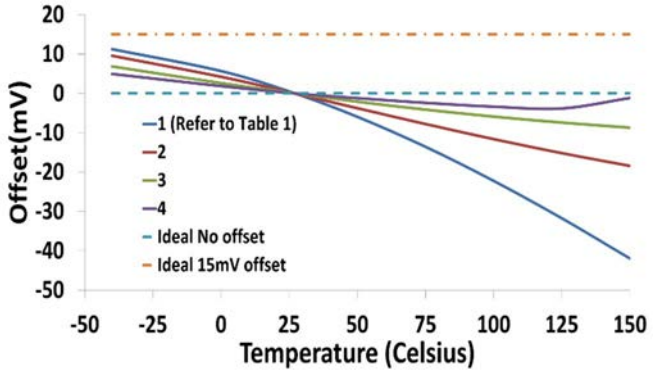


Fig. 5. Offset trim over temperature obtained from various programming combinations of the circuit in Fig. 3

Assuming a baseline 15 mV threshold mismatch between input pair M1 and M2, untrimmed, we obtain a constant 15mV mismatch across temperature. Trimming to zero offset at 27 ºC observe, as seen in Fig. 5 that we do not automatically achieve the same offset over the whole temperature range. Different cases give different results, as follows:

Case 1: Only one AFG device used for trimming. Instead of improving the offset, it becomes worse with temperature. This is because we are operating the AFG near to its threshold voltage. Since threshold voltage is not independent of temperature but the AFG voltage is fixed.

Case 2: Both AFG devices are operating. The charge stored on the floating gates is higher than in Case 1. We see an improvement in the temperature coefficient, though it remains unacceptably large. This is due to charge on both AFG devices still being close to threshold voltage at room temperature.

Case 3: Both AFG devices are operating here further from V_{th} , close to V_{th} +0.1V (under room temperature conditions). The results further improvement in temperature coefficient due to pushing the AFG devices into saturation region.

Case 4: Both AFG devices are operating further from their device V_{th}, giving even lower temperature coefficient. Fig. 5 shows that at higher temperatures the curve is not linear with respect to temperature. This issue is considered in the following sections.

We conclude from above that, increasing the stored charge (voltage) on the AFG devices improves offset drift characteristics over temperature. This is achieved because higher voltages move the AFG transistor into the saturation region of operation. However, though we have a very low temperature coefficient, nonlinearity is introduced at higher temperatures because we are shunting more current through the AFG devices leaving inadequate current to maintain the remainder of the circuit in a linear operational mode. This also

impacts the OTA slew-rate, bandwidth and phase characteristics.

TABLE I. SHOWS THE AFG PAIR VOLTAGES, AND CURRENTS FOR VARIOUS TEMPERATURES, TOGETHER WITH THE RESULTING OTA OFFSET

15mV offset between M1 & M2 devices							
Tail current = 10µA					Offset in mV		
#	VAFG 1 (mV)	VAFG 2 (mV)	IAFG 1 (µA)	IAFG2 (µA)	27 ºC	-40 ºC	150 ºC
1	937	0	0.685	0.009	0	11.2	-42
2	981	895	1.1	0.41	0	9.5	-18.5
3	1058	1015	2.2	1.5	0	6.8	-8.7
4	1115	1085	3.4	2.72	0	4.8	-1.2

From this we observe that shunting more current through the AFG devices, can improve offset over temperature. But we are limited by the tail current. We can resolve this by increasing the tail current, but depending on offset we do not always need an excess of this current. To resolve this, we propose a new AFG device as show in Fig. 6 and a modified OTA circuit which provides additional tail current, just to the level required by the circuitry.

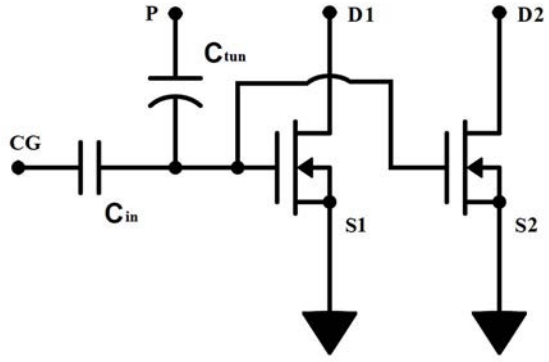


Fig. 6. New AFG configuration. This device has the same charge storage, but has two outputs, one to direct current from the OTA circuit, another to correct the tail current

By adding one more MOS transistor in the AFG circuit, which is used as a means to mirror current back into the input pair, we can introduce just the additional current we need to operate the circuit and correct the offset. The configuration used is shown in Fig. 7.

Fig. 7 shows the configuration of the modified AFG-based OTA. Here M11 and M12 are used in a feedback current scheme to add to the baseline tail current, through the M13 and M14 current mirror. This permits significantly larger tail currents that automatically adjust depending on the AFG demand, and gives the temperature operation as shown in Fig. 8, and Table II. Using this design change the performance parameters are met without loss in the output current and with resultant improved offset drift characteristics over temperature.

We analyzed the circuit mismatch over temperature for the modified design shown in Fig. 7 and the results are shown in Fig. 8.

Case 1: Stored charge on both AFG devices are shown. Offset is zero at 27 ºC and is around 5mV from -40 ºC to 150 ºC. So, we have an improved temperature coefficient and better linearity compared to the basic circuit.

Case 2: As we continue to further increase the AFG currents, we continue to see a better temperature coefficient than Case 1.

Case 3: This is best case observed. Offset in Case 3 is reduced to within 0.5mV over the entire temperature range of -40 ºC to 150 ºC.

With Case 3, Gain and phase are comparable as shown in Table II. We see a marginal improvement in frequency due to the higher feedback current.

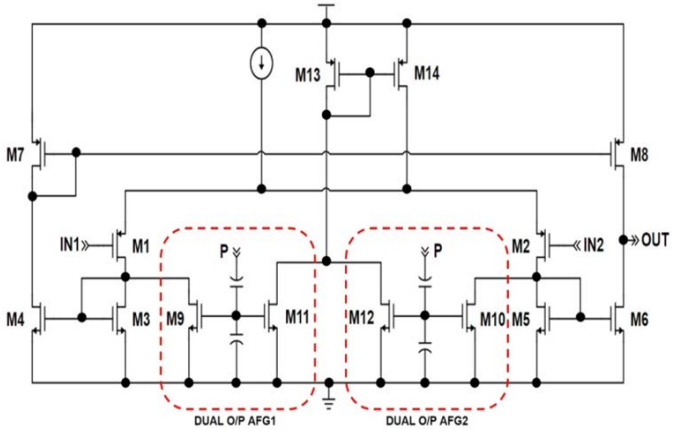


Fig. 7. Circuit including AFG feedback scheme showing the additional shunt current through AFG devices being mirrored and added to the tail current.

TABLE II. CHARACTERISTICS OF THE MODIFIED OTA, SHOWING OFFSET OVER TEMPERATURE TOGETHER WITH GAIN AND PHASE CHARACTERISTICS

Tail current = 10µA						Offset in mV			Characteristics		
15 mV offset	VAFG1 (mV)	VAFG2 (mV)	IAFG1 (µA)	IAFG2 (µA)	Feedback Current(µA)	27 ºC	-40 ºC	150 ºC	Gain (dB)	UGB (MHz)	Phase (degree)
1	1139	1101	4.07	3.095	7.31	0	2.81	-1.92	43.21	173.64	13.94
2	1209	1177	6.3	5.11	11.50	0	1.3	-0.27	44.33	185.02	11.95
3	1300	1272	10.07	8.79	18	0	0.23	0.45	46.08	196.39	9.07
Baseline is ideal OTA (no mismatch, no AFG)						Baseline			40.34	142.09	21

The accuracy to which we can program an AFG device depends on the charge change that can be introduced. It is important to know the precision with which we can program the AFG devices. Drain current trimming can be achieved by precise voltage trim of the floating gate. The output current of AFG devices can be varied by changing the MOS device size, programming voltage and pulse width.

Table III shows four tests which depict the relationship between the input offset that needs correction and its respective gate voltage difference between the two AFG devices. To correct 1mV input offset the AFG devices require approximately 10mV difference on the floating gates as shown in Fig. 9.

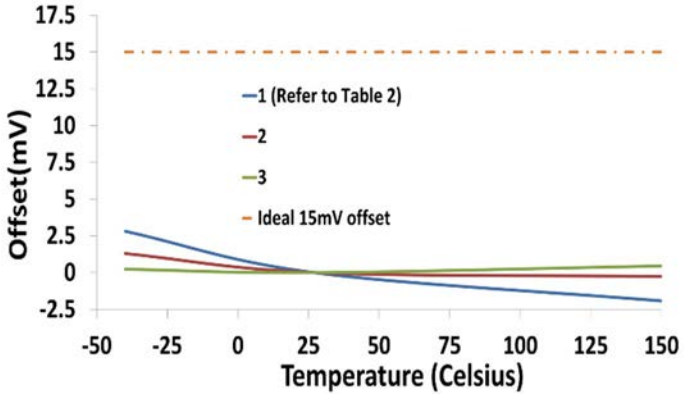


Fig. 8. Mismatch over temperature for the compensated circuit of Fig. 7

TABLE III. CHANGE IN AFG VOLTAGE TO CORRECT RESPECTIVE OFFSET

Test	Offset(mV)	ΔVAFG(mV)
1	1	10.206
2	5	52.832
3	10	111.32
4	15	178.535

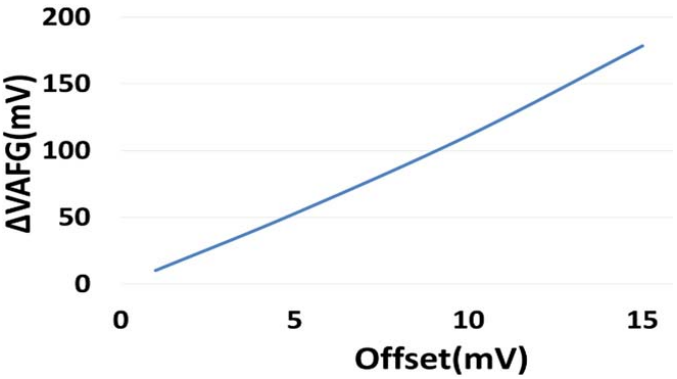


Fig. 9. Relation between change in AFG voltage required to correct corresponding input offset voltage

A major reason for using analog floating gate is the resultant overall circuit area reduction compared to a non-AFG circuit option. To create a no AFG OTA with the same offset as we get with the AFG trim, requires much larger circuit components. Using statistical models, we can determine the size difference, and this is shown in Table IV. Both the circuits were designed using 0.13µm CMOS technology. Table IV assumes an OTA design without AFG devices to have offset within ±1mV target range. This is compared to the OTA sizing from which we can trim with AFG components, to within ±1mV. We thus assume an OTA that is accurate by design to better than 15mV for the trimmable circuit.

TABLE IV. PERFORMANCE AND AREA COMPARISION FOR OTA DESIGNS WITH AND WITHOUT AFG DEVICES

Version	Gain (dB)	PM (deg)	UGF (MHz)	I_{TAIL} (µA)	Area
AFG Trim	46.26	14.75	210	10	1X
W/O AFG devices	46.82	19.4	251	500	1.304X

Therefore, the offset yield is comparable in both designs. The proposed methodology results in offset correction for continuous time operation, provides low power operation, area efficiency and does not limit bandwidth.

IV. SUMMARY

Random operational amplifier input offset due to device mismatch is corrected using AFG memory to achieve mismatch performance objectives without compromising other characteristics of the amplifier. Previously proposed techniques limit bandwidth and/or are discrete in the achievable correction range.

The performance characteristics of the OTA have been maintained, while minimizing silicon area compared to correct-by-design offset. This enables lowest operating power, continuous range of offset voltage correction, and minimum area. Offset characteristics over temperature have been studied and a novel current feedback scheme ensures offset voltage to remain within prescribed limits over the automotive temperature operating range.

V. ACKNOWLEDGMENTS

This research is supported by 'Texas Instruments Incorporated'.

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