An Automated Flow for Design Validation of Switched Mode Power Supply

Pradeep Kumar Chawda¹, Shrikrishna Srinivasan² Texas Instruments Inc., 3833 Kifer Rd, Santa Clara, CA ¹E-mail: <u>pkc@ti.com</u>, ²E-mail: <u>shrikrishna.srinivasan@ti.com</u>

Abstract—Traditionally SPICE simulations have been extensively used to validate switched mode power supply designs. It takes multiple iterations of each simulation type at a design corner and there are multiple such simulations required over several design corners to find and fix issues, which is tedious and error prone. This paper presents a novel methodology of using detailed analytical circuit equations in addition to simulations for automated validation of power supply design. In this work we propose automatic detection and correction of design issues over required design corners. This significantly reduces the number of simulations required for design signoff and therefore drastically reduces overall design cycle time.

Keywords—Power Supply; Switching Converter; Circuit Equation; Analysis; Simulation

I. INTRODUCTION

An electronic design operates under different input, output and component parameter variations caused by several factors while meeting desired characteristics in order to meet the requirements of larger electronic system. Designers need to ensure that their design meets all the requirements for a constant set of input, output and component parameters of their designs. It is not practical in most cases and is otherwise too expensive to minimize the variation of these set of parameters. In order to match these characteristics over a wide range of input, output and component parameters variations, we need to simulate the design with these variations and measure key design characteristics. For instance, a power supply design should meet certain characteristics such as load and line regulation, overshoot and undershoot variation, peak current variation, ripple variation[1-5]. Not all parameters variations are critical for design and therefore identifying the key parameters variations will help in reducing the resources required to run these simulations. This requires knowledge of the design as well as application apart from good sampling techniques. Once the simulations are completed and performance parameters are extracted, it needs to be checked against design thresholds to ensure all parameters are within required limits. Identifying key parameter variations, running simulations, extracting performance parameters for switching power supplies is very time consuming. In the absence of any well-defined method/tool to achieve this, users have to spend a lot of time doing it manually which is error prone. Therefore it results in inefficient designs which not only increase the system cost but also causes system failures. With a welldefined system and method/tool to accurately identify key parameter variations as well as using accurate measurement of performance parameters and running simulations in parallel we can make more reliable and cost effective designs. This paper presents a novel methodology for an automated power supply

design validation and correction. We start from the review of existing methods then the new method is discussed in detail followed by several examples.

II. SIMULATION AND ANALYSIS

A. Overview of Existing Methods

In order to address aforementioned issues, there are several attempts made at different levels. At IC design level, several tools, flow methodologies are available which rely heavily on simulation. For board level, simulating a complete IC at transistor level or multiple ICs together is not feasible due to excessing simulation time and therefore the existing IC tool/flows are not applicable and we need to take a different approach. At board level, in one approach a simplified behavioral model (equation based) of IC is used. This addresses the issue of simulation time however too much simplification reduces the accuracy and therefore not very useful. In another approach a macro model is used to characterize the IC. This approach is both accurate and feasible. However the simulation run time is still high as a large number of simulations are required as illustrated in Fig.

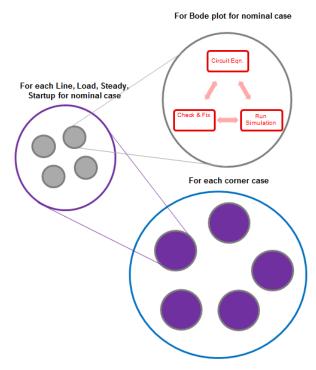
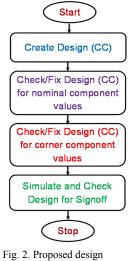


Fig. 1. Traditional design validation flow

1. Therefore it makes it difficult to adopt this approach in system design cycle. Ideally there is a need of a hybrid approach where initial design exploration is done using behavioral equations and simulations are run for more accurate results. This approach would reduce the number of simulations as well as maintain the accuracy by verifying design using accurate macro models.

B. Proposed New Method

Our solution is about advanced performance simulation and analysis to improve design quality and reduce design cost in shortest possible time using latest computing technology with minimal design/tool input required from the user. In our solution as shown in Fig 2, users need not worry about type and number of simulations to be run or the involved variables because, these are identified by а circuit calculator (CC). Circuit Calculator is a behavioral model of a power supply design circuit, which helps



validation flow

evaluate its performance in terms of operating value parameters like switching frequency, efficiency, duty cycle etc. The circuit is typically designed around the power supply IC to meet user requirements for input voltages, output voltages and current. The model correlates the component parameters of the circuit (for example – output capacitor capacitance, output capacitor ESR, FET Rdson, Feedback resistors etc.) with the operating value parameters mentioned above and is used to recommend the optimal combination of component and operating value parameters to achieve the design requirements. These operating value parameters may vary based on the circuit design. For example, if the IC requires an external compensation network, it will include Phase margin, Crossover frequency, gain margin etc. Once we have identified the required simulations and the variables

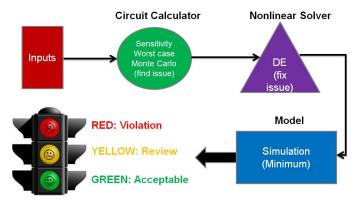


Fig. 3. Automated power supply validation and correction data flow.

involved, we automatically invoke those simulations.

All the simulations are run on the cloud and in a parallel fashion. We summarize the results of simulations in terms of pass/fail and the margin by which it failed and suggest the remedy. In addition to the summary, We generate performance simulation design report for designers. Our solution also helps users quickly verify the spice models of power supply designs over a wide design space and helps them identify the operating space for the design which meets their system requirement.

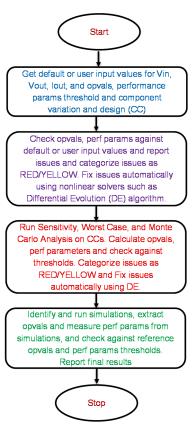


Fig. 4. Algorithm for automated power supply validation and correction.

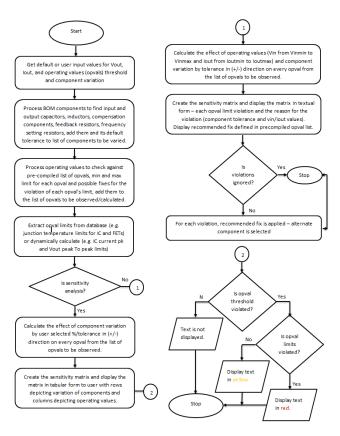


Fig. 5. Automated sensitivity and worstcase analysis flow.

1) Automated Validation and Correction

The automated power supply validation and correction flow is shown in Fig. 3 and Fig. 4. The flow for identifying key parameter variations and figure of merit for a given design is described below.

- a) We identify key parameter variations from CC based sensitivity and worst case analyses and use that information to setup circuit simulations.
 - Load and Line Regulation
 - Overshoot and Undershoot Variation
 - Phase Margin and Crossover Frequency Variation
- b) Following are the simulation of interest for Switching Power Converters

Performance Characteristics	Simulation Type
DC/AC gain, phase margin, gain margin, cross frequency	AC Analysis
Startup time, overshoot, undershoot, ripple, etc	Transient Analysis

- c) The circuit calculator based sensitivity analysis helps identify the critical component variations in circuit that affect operating value parameters and in turn the performance of the circuit.
- d) The circuit calculator based worst case analysis helps identify corners required for circuit simulation to validate the design safe operating area.
- e) Once the key component variations are identified, the key Input and output variations are identified based on design input and load requirements.
- f) Depending on the performance plots to be generated such as load and line regulation which requires parameter sweep analysis to sweep input voltage, output load current for power electronic designs (switching converters etc) is setup.

In order to reduce the number of simulations, the circuit calculators are used to estimate the overshoot and undershoot and fewer simulations are setup to validate only those cases. The key performance analyses identified are parametric sweep, sensitivity analysis and worst case analysis.

2) Simulation Setup and Report Generation

- User choose the performance characteristics (with validation range)
- The tool will select the simulation type based on user inputs and run worst case analysis
- From CC sensitivity analysis and worst case analysis, we know the sensitive opvals and the components they are sensitive to. Based on that information, we

identify only relevant simulations to be run for worst. case

3) Entry Points to Proposed Algorithm in a Design Creation Process

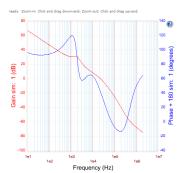
- Design creation
- Alternate component selection
- Select a different design parameter e.g. frequency

III. IMPLEMENTATION

The proposed methodology is implemented in WEBENCH Power Designer which has been fully described in [6]. In this section we will cover the sensitivity and worst case analysis implementation details.

A. Performance Parameters

Performance parameters are extracted from AC and Transient Simulation results and displayed as shown in Fig. 6. The corresponding algorithms are described in detail in our





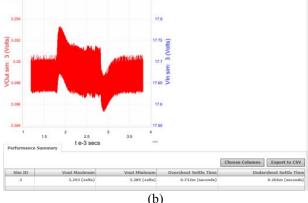


Fig. 6. Implementation results of measuring performance parameters of switching converters: a) Small signal analysis b) Large signal analysis.

		+~+		4V ~~~~		0 2		T-1-	- D		-	
🖛 🖒 🔍 📑	Öğili 🧉	**	100	dt 01	$^{\prime}$		2.	TCAD TS			0	
Back New Solutions Visualizer	BOM Ch	arts Schemat	tic Optimize	op Valis Re.Com	o Sin T	hermal Build R	Lite Edit	Export Sim E	xport Print	Share Design	Help	
					OPERATING	VALUES						
Optimization Tuning	Operating Val	ues Served	tivity Matrix (BB	TA) Worst C	ase Analysis ()	SETA)						
Lowest	Vin (V): 42.00	0 lout (A):	5.000 Com	poment Variation	10%	1.	Operating Valu	es Threshold	0.1%	Apply Charges		
DM Cost	The John halos	holice constant	tone the entrol	al sensitivities of	this designate of		the state of the s					
				perating values t								
Smallest potpetint	Component	Frequency	Efficiency	Vout p-p (V)	Duty Cycle	Phase Marg	Cross Freq	Gain Marg	IC TJ (depC)	IC lok (A)	Cout IRMS	Vost Act
	Name	(Hz) Min-100k	(%) Min=30	Min=0.0 Max=0.5	(%) Min=0.0	(deg) Min=35	(Hz) Min-24,416k	(dD) Max=-10	Mit=-40 Max=150	Max-6.3	(A) Max-3.805	(V) Min-4.75
outprint BOM Cost Efficiency	Ccomp_C(+10, 0%)			100000.0000		63.43						
422 \$5.12 87	Coomp_C(- 10.0%)					63.15						
Change Design Inputs	Ccomp2_C(+10					63.16		-16.57				
Advanced Options	Ccomp2_C(- 18.0%)					63.45		.16.79				
ode of Operation:	Cout_ESR(+10.			10.41m		63.52		-16.88				
INTERNAL_UVLO •	Cout_ESRI-			9.971m		63.09		-16.48				
User Preferred Frequency:	10.0%) L1_L(+10.0%)			9.254m		62.30	47.51k	-16.87		5,854	0.3775	
ednearch: D												
100kHz < ###### kHz < 831.834kHz	L1_L(-10.0%)			11.31m		64.36	48.38k	-16.47		5,799	0.4614	
atput Cap Options:	L1_DCR(+10.0		85.92									
Autosetel	L1_DCR -		86.23									
Cobarte	10.0%) Roomp R(+10.					59.82	51.98R	-15.44				
Use Advanced Options >>	(1%) Roomp RI-					65.85	43.71k	.18.06				
-	18.0%)					00.00	42.CTA	-10.09				
Carrent Design: #7258	Rfbb_R(+10.0%											4.620
base_pn TPS54540	RBb_R[-											5.469
VerMin 8.5 V VerMin 42 V	10.0%) R154_R(+10.0%											5.422
acuros OC)											
Vout 6 V	Rtbt_R(-10.0%)											4.582
1011 F.A	Rt FX+10.0%3	441.58	86.40	12.10m		62.18	47.83k	-15.91	62.60	5,792	0.4572	

Fig. 7. Implementation results of sensitivity analysis

previous work [7].

B. Sensitivity and Worst Case Analysis

Figure 5 show the algorithm to implement sensitivity and

Operating Value				Worst Cas	e Analysic	s (BETA)								
in (V): 42.000	lout (A):	5.000	Component V	variation	Compor	ent Tolerance 🛛 🔹	Operating Value	s Threshold	10%	 Apply Cl 	nanges			
The table below helps you explore the potential sensitivities of this design's operating values that might occur as a result of component variation. Results in black represent operating values that are affected by more than the selected 'operating values threshold' due to corresponding' component variation'. Results in red represent operating values whose limits are violated.														
Component Name	Frequency Min=100k Max=881.83	1000	Efficiency (%) Min=30 Max=100	Vout j Min=0. Max=0	0	Duty Cycle (%) Min=0.0 Max=100	Phase Marg (deg) Min+35	Cross Free Min=24.416 Max+97.66	6.01	Gain Marg (dB) Min=-31 Max+-10	IC Tj (degC) Min=-40 Max=150	IC lpk (A) Max=6.3	Cout IRMS (A) Max=3.881	Vout Actual (Min=4.75 Max=5.25
L1_L(+20.0%)				4.687m									0.2353	
L1_L(-20.0%)				7.030m									0.3530	

Default design – very few opval threshold violations, because threshold is very high.

Operating Value		y Matrix (BETA)		e Analysis (BETA)							
in (V): 42.000	lout (A): 6.0	00 Compone	ent Variation	Component Tolerance	Operating Val	ues Threshold	0.1%	- Apply	Changes		
he table below he elected 'operating	ilps you explore y values thresh	the potential se ald' due to corre	nsitivities of thi sponding 'comp	is design's operating values soment variation'. Results in	that might occur red represent op	as a result of co erating values v	mponen hose lit	nt variation. Resinits are violated.	ults in black rep	resent operating va	dues that are affecte
Component Name	Frequency (F Min=100k Max=881.834k	z) Efficiency Min=30 Max=100	(%) Vout p- Min=0.0 Max=0.0	Min=0.0	Phase Marg (deg) Min#36	Cross Freq Min=24.416 Max=97.663	e 18	Gain Marg (dB) Ain=-31 Axxx-10	IC Tj (degC) Min#-40 Max=150	IC lpk (A) Max=6.3	Cout IRMS (A Max=3.881
Ccomp_C(+6.0%)					61.87						
Coomp_C(-5.0%)					61.74						
Ccomp2_C(+6.0%					61.73		-1	8.98			
Ccomp2_C(-					61.89		-1	9.13			
Cout_ESR(+2.0%)			5.656m				-1	9.13			
Cout_ESR(-2.0%)			5.582m				-1	8.98			
L1_L(+20.0%)			4.687m		59.58	39.42k	-1	9.41		5.408	0.2353
L1_L(-20.0%)			7.030m		64.32	41.17k	-1	8.59		8.611	0.3530
Roomp_R(+1.0%)					61.48	40.63k	-1	8.90			
Rcomp_R(-1.0%)					62.14	39.94k	-1	9.20			
Rfbb_R(+1.0%)											
Rtbb_R(+1.0%)											
Rfbt_R(+1.0%)											
Rfbt_R(-1.0%)											
RT_R(+1.0%)	483.4k		5.716m		61.72		-1	8.97	84.76		0.2853

Default design – no opval limit violations, although there's threshold violations. (C3216X5R1A686M160AC cout=68uF, ESR=3.494m)

n (V): 42,990 liser	c(4): 5.000 Compo	cent Variation Comport	nent Tolevance + Ope	rating Values Threshold	1.01% + Anth Change					
he table below helps y red represent operation	you explore the potential ing values whose limits at	sensitivities of this design re-violated.	n's operating values that a	sight occur as a result of co	reponent variation. Results i	n black represent operativ	g values that are affected	by more than the selecte	l'operating values three	holf due to correspond
Component Name	Fraquency (72) Mar-120x Mar-021,824k	Efficiency (%) Min=20 Max=100	Most p-p (V) Mos+0.1 Max+0.1	Duty Cycle (%) Min-6.0 Max-100	Phase Morg (deg) Mor-25 Max-90	Cross Feeg (Hz) Mic-24.410x Mez-07.0028	Gain Marg (d3) Mis+31 Mas+10	IC 1) (degC) Micr-40 Max-100	E ipa (A) Max-6.5	Cout FIMS (A) Max-0.15
Conne_C(-5.I%)						184.98				
Comp2_Q+5.8%					70.15	184.00	-15-22			
Coongil_(2-6-9%)					70.41	115.44	-15.24			
Cout,ESR(+2.0%)			0.1996		99.44	187.76	-15.09			
Cout_ESR(-2.8%)			0,1917		71.15	182.%	-15.37			
11,12(23.3%)		85.39	0.1530		74.81	167.2k	-16.82		5.408	6,3965
L1_L(-20.3%)		85.35	0.2646		64.58	216.04	-13.45		5.611	0.3530
L1_DON(+2.0%)		65.33								
1,008(23%)		85.42								
Renne_Ret 196					69.62	105.28	-15.13			
Roomp, Ref. 13%)					70.34	183.7k	-15.33			
884,8(+1.0%)										
R04_8(-1.05)										
85(8(115)										
AND ALL THE										
8(8(+1.0%)	45.4	85.41	0.1976		70.12	104.58	-15.15	64,78	5.454	0,3963
81,821.010	455.38	85.34	0.1937		70.43	185-0	-15.31	65.30	5.494	0.27%6

Changed Cout component – opval limit violations in addition to threshold violations. (EEE-FC1C680P – cout = 136uF, ESR=0.2 Ohm)

Fig 8. Illustrating the sensitivity analysis results.

Run Worst Case An	alysis			
Op Val	Min Mal	Max Val		Worst Case Analysis Results X
Frequency (Hz)	100k	881.834k		After running the worst case analysis, no issues have been identified with the design
Efficiency (%)	30	100		
Vout p-p (V)	0.0	0.5		
Duty Cycle (%)	0.0	100		
Phase Marg (deg)	35	90		
Cross Freq (Hz)	24.416k	97.663k		
Gain Marg (dB)	-31	-10	_	
IC Tj (degC)	-4.0	150		
C lpk (A)	N/A	3.3	_	
Cout IRMS (A)	N/A	3.881		
Vout Actual (V)	4.75	5.25		

Default design - C3216X5R1A686M160AC cout=68uF, ESR=3.494m

Run Worst Case Ana	ilysis			
Op Val	Min Vat	Max Val		Worst Case Analysis Results
Frequency (Hz)	100k	881.834k	-	Phase Marg (deg): 96.41 is out of range (35.00, 90.00) when vin = 8.5, jout = 5
Efficiency (%)	30	100		90.79 is out of range (35.00, 90.00) when vin = 8.5, iout = 5 90.79 is out of range (35.00, 90.00) when vin = 8.5, iout = 0.5 Cross Fred (Hz):
Vout p-p (V)	0.0	0.5		184.9k is out of range (24.42k, 97.66k) when vin = 42, iout = 5 212.5k is out of range (24.42k, 97.66k) when vin = 42, iout = 0.5
Duty Cycle (%)	0.0	100		Gain Marg (dB): -31.31 is out of range (-31.00, -10.00) when vin = 8.5, jout = 5
Phase Marg (deg)	35	90		Cout IRMS (A): 0,2824 (should be less than 0.1500) when vin = 42, jout = 5
Cross Freq (Hz)	24.416k	97.663k		0.2024 (should be less than 0.1500) when vin = 42, lot = 3 0.2760 (should be less than 0.1500) when vin = 42, lot = 0.5
Gain Marg (dB)	-31	-10		
IC Tj (degC)	-40	150		
IC lpk (A)	N/A	6.3		
Cout IRMS (A)	N/A	0.15		
Vout Actual (V)	4.76	5.25		

Changed Cout component – opval limit violations in addition to threshold violations. (EEE-FC1C680P – cout = 136uF, ESR=0.2 Ohm)

Fig 9. Illustrating the worst case analysis results.

worst-case analysis. The detailed algorithm is explained in work [12]

IV. RESULTS AND DISCUSSIONS

In order to demonstrate the effectiveness of proposed algorithm, we have selected a step down DC-DC converter [11] for discussion and results are presented in this section. This design is publicly shared and can be accessed by visiting the link provided in reference [13].

A. Sensitivity Analysis

For every opval associated with the part, we change all the component parameters (both positive and negative variation) and display its effect. There could be 2 levels of violation – violation of opval threshold selected by user using a drop down menu, or violation of opval limits for the design. All violations of selected opval threshold are displayed in yellow. Fig 7 shows the sensitivity analysis results for the default design and Fig 8 shows the results as we change component values.

- All violations of opval limits are displayed in red.
- User can also choose to change the operating output current and input voltage values and see the effects.
- User can also choose to select a component variation value different from default component tolerance.

B. Worst Case Analysis

Worst case analysis calculates operating values of the design at its corner cases by varying V_{in} from min to max and varying I_{out} from min to max. If no violations of opval limit occur, then each of the components is varied by its default component tolerance along with V_{in} and I_{out} . For each

violation, we display the value and the corresponding V_{in} and I_{out} values and the component that caused the violation if applicable. Fig. 9 shows the worst case analysis results.

C. Automated fixes of violations

In order to fix the violations, we have developed an algorithm which uses a technique to minimize opval violation errors by minimizing the objective function. The objective function is the sum of the weighted square errors of all the opvals in the design as -

Obj Fun =
$$\sum_{i=0}^{n} W_i X_i^2$$

where X_i is the OpVal_{target} – OpVal, n is the number of opvals in the design. More details about this approach can be found in our work [8-9].

The goal is to vary each component in the design except the one modified by the user (if that's the case) so that the global minima of the objective function is achieved. For every component, the limits of variation are set dynamically by introspecting the results of sensitivity matrix and the direction of component change affecting the opval. For example, it can be understood from sensitivity matrix results that C_{out} I_{RMS} can be decreased by increasing output inductance or decreasing frequency setting resistance. Therefore, if C_{out} I_{RMS} error is being minimized, output inductance limits are set to current inductance value and tolerance percent of the current inductance value. Once the convergence is achieved for minimizing the objective function, all violations are guaranteed to be fixed.

V. CONCLUSION

Extensive circuit simulations for validation of power supply design can be avoided by carefully using analytical circuit equations and doing advanced analysis at the circuit calculator level speeds up the design cycle time by minimizing the number of circuit simulations. This paper has presented a novel flow for validating and correcting the power supply design issues using circuit calculators first and using simulation for signoff only. The problem of identifying key parameter variations for running simulations and extracting performance parameters to identify issues and fixing them for switching power supplies because of limited expertise and resources is solved by feeding input from circuit calculators to identify minimum simulations required to accurately measure the performance parameters causing issues and proposing solutions to fix the identified issues.

REFERENCES

- Severns, R. P., & Bloom, G. (1985). Modern DC-to-DC switchmode power converter circuits. Van Nostrand Reinhold Company.
- [2] Maniktala, S. (2004). Switching power supply design & optimization. McGraw-Hill, Inc..
- [3] Mohan, N., & Undeland, T. M. (2007). Power electronics: converters, applications, and design. John Wiley & Sons.
- [4] Brown, M. C. (2012). Practical switching power supply design. Elsevier.
- [5] Kazimierczuk, M. K. (2015). Pulse-width modulated DC-DC power converters. John Wiley & Sons.
- [6] Jeffrey Robert Perry, et al. "Power supply architecture system designer", US Patent US8712741B2
- [7] Chawda, Pradeep Kumar, et al. "Determination of one or more operating parameters for a Switched-Mode Power Supply", US Patent Application No 62556216.
- [8] Pam, S., Satija, Y., Chawda, P., Mansour, M., Hanrahan, R., & Perry, J. (2016, March). A web-based tool for compensation design of power converters using hybrid optimization. In Applied Power Electronics Conference and Exposition (APEC), 2016 IEEE (pp. 3266-3272). IEEE.
- [9] Pam, S., Satija, Y., Chawda, P., Mansour, M., Hanrahan, R., & Perry, J. A Web-based tool for Compensation Design of Power Converters using Hybrid Optimization
- [10] WEBENCH Power Designer, https://webench.ti.com/webench5/power/
- [11] Step-Down DC-DC Converter, http://www.ti.com/product/TPS54540
- [12] Chawda, Pradeep Kumar, et al "Simulation and Analysis of Circuit Designs", US Patent No. 62566074
- [13] <u>https://webench.ti.com/appinfo/webench/scripts/SDP.cgi?ID=2C410572</u> <u>6AE14D94</u>