

Graphene-Based FPGA Design and Optimization at the 7nm FinFET Technology Node

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Abstract— Emerging graphene-based interconnects exhibit excellent conductivity, rendering them a promising alternative to traditional interconnect materials. The energy consumption and delay of field-programmable gate arrays (FPGAs) are significantly influenced by global routing, which presents a compelling opportunity for graphene interconnect technology. This study examines the potential benefits of replacing copper (Cu), the conventional interconnect material, with graphene. Three interconnect technologies are examined: Cu interconnects, improved graphene-capped Cu interconnects, and thick graphene. An interconnect/system co-design framework is designed to systematically evaluate their performance differences. Concerning graphene material-level parameters, our focus is on the impact of graphene contact resistance and mean-free-path on performance. Benchmark simulations indicate that graphene-based interconnects can enhance the energy-delay product of circuits by up to 32% in comparison to conventional Cu interconnects at the 7nm FinFET technology node.

Keywords— *Graphene interconnect, contact resistance, mean-free-path (MFP), field-programmable gate array (FPGA), interconnect/system co-design, benchmarking, FinFET.*

I. INTRODUCTION

As interconnect dimensions decrease, the resistivity of conventional copper (Cu) interconnects rises substantially due to increased grain boundary scattering, surface scattering, and the presence of a high-resistivity diffusion barrier layer [1-3]. Addressing these challenges has spurred considerable research, leading to the exploration of alternative interconnect materials such as Cobalt (Co), Ruthenium (Ru), and Nickel Silicide (NiSi) as potential substitutes for Cu [4, 5]. Among these alternatives, graphene—a promising two-dimensional material—demonstrates superior conductivity owing to its extended mean-free-path (MFP) [6, 7]. Nevertheless, graphene also introduces practical challenges, including high contact resistance, making

it more suitable for longer interconnects (on the order of micrometers to much longer distance) compared to short local ones. Additionally, producing high-quality multilayer graphene with numerous layers through chemical vapor deposition (CVD) remains challenging.

Recent studies have examined the application of graphene in Very-Large-Scale Integration (VLSI) design [8-11], revealing that graphene-based interconnections can effectively improve circuit delay as well as power consumption. However, most research has concentrated on Application-Specific Integrated Circuits (ASICs), with less emphasis on Field-Programmable Gate Arrays (FPGAs). FPGAs, comprised of configurable logic blocks (CLBs) interconnected by programmable routing elements, are particularly sensitive to interconnection network performance [12, 13]. The large amount of routing resources required to connect each reconfigurable unit can cause significant delay and energy overhead [14]. Therefore, emerging graphene-based interconnect materials present a promising approach to alleviate these overheads and improve FPGA performance.

Lee et al. investigated the interconnects based on graphene and evaluated its performance across various supply voltages [15]. The experiment indicates that graphene interconnects offer over 200% improvement in speed and 150% enhancement in energy efficiency at low-swing voltages. While this research underscores the potential of graphene-based interconnects, it mainly focuses on low-voltage applications with the circuit operating at a voltage of 0.4V, which involves a trade-off between performance and energy efficiency. Consequently, the benefit of graphene-based interconnects for high-performance FPGA applications remains uncertain. Furthermore, the study fails to consider some pivotal material-level parameters, including the contact resistance between graphene interconnects

and transistors, as well as the mean free path of graphene material. These factors are of particular significance in narrow geometries. The graphene-based interconnects in this work are limited to top metal layers with a 180nm technology node, in contrast, the current mainstream FPGAs employ advanced 7nm processes. This inevitably results in interconnect widths that are so excessively wide that they fail to reflect the advantages of graphene interconnects. To evaluate graphene's benefits, we need to look at how it works with devices and connections at the advanced technology node.

In this paper, we will explore the potential benefits of using multilayer graphene based global routing interconnects in FPGAs within the context of the prevalent 7nm FinFET technology node [16]. Our study will conduct a thorough comparison of three interconnect materials: traditional Cu, graphene-capped Cu, and thick graphene. We will evaluate and benchmark these materials based on their performance characteristics and practical viability. Additionally, we will assess the impact of non-ideal material-level parameters for graphene, such as contact resistance and mean free path, within an interconnect/system co-design framework specifically designed for FPGA systems. To refine our evaluation, we will integrate repeater insertion into interconnect segments, optimizing the number and size of repeaters to minimize the energy-delay product (EDP). By addressing these aspects, our study aims to offer an in-depth analysis of the practical advantages and challenges associated with incorporating multilayer graphene into advanced FPGA designs, emphasizing its potential to enhance performance in high-performance applications.

The primary contributions are outlined below:

- A robust co-design framework is introduced to improve the optimization and evaluation processes of multi-layer graphene interconnects.
- The impact of disparate non-ideal material-level parameters, including contact resistance and MFP, is evaluated for multi-layer graphene interconnects. The performance of these interconnects is then benchmarked against that of Cu and graphene-capped Cu counterparts.

TABLE I
DEVICE-LEVEL ASSUMPTIONS AND METRICS

	Parameter	Value
Electrical Parameters	Vdd (V)	0.75
	Ion (μA)	85.5
	Ron (kΩ)	8.8
	Intrinsic Delay (ps)	0.86
	Switch Energy (fJ)	0.85
	Cg (aF)	44.1
Layout Parameters	Fin/Sheet Pitch (nm)	32
	Gate Pitch (nm)	54
	Inverter Area (μm ²)	0.052

- Results offer valuable insights that facilitate collaboration between interconnect and circuit/system designers, enabling the development of more suitable interconnect materials for enhanced FPGA performance.

I. MODELING APPROACH

In this section, we will first introduce the physical modeling of different material interconnects and compare their performance differences. Then we will explore the improvements that graphene interconnects can bring to FPGA global routing based on the 7nm FinFET technology node. In particular, the circuit model based on graphene interconnect and repeater insertion will be highlighted. Finally, an interconnect/system co-design framework for FPGA using different interconnect materials will be presented.

A. Interconnect Resistance Modeling

There are three interconnect materials that will be examined in this paper: (i) conventional Cu interconnects, (ii) graphene-capped Cu interconnects, where 10 layers of graphene are deposited atop the Cu to reduce the resistance, and (iii) thick graphene interconnects, consisting of a significant number of graphene layers, have their resistance modeled using quantum transport theory in accordance with established methodologies [11]. The mathematical relationship between electrical conductivity, mobility, and mean free path is given by the following semiclassical equation: [17]:

$$\sigma = en\mu = \frac{2e^2}{h}(\sqrt{\pi n} \cdot MFP), \quad (1)$$

where n is carrier density, σ is conductivity, and μ is mobility. At $n \approx 4.85 \times 10^{10} \text{ cm}^{-2}$, the MFP is set as 460 nm for 1μm wide graphene based on the existing work [18]. The MFP is observed to decrease with increasing width, a phenomenon attributed to edge scattering. The mobility as a function of width is extracted based on experimental data [19]. Other than the intrinsic interconnect resistance, an additional contact resistance is added on each side of the interconnect, whose value is $R_{cont}/(WN_{layer})$, where R_{cont} is the contact resistance in the unit of $\Omega \cdot \mu\text{m}$, N_{layer} is the number of graphene layers, and W is the interconnect width.

The resistivity model for Cu follows established work, incorporating a grain boundary reflectivity of 0.5 and a side wall specularity of 0.5 [17]. In terms of graphene-capped Cu interconnects, where electrons experience reduced scattering within the Cu due to the graphene layer, we account for this effect by modeling the grain size as $3\times$ larger, based on experimental data [20, 21]. The capacitance of the interconnects is computed as the series combination of quantum capacitance and electrostatic capacitance.

B. Device-Level Modeling

In this paper, we adopt the CMOS FinFET device metrics at the 7nm technology node based on the 2018 IRDS report [16], and TABLE I provides a summary of the principal electrical parameters and design rules. The corresponding layout and

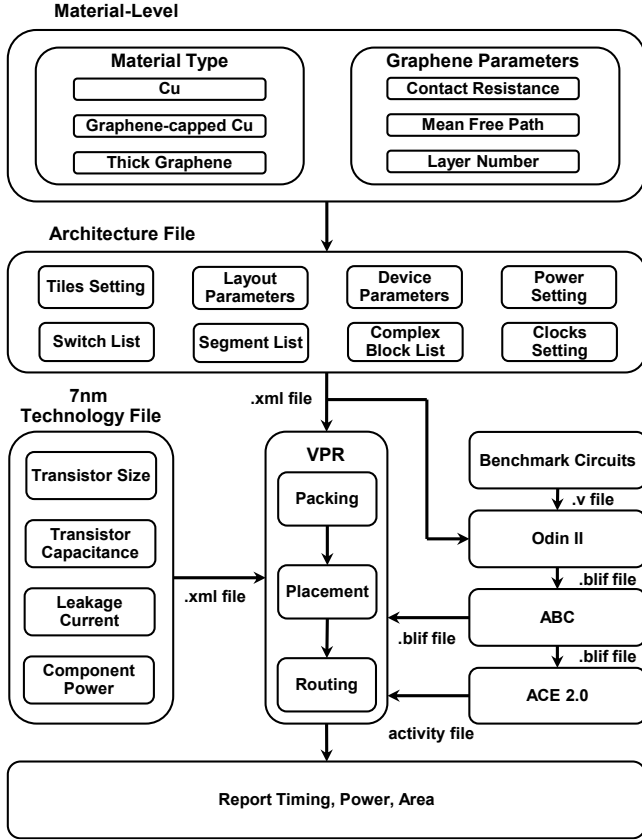


Fig. 1. Technology/system co-design framework for FPGA using different interconnect materials.

geometry of the minimum size transistor are designed in accordance with the layout design rule provided by the report, including the specifications for fin/nanosheet pitch and contacted gate pitch. The transistor area exerts a considerable influence on the system as a whole, as it affects the dimensions of crucial components such as CLBs and switch boxes (SBs). Consequently, this has an impact on the length and width of the interconnecting wires, which will be presented in Section II.

C. System-Level Interconnect Modeling

In order to systematically simulate the FPGA global routing network, we adopt VTR [22], an open-source FPGA simulation platform. In VTR FPGA architecture, CLBs are connected to each other through a connection block (CB), routing channel, and SB. The CB connects CLB inputs and outputs to global routing interconnect wires, and the SB connects vertical and horizontal routing channels. There are several types of switch boxes, the Disjoint style, the Universal style and the Wilton style. Disjoint style has been used in the Xilinx XC4000 series, and Universal style and Wilton style require fewer routing tracks and a smaller logic area [23]. All these styles have trade-offs among performance metrics, and the Wilton style is used in this paper.

The global routing of the FPGA has $W_{channel}$ interconnect segments, which is widely used in VTR and related studies. We assume here that the total width occupied by these $W_{channel}$ interconnects is equal to the width of a single SB. In terms of

interconnect geometry, we set its width W_{wire} equal to the space S_{wire} between neighboring interconnects. Here, the value of 300 is assigned to the number of channels, in accordance with the specifications set forth by the VTR tool [22], the length of a single segment spans 4 CLBs.

D. Repeater Insertion Modeling

To mitigate the quadratic delay dependency on interconnect length, repeaters are inserted at regular intervals along the routing interconnects. It is important to note that the introduction of a repeater into a graphene interconnect will result in the addition of two supplementary contact resistances at the interface between the repeater and the graphene. Consequently, the insertion of an excessive number of repeaters will result in a discernible escalation in the delay overhead. It is therefore imperative to conduct a comprehensive optimization of the repeater insertion process to minimize both delay and energy consumption.

A thick graphene-based interconnect of length H is subjected to a breakage test with K repeaters. The delay and energy of this model are expressed by the following equations:

$$t_d = 0.7R_0 \frac{C_w}{H} + 0.7 \left(\frac{R_q}{2} + R_{cont} \right) C_w + 0.4R_w \frac{C_w}{K} + 0.7R_0 C_0 K \quad (2)$$

$$+ 0.7(R_q + 2R_{cont})C_0 HK + 0.7R_w C_0 H + 0.7R_0 \frac{C_{load}}{H},$$

$$E = 0.5(C_w + C_0 HK + C_{load})V_{dd}^2, \quad (3)$$

where R_w and C_w are wire resistance and capacitance of a unit length segment, R_0 and C_0 are the repeater resistance and capacitance, respectively, R_q is the quantum resistance, C_{load} refers to the load capacitance of the buffers or MUXes that are connected to the interconnect wire. In this paper, we select EDP as the metric for optimization.

E. Interconnect /System Co-Design Framework

In order to facilitate the translation of interconnect material-level parameters to system-level performance and enable the exploration of an efficient and expansive design space, we have developed a framework for the co-design of interconnect technology and systems [24], as shown in Fig. 1. First, the corresponding FPGA architecture files are generated based on the aforementioned interconnect model. In this process, material parameters such as the contact resistance of graphene and the MFP are taken into account as variables, which contain the settings of the unit length interconnect's resistance, capacitance, and other important parameters. Then, for a given circuit, an open-source tool, Odin II [25], is used to transform Verilog files into BLIF netlist files. Subsequently, the open-source synthesis tool, known as ABC, is employed to transform the netlist circuit into a 6-input LUT structure [26]. Following that, VPR is used to perform LUT clustering, placement, and routing [22]. In order to calculate the switching of energy calculations, the activity files are generated by ACE2.0 [27], this process generates

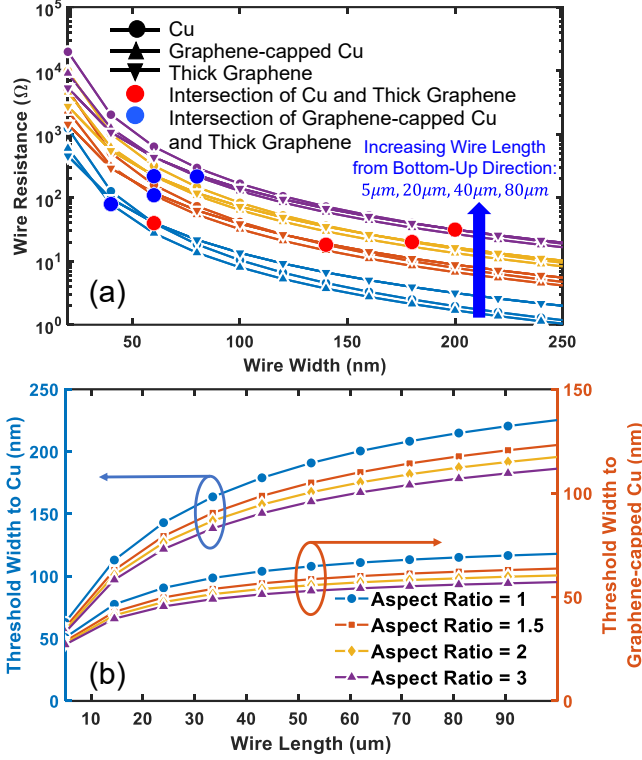


Fig. 2. (a) Interconnect resistance vs. width for different wire lengths. The red/blue dots show the width at which Cu/graphene-capped Cu and thick graphene have the equal wire resistance with an aspect ratio of 1.5. (b) shows the width at which thick graphene provides the same resistance as Cu and graphene-capped Cu, respectively, as a function of length with different aspect ratios. The left y-axis shows the difference in width between thick graphene and Cu, while the right y-axis shows the difference between thick graphene and graphene-capped Cu. In this case, the thick graphene contact resistance is $100 \Omega \cdot \mu\text{m}$.

activity factors for each node in the FPGA system, based on the circuit netlist generated by ABC. To assess the performance of the proposed methodology, several representative circuits with varying sizes are selected from the IWLS 2005 benchmark [28].

II. SIMULATION RESULTS

In this section, we will quantitatively analyze the simulation results based on different interconnect materials. First, we will analyze the material-level performance between three different interconnect materials. Then we will analyze the simulation results for a single FPGA segment, and finally, we will analyze the simulation results at the FPGA system level, focusing on the graphene contact resistance as well as the effect of MFP on the system level.

A. Material-level Performance Comparison

1) Threshold Width Analysis

Based on the previously discussed modeling, we proceed to assess the impact of interconnect width and length on the interconnect resistance. This analysis is illustrated in Fig. 2. The resistance of all three materials demonstrates an increase as the interconnect width is reduced. This phenomenon is especially pronounced in the case of Cu interconnects, which exhibit

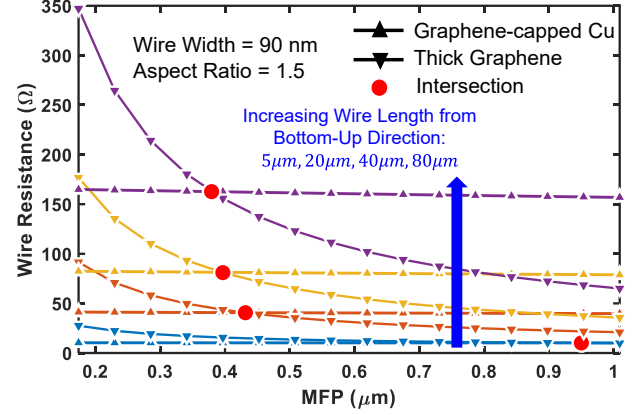


Fig. 3. Relationship between MFP and wire resistance with different wire length.

considerable size effects due to their intrinsic resistivity characteristics. As illustrated in Fig. 2(a), the red/blue dots indicate the intersections between Cu/thick graphene and graphene-capped Cu/thick graphene, respectively. It is evident that when the width of the wire is less than the aforementioned threshold width, defined as the point at which graphene exhibits lower resistance, the material is more suitable for use in narrow wires.

Fig. 2(b) illustrates the relationship between threshold interconnect width and interconnect length across various aspect ratios. The results indicate that the threshold width increases with interconnect length, suggesting that thick graphene has superior tolerance compared to traditional materials. Moreover, interconnects with smaller aspect ratios exhibit a larger threshold width, highlighting that traditional Cu interconnects are more susceptible to size effects as the aspect ratio decreases. This behavior underscores the benefits of using thick graphene for improved performance in longer interconnects and with varying aspect ratios.

2) Graphene Effective MFP Influence

Unlike copper wires, which typically have an MFP of approximately 39 nm [29], high-quality graphene can achieve an MFP of up to several micrometers or even longer. The exact length of the MFP depends on specific experimental conditions and the quality of the graphene material. Here we take a conservative range of values considering the difficulties that may be faced in practical large-scale manufacturing, as shown in Fig. 3, which is the relationship between the graphene-capped Cu as well as the thick graphene resistance with the MFP values in the case of $0.1 \sim 1 \mu\text{m}$. Fig. 3 illustrates that both graphene-capped Cu and thick graphene interconnects are affected by their MFP values, with thick graphene demonstrating a more pronounced impact. The larger MFP value can effectively reduce the resistance of thick graphene, making thick graphene even more suitable for shorter local interconnects.

B. Single Interconnect Performance Comparison

In alignment with the interconnect model featuring repeater insertion outlined in Section II, we conduct a quantitative

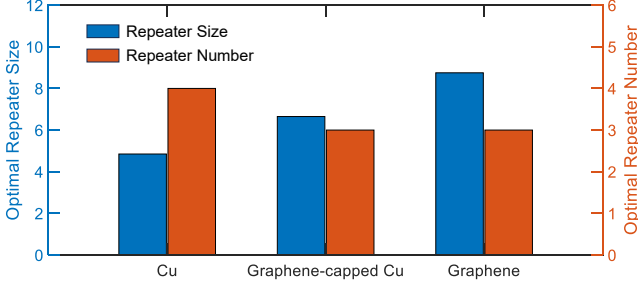


Fig. 4. Optimal number and size of repeaters to minimize EDP for Cu, graphene-capped Cu, and thick graphene under 7nm FinFET technology node.

analysis to evaluate the performance of three different interconnect materials across varying MFP values. In this analysis, the aspect ratio of the interconnect is held constant at 1.5, while the interconnect length is set to match the width of a single CLB. To achieve optimal performance, the number and size of repeaters are adjusted to minimize the EDP. Fig. 4 shows the optimal number and size of repeaters for a single CLB length, aimed at minimizing the EDP. The results indicate that, due to the additional contact resistance associated with graphene, fewer but larger repeaters are more effective for graphene interconnects compared to copper and copper-capped graphene interconnects.

As shown in Fig. 5(a), graphene-capped Cu and thick graphene interconnects, with the baseline MFP, are shown to achieve up to 26% and 33% delay reduction, respectively, compared to conventional Cu interconnects at the 7nm technology node. As fabrication techniques advance, both the quality of graphene and its MFP are expected to improve further [30, 31]. Here, we aim to quantify the potential benefits of graphene if its MFP is to be improved by a factor of two or three. This analysis will provide a compelling rationale for researchers to invest in the development of high-quality graphene. Fig. 5(a) illustrates that graphene with a $2\times$ baseline MFP and a $3\times$ baseline MFP exhibits a reduction in delay of up to 28% and 40%, respectively, in comparison to its baseline MFP counterpart at the 7nm technology node.

In terms of switching energy, Fig. 5(b) shows that the energy consumption for graphene-based interconnects remains nearly constant as the MFP increases from the baseline to three times the baseline. Furthermore, there is no notable discrepancy in energy consumption among the various interconnects, as the energy is predominantly influenced by the fixed interconnect capacitance, given that all interconnects have an identical wire length. Fig. 5(c) illustrates the variations in overall EDP among the three interconnect technologies. At the 7nm technology node with the baseline MFP, graphene-capped Cu and thick graphene achieve up to 26% and 35% reductions in EDP, respectively, compared to traditional Cu interconnects. These improvements become even more significant with increased MFP, with graphene-capped Cu and thick graphene demonstrating reductions of 33% and 61%, respectively, when the MFP is three times the baseline.

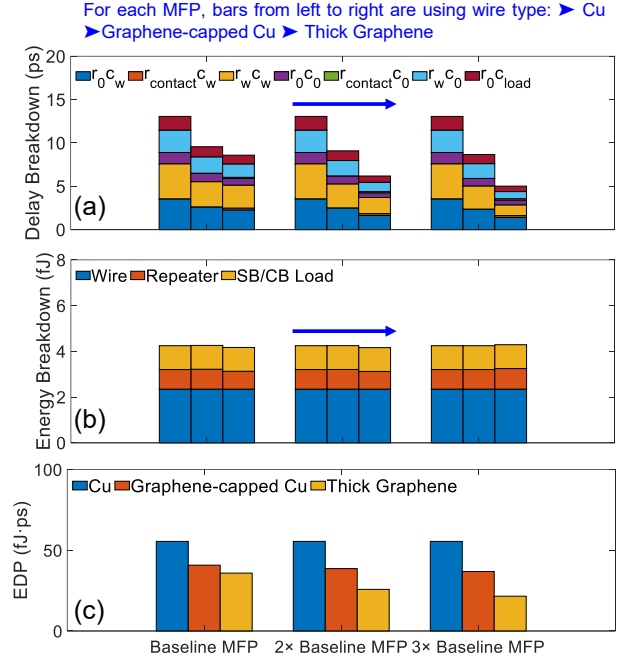


Fig. 5. Comparison of (a) delay breakdown, (b) energy breakdown, and (c) EDP of a single interconnect using three materials under various MFP values. Here, the contact resistance is set to $100\Omega\cdot\mu\text{m}$.

C. Impact of Material-Level Parameters of Graphene

In this subsection, we explore how key material-level parameters of graphene affect overall FPGA system performance. The default settings are a 7nm technology node, a contact resistance of $100\Omega\cdot\mu\text{m}$, and 300 routing channels, unless stated otherwise.

1) Graphene Contact Resistance

As illustrated by the RC model described in Section II D, there is a non-negligible contact resistance when graphene interconnects are connected to the device. The value of this contact resistance is highly dependent on the fabrication process and can vary significantly [32]. To quantify the impact of contact resistance on the overall performance of the interconnects, Fig. 6 illustrates the overall performance across a range of contact resistance values, from $100\Omega\cdot\mu\text{m}$ to $2000\Omega\cdot\mu\text{m}$. The results show that even at high contact resistance levels (e.g., $500\Omega\cdot\mu\text{m}$), graphene interconnects continue to outperform both Cu and graphene-capped Cu interconnects (represented by the first two bars).

2) Graphene Effective MFP

Graphene interconnect modeling reveals that MFP significantly affects graphene conductivity and FPGA system performance, as shown in Fig. 7. An increased MFP reduces both local and global route delays by lowering wire resistance (Fig. 7(a)). Improved global routing efficiency allows for better distribution of BLEs across CLBs, raising the number of switch boxes and shifting more energy consumption to these components and the wiring Fig. 7(b)). Enhancing the MFP by a factor of 3 could reduce overall EDP by up to 20% compared to the baseline MFP, highlighting the importance of advancing

For each netlist, bars from left to right are using: Cu ➤ Graphene-capped Cu ➤ Thick Graphene with $R_{\text{cont}} = 100\Omega \cdot \mu\text{m}$ ➤ $R_{\text{cont}} = 500\Omega \cdot \mu\text{m}$ ➤ $R_{\text{cont}} = 1000\Omega \cdot \mu\text{m}$ ➤ $R_{\text{cont}} = 2000\Omega \cdot \mu\text{m}$

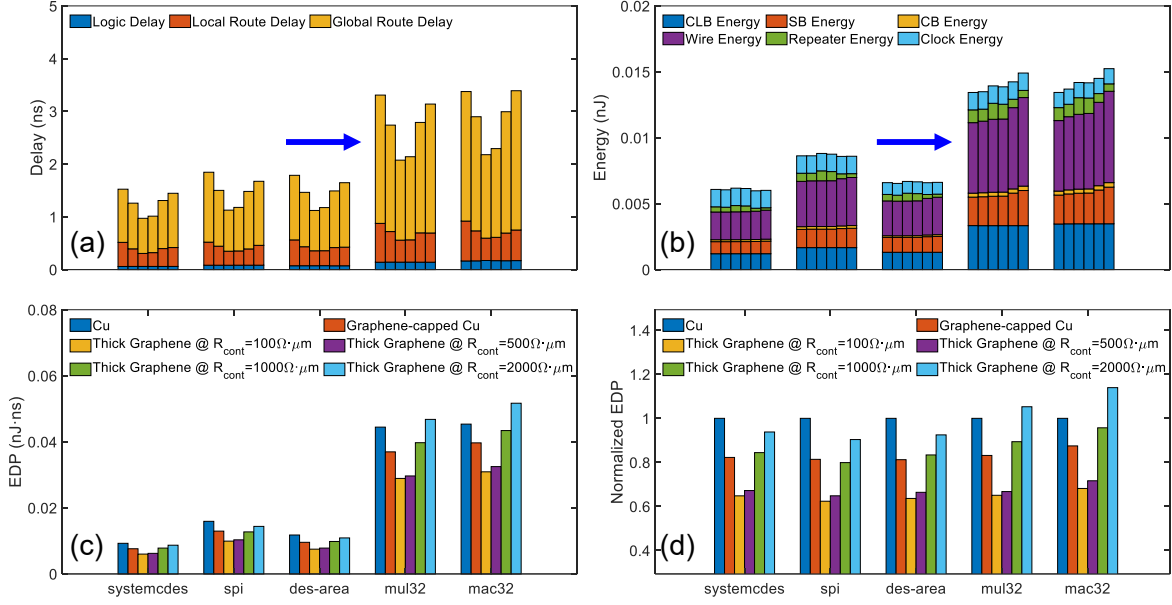


Fig. 6. Comparison (a) delay breakdown, (b) energy breakdown, (c) EDP, and (d) normalized EDP among three interconnect materials under various contact resistance.

For each netlist, bars from left to right are using wire type: ➤ Cu ➤ Graphene-capped Cu ➤ Thick Graphene with Baseline MFP ➤ 2× Baseline MFP ➤ 3× Baseline MFP

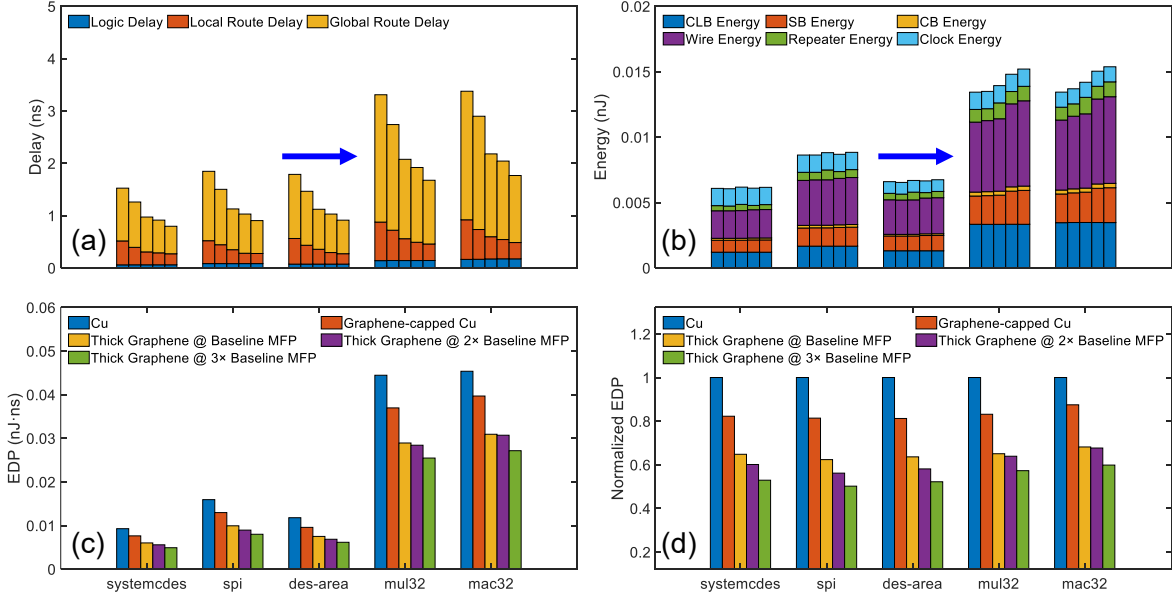


Fig. 7. Comparison (a) delay breakdown, (b) energy breakdown, (c) EDP, and (d) normalized EDP among three interconnect materials under various MFP values.

manufacturing to produce thick graphene with longer MFP for better performance.

III. CONCLUSION

This paper theoretically examines the advantages of graphene-based interconnects for global FPGA routing. It shows that material parameters such as mean free path and contact resistance significantly impact FPGA performance. At the 7nm technology node, graphene interconnects reduce delay by 35%

and EDP by 32% compared to conventional Cu interconnects, with greater benefits expected as technology advances. These findings highlight the importance of graphene quality in improving FPGA performance and energy efficiency. Future work should aim to achieve a contact resistance below $500 \Omega \cdot \mu\text{m}$ and higher mean free path values.

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REFERENCES

- [1] T. Zhan *et al.*, "Effect of thermal boundary resistance between the interconnect metal and dielectric interlayer on temperature increase of interconnects in deeply scaled VLSI," *ACS applied materials & interfaces*, vol. 12, no. 19, pp. 22347-22356, 2020, doi: 10.1021/acsami.0c03010.
- [2] T. Gupta *et al.*, *Copper interconnect technology*. Springer Science & Business Media, 2010.
- [3] D. Josell *et al.*, "Size-dependent resistivity in nanoscale interconnects," *Annual Review of Materials Research*, vol. 39, no. 1, pp. 231-254, 2009.
- [4] A. E. Kaloyeros *et al.*, "Review—Cobalt Thin Films: Trends in Processing Technologies and Emerging Applications," *ECS Journal of Solid State Science and Technology*, vol. 8, no. 2, pp. P119-P152, 2019.
- [5] A. A. Vyas *et al.*, "On-chip interconnect conductor materials for end-of-roadmap technology nodes," *IEEE Transactions on Nanotechnology*, vol. 17, no. 1, pp. 4-10, 2016.
- [6] R. Murali *et al.*, "Breakdown current density of graphene nanoribbons," *Applied Physics Letters*, vol. 94, no. 24, 2009, doi: 10.1063/1.3147183.
- [7] H. Sharma, "Graphene Nanoribbon for Future VLSI Applications: A Review," *Integrated Devices for Artificial Intelligence and VLSI*, pp. 101-123, 2024, doi: 10.1002/9781394205158.ch5.
- [8] C. Pan *et al.*, "System-level performance optimization and benchmarking for on-chip graphene interconnects," in *2012 IEEE 21st Conference on Electrical Performance of Electronic Packaging and Systems*, 2012: IEEE, pp. 33-36, doi: 10.1109/EPEPS.2012.6457837.
- [9] N. C. Wang *et al.*, "Replacing copper interconnects with graphene at a 7-nm node," in *2017 IEEE International Interconnect Technology Conference (IITC)*, 2017: IEEE, pp. 1-3, doi: 10.1109/IITC-AMC.2017.7968949.
- [10] C. Pan *et al.*, "Technology/circuit/system co-optimization and benchmarking for multilayer graphene interconnects at sub-10-nm technology node," *IEEE Transactions on Electron Devices*, vol. 62, no. 5, pp. 1530-1536, 2015, doi: 10.1109/TED.2015.2409875.
- [11] Z. Pei *et al.*, "Graphene-based interconnect exploration for large SRAM caches for ultrascaled technology nodes," *IEEE Transactions on Electron Devices*, vol. 70, no. 1, pp. 230-238, 2022, doi: 10.1109/TED.2022.3225512.
- [12] V. Betz *et al.*, *Architecture and CAD for deep-submicron FPGAs*. Springer Science & Business Media, 2012.
- [13] E. Ahmed *et al.*, "The effect of LUT and cluster size on deep-submicron FPGA performance and density," in *Proceedings of the 2000 ACM/SIGDA eighth international symposium on Field programmable gate arrays*, 2000, pp. 3-12, doi: 10.1145/329166.329171.
- [14] M. Lin *et al.*, "Performance benefits of monolithically stacked 3D-FPGA," in *Proceedings of the 2006 ACM/SIGDA 14th international symposium on Field programmable gate arrays*, 2006, pp. 113-122, doi: 10.1145/1117201.1117219.
- [15] K.-J. Lee *et al.*, "Demonstration of a subthreshold FPGA using monolithically integrated graphene interconnects," *IEEE Transactions on Electron Devices*, vol. 60, no. 1, pp. 383-390, 2012, doi: 10.1109/TED.2012.2225150.
- [16] "International Roadmap for Devices and Systems (IRDS™) 2022 Edition." <https://irds.ieee.org/editions/2022> (accessed July. 27, 2024).
- [17] K. I. Bolotin *et al.*, "Ultrahigh electron mobility in suspended graphene," *Solid state communications*, vol. 146, no. 9-10, pp. 351-355, 2008, doi: 10.1016/j.ssc.2008.02.024.
- [18] S. Achra *et al.*, "Characterization of interface interactions between graphene and ruthenium," in *2020 IEEE International Interconnect Technology Conference (IITC)*, 2020: IEEE, pp. 133-135, doi: 10.1109/IITC47697.2020.9515595.
- [19] X. Wu *et al.*, "Graphene Interconnects-High Performance Twisted 20 nm Graphene Ribbons," in *2018 IEEE International Interconnect Technology Conference (IITC)*, 2018: IEEE, pp. 25-27, doi: 10.1109/IITC.2018.8430432.
- [20] H. C. Lee *et al.*, "Toward near-bulk resistivity of Cu for next-generation nano-interconnects: Graphene-coated Cu," *Carbon*, vol. 149, pp. 656-663, 2019, doi: 10.1016/j.carbon.2019.04.101.
- [21] T. Yu *et al.*, "Bilayer graphene/copper hybrid on-chip interconnect: A reliability study," *IEEE transactions on nanotechnology*, vol. 10, no. 4, pp. 710-714, 2010, doi: 10.1109/TNANO.2010.2071395.
- [22] K. E. Murray *et al.*, "Vtr 8: High-performance cad and customizable fpga architecture modelling," *ACM Transactions on Reconfigurable Technology and Systems (TRETS)*, vol. 13, no. 2, pp. 1-55, 2020, doi: 10.1145/3388617.
- [23] G. G. Lemieux *et al.*, "Analytical framework for switch block design," in *Field-Programmable Logic and Applications: Reconfigurable Computing Is Going Mainstream: 12th International Conference, FPL 2002 Montpellier, France, September 2-4, 2002 Proceedings 12*, 2002: Springer, pp. 122-131.
- [24] C. Pan *et al.*, "A fast system-level design methodology for heterogeneous multi-core processors using emerging technologies," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 5, no. 1, pp. 75-87, 2015, doi: 10.1109/JETCAS.2015.2398218.
- [25] P. Jamieson *et al.*, "Odin ii-an open-source verilog hdl synthesis tool for cad research," in *2010 18th IEEE Annual International Symposium on Field-Programmable Custom Computing Machines*, 2010: IEEE, pp. 149-156, doi: 10.1109/FCCM.2010.31.
- [26] R. Brayton *et al.*, "ABC: An academic industrial-strength verification tool," in *Computer Aided Verification: 22nd International Conference, CAV 2010, Edinburgh, UK, July 15-19, 2010. Proceedings 22*, 2010: Springer, pp. 24-40, doi: 10.1007/978-3-642-14295-6_5.
- [27] J. Lamoureux *et al.*, "Activity estimation for field-programmable gate arrays," in *2006 International Conference on Field Programmable Logic and Applications*, 2006: IEEE, pp. 1-8, doi: 10.1109/FPL.2006.311199.
- [28] C. Albrecht, "IWLS 2005 benchmarks," in *International Workshop for Logic Synthesis (IWLS)*, 2005, vol. 9.
- [29] D. Gall, "Electron mean free path in elemental metals," *Journal of applied physics*, vol. 119, no. 8, 2016.
- [30] L. Banszerus *et al.*, "Ballistic transport exceeding 28 μm in CVD grown graphene," *Nano letters*, vol. 16, no. 2, pp. 1387-1391, 2016, doi: 10.1021/acs.nanolett.5b04840.
- [31] M. D. Bachmann *et al.*, "Directional ballistic transport in the two-dimensional metal PdCoO₂," *Nature Physics*, vol. 18, no. 7, pp. 819-824, 2022, doi: 10.1038/s41567-022-01570-7.
- [32] S. Aslanidou *et al.*, "Electronic interface and charge carrier density in epitaxial graphene on silicon carbide. A review on metal-graphene contacts and electrical gating," *APL Materials*, vol. 8, no. 10, 2020, doi: 10.1063/5.0022341.