A Study on NBTI-induced Delay Degradation Considering Stress Frequency Dependence

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***Abstract*—The degradation of transistors in integrated circuits is known to be dependent on stress frequency in addition to the well-known stress duty cycle. This paper analyzes the impact of frequency dependence of the NBTI degradation on a processor-scale circuit under various workload scenarios by using different levels of available information. A simple estimation for wire switching frequency from duty cycle is also proposed. Using real workloads running on MIPS processor, it is found that frequency dependency of the worst path delay is not large since there are many DC stress components independent of frequency. However, frequency dependency of path delay increases when DC component decreases due to execution of multiple applications.**

I. Introduction

Negative bias temperature instability (NBTI) is one of the most serious reliability threats for miniaturized integrated circuits. The NBTI degradation increases threshold voltage ($V_{\rm th}$) of pMOS transistors that compose the logic gates. The rise in the threshold voltage increases path delay, which may result in a delay fault while the chip is used in various systems. The accurate lifetime estimation of the chip is hence becoming increasingly important.

The degradation due to NBTI is enhanced by higher temperature and stronger negative voltage applied to the gate terminal of pMOS transistors. The degraded threshold voltage recovers partially, during the period in which the negative stress bias of the transistor is removed. In order to quantitatively estimate the impact of NBTI, various models have been proposed [1]–[11]. Two major models for NBTI are the reaction-diffusion (RD) model [2]–[4] and the hole-trapping (HT) model [5]–[8].

In the RD model, the degradation mechanism is explained by the generation of interface trap [3,4]. Hydrogen ions are separated from Si-SiO_2 interface and diffuse into the gate oxide film when the negative bias is applied to the gate electrode. The hydrogen ion recombines with the silicon at the interface when the application of the negative bias is removed. This recombination causes threshold voltage recovery. On the other hand, the HT mechanism [5] is explained by trapping of holes in pre-existing defects at Si-SiO_2 interface. Most of the existing models consider only one of the two mechanisms. Using the RD model, the rapid recovery of the threshold voltage cannot be fully explained because diffusion of hydrogen ion in oxide is generally a slow process even under a strong recovery stress. On the other hand, the HT model cannot necessarily explain permanent component of the degradation, which is widely observed through measurements and reported in various literature. Hence, the models that combine the two mechanisms are recently proposed [9,10].

It is well known that NBTI degradation depends strongly on chip temperature, supply voltage, and stress probability [3, 8,10]. In most applications, temperature and voltage of a chip can be considered constant over the period of circuit operation, or the worst case condition is applied to guardband the aging effect. On the other hand, the stress probability, or stress duty, which is defined as the period of a wire being in stress condition divided by the entire period of chip operation, varies from transistor to transistor as the change of workloads and data patterns given to the circuit. Hence, various techniques have been proposed trying to estimate or to mitigate the effect of NBTI, considering the stress probability as the most important variable [12]. However, in other literature, it is claimed that the stress frequency of a transistor cannot be ignored when the hole trapping model is assumed, particularly when the circuit operates at a low frequency [10,11].

In this paper, the timing degradation of a processor is quantitatively analyzed by simultaneously considering stress probability and stress frequency. As a result of this study, the following insights on the NBTI induced delay degradation are derived.

- Frequency dependence of delay degradation in the worst path delay is not so significant because most of the gates in such paths are given DC stress, which is independent of frequency, but application of mitigation techniques may change the significance.
- Frequency dependence of delay degradation becomes large when multiple applications are executed.
- By a simple calculation of frequency using duty cycle gives reasonably good approximation of frequency dependent delay.

This paper is organized as follows. In Section II, the degradation models for NBTI that are used in this work are described. In Section III, the evaluation method of frequency dependence on circuit degradation is proposed. Then, in Section IV, evaluation results of path delay degradation were proposed. Finally, the paper is concluded in Section V.

II. NBTI Model

The RD and HT mechanisms are two most widely recognized degradation models for NBTI. In recent study, degradation due to the HT mechanism is reported to be strongly frequency-dependent [10,11] in addition to the duty cycle. Thus, the NBTI model that is based on the HT mechanism is considered in our study. In the HT mechanism [8], threshold voltage shift caused by NBTI is represented as follows:

$$|\Delta V_{\rm th}| = \phi_1[A + B\log(1 + C\alpha T_{\rm clk})]\frac{1}{1-\beta_1\beta_2} + \phi_2[A + B\log(1 + C(1-\alpha)T_{\rm clk})]\frac{\beta_1}{1-\beta_1\beta_2}. \quad (1)$$

Here, β_1 and β_2 are defined as

$$\beta_1 = 1 - \frac{k + \log(1 + C\alpha T_{\rm clk})}{k + \log(1 + C(t + C\alpha T_{\rm clk}))}, \text{ and} \quad (2)$$

$$\beta_2 = 1 - \frac{k + \log(1 + C(1-\alpha) T_{\rm clk})}{k + \log(1 + C(t + C\alpha T_{\rm clk}))}, \quad (3)$$

where $T_{\rm clk}$, α, and t are the clock period, the duty cycle, and the time, respectively. C and k are the fitting parameters for the stress and the recovery.

It is known that (1) cannot predict large threshold voltage shift caused by DC stress very well. Hence, instead using (1), we use (4) for the threshold voltage degradation of the DC stress condition [3,4].

$$|\Delta V_{\rm th}(t)| = (K_v^2 t)^n. \quad (4)$$

Here, K_v is a function of the gate-source voltage $V_{\rm gs}$, the initial threshold voltage $V_{\rm th}$, and the temperature T. n is determined as a diffusion constant, which typically takes the value in between 1/4 and 1/6.

By applying (1) and (4) to the Nangate 45 nm Open Cell Library [13], the relationship among the duty cycle, clock frequency, and the threshold voltage degradation is obtained as shown in Figs. 1 and 2. The parameters in (4) are determined according to [3,4], which are also used in other literatures such as [12,14]. In addition, the parameters in (1) are determined from the recent actual measurement data [10]. In the data, $\Delta V_{\rm th}$ of $\alpha = 1.0$ at DC is about 2.5 times as large as $\Delta V_{\rm th}$ of $\alpha = 1.0$ at $f_{\rm net} = 1\,{\rm MHz}$. Also, $\Delta V_{\rm th}$ of $f_{\rm net} = 1\,{\rm MHz}$ and $\alpha = 0.5$ is about 1.5 times as large as $\Delta V_{\rm th}$ of $f_{\rm net} = 1\,{\rm kHz}$ and $\alpha = 0.5$. These trends of measured data [10] is shown in Figs. 1 and 2.

In addition to the above example, unignorable frequency dependence of NBTI degradation is reported in recent publications [10,11]. However, no study has investigated the impact of frequency dependence of NBTI upon path delay degradation. Thus, we quantitatively evaluate the frequency dependence of path delay degradation using an actual processor circuit and using the models based on measured data. We also experimentally try to clarify how we can efficiently and effectively include the effect of frequency dependency in NBTI-aware timing analysis.

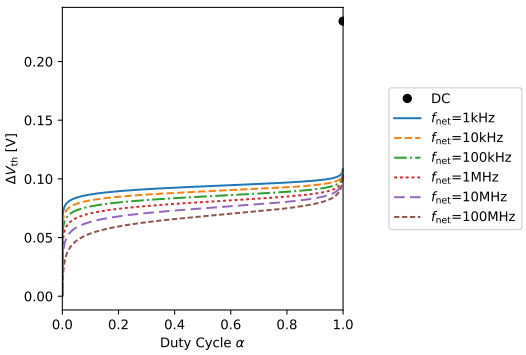


Fig. 1. Threshold voltage degradation as a function of duty cycle for Nangate Open Cell Library [13].

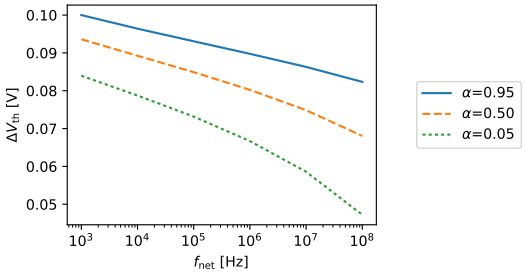


Fig. 2. Threshold voltage degradation as a function of operation frequency for Nangate Open Cell Library [13].

III. Evaluation Method

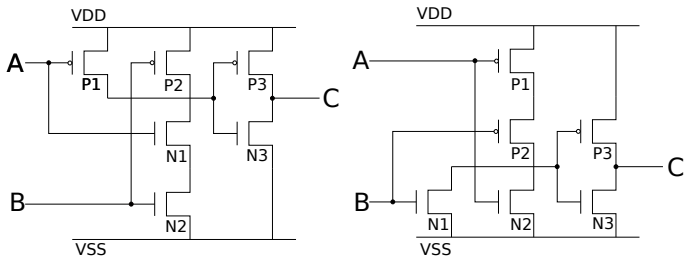
A. Frequency Consideration Scenarios

Considering the typical design flow for logic circuits, there are several scenarios to include frequency dependence in the NBTI degradation, on the basis of different information available. In what follows, we compare the frequency dependence of path delay degradation under the following three conditions:

- Cond-1: Annotate a common constant frequency for all the transistors in the circuit.
- Cond-2: Annotate a frequency for each transistor; the frequency is determined as a corresponding frequency to the separately calculated duty cycle.
- Cond-3: Annotate a simulated frequency for each transistor.

In Cond-1, the frequency dependence of the degradation is reflected by annotating the half of the global clock frequency for all the transistors in the circuit. The frequency difference among transistors is entirely ignored. This condition should yield the minimum degradation possible because degradation increases in inversely proportional to the frequency.

In Cond-2, the frequency for each net is calculated by its duty cycle. This frequency calculation is considered handy and practical, when toggle information obtained by logic simulations is available for use to calculate the duty cycle. By assuming signal transition occurs almost evenly during the operation, the calculated duty cycle can be translated into



(a) AND (b) OR

Fig. 3. Schematics of a 2-input AND and a 2-input OR gates.

TABLE I
DUTY CYCLE OF EACH TRANSISTOR IN AND AND OR GATES

Circuit	P1	P2	P3
AND	$1-\alpha_{\mathrm{A}}$	$1-\alpha_{\mathrm{B}}$	$\alpha_{\mathrm{A}}\alpha_{\mathrm{B}}$
OR	$1-\alpha_{\mathrm{A}}$	$1-\alpha_{\mathrm{B}}$	$1-(1-\alpha_{\mathrm{A}})(1-\alpha_{\mathrm{B}})$

the frequency. For example, consider an input of a gate with duty ratio of 0.5, in which the input signal toggles at every clock cycle. The corresponding frequency of this example is the clock frequency. Another example is an input of a gate that is turned ON once in every 10 clock period, i.e., the duty cycle is 0.1. Its frequency is considered 1/10 of the clock frequency. Thus, the max frequency in a certain frequency is calculated from the operating frequency f_{op} and the duty cycle α by the following formula:

$$f_{\mathrm{net}} = F_2(\alpha) = \begin{cases} 2f_{\mathrm{op}}\alpha & (\alpha \leq 0.5) \\ 2f_{\mathrm{op}}(1-\alpha) & (\alpha > 0.5) \end{cases}. \quad (5)$$

The duty cycle of each transistor are calculated from the result of logic simulation by the following procedure [12]. First, the duty cycle of each wire are obtained from the logic simulation. Then, the duty cycles of the transistors inside the logic gate instance are calculated from the duty cycle of the input. For example, assume a 2-input AND and a 2-input OR gates shown in Fig. 3. The duty cycles of the inputs are obtained from logic simulation. If the duty cycle of inputs A and B are available as α_{A} and α_{B}, respectively, the duty cycle of each transistor in the logic gates can be calculated by using Table I.

In Cond-3, both the frequency and the duty cycle of each transistor are annotated using the result of logic simulation. This condition should give the most accurate estimation. The toggle count of the input and output pins are obtained from the logic simulation, in addition to the duty cycles as in the case of Cond-2. From the toggle count Tc and logic simulation time t_{sim}, the frequency of the transistor is calculated by

$$f_{\mathrm{net}} = \frac{\mathrm{Tc}}{2t_{\mathrm{sim}}}. \quad (6)$$

In this study, we use logic gate instances whose transistors are connected directly to input or output of the instances. Thus, we can obtain frequencies of all the transistors by the logic simulation only.

The toggle counts of the AND and OR gates in Fig. 3 calculated by Cond-1, 2, and 3 are summarized in Table II.

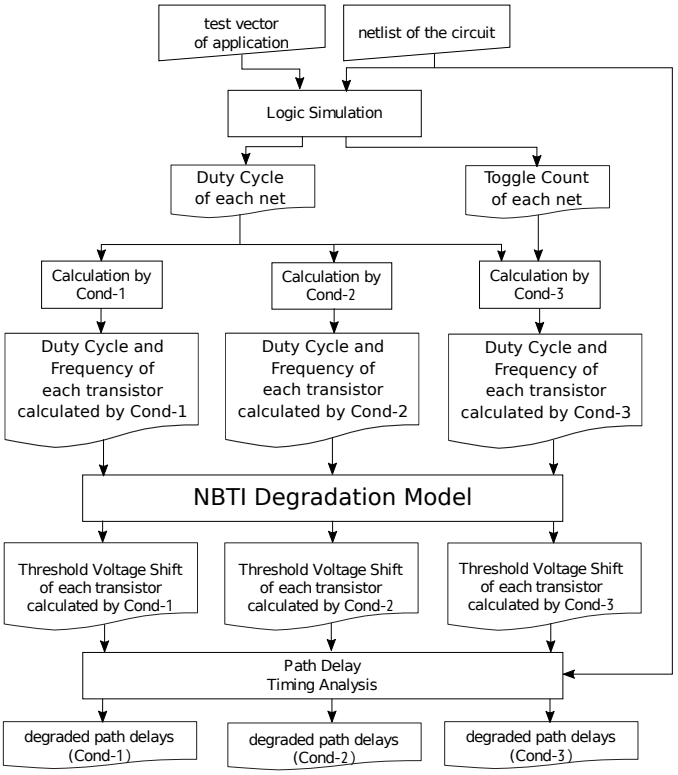


Fig. 4. NBTI-aware timing analysis flow to evaluate frequency dependence.

B. Evaluation of Path Delay Degradation

The delay degradation due to NBTI is calculated by using the flow shown in Fig. 4. First, logic simulation on a target circuit is conducted at a gate-level to obtain toggle count and duty cycle of each wire. Second, the threshold voltage shift ΔV_{th} of each transistor is calculated according to Cond-1, Cond-2 and Cond-3. The threshold voltage shift ΔV_{th} for each transistor is then annotated to the SPICE netlist. Finally, path delay is calculated through circuit simulation, and the path delay degradation is obtained. By comparing the results with those of the timing analysis in a fresh state, we obtain the degradation amounts of the path delays by Cond-1, Cond-2 and Cond-3, respectively.

IV. NUMERICAL EVALUATION

A. Evaluation Setup

The delay degradation for each condition is obtained by using a five-stage pipelined processor [15] that implements the full MIPS32 instruction set with a co-processor handling exceptions. In the experiment, Nangate 45nm Open Cell Library [13] is used for circuit synthesis and the processor is synthesized by logic-synthesis tool [16]. The operation frequency of the targeted CPU is 50 MHz. A subset of the application programs in the MiBench [17] and high-level C sources in GAUT [18] is selected to carry out logic simulation by using a commercially available simulator [19]. The simulated application programs are listed in Table III. Here, "multiple applications" is the consecutive execution of the

TABLE II
TOGGLE COUNT OF EACH TRANSISTOR IN COND-1, 2, AND 3

Cond	Circuit	P1	P2	P3
1	AND	$f_{\rm op}$	$f_{\rm op}$	$f_{\rm op}$
	OR	$f_{\rm op}$	$f_{\rm op}$	$f_{\rm op}$
2	AND	$F_2(1-\alpha_{\rm A})$	$F_2(1-\alpha_B)$	$F_2(\alpha_A\alpha_B)$
	OR	$F_2(1-\alpha_{\rm A})$	$F_2(1-\alpha_{\rm B})$	$F_2(\alpha_{\rm A}+\alpha_{\rm B}+\alpha_{\rm A}\alpha_{\rm B})$
3	AND	${\rm Tc_A}/2t_{\rm sim}$	${\rm Tc_B}/2t_{\rm sim}$	${\rm Tc_C}/2t_{\rm sim}$
	OR	${\rm Tc_A}/2t_{\rm sim}$	${\rm Tc_B}/2t_{\rm sim}$	${\rm Tc_C}/2t_{\rm sim}$

TABLE III
APPLICATION PROGRAMS AND THEIR RUNTIMES

Application	Simulation period
cordic	25,460 ns
fft	880,360 ns
multiple applications	2,952,600 ns

applications: cordic, fft, conv3x3, lms, qsor, sieve, sobel, and aes. As a result of logic simulation, toggle count and duty cycle of each wire are obtained from a switching activity interchange format (SAIF) file. In the timing analysis, commercial SPICE tool [20] is used.

B. Distribution of Duty Cycle and Frequency

In Fig. 6, the distribution of duty cycle and frequency for all the wires is presented for fft. In this figure, all the toggle activities in the logic simulation are considered to calculate the frequency of the wires. In both applications, the first observation is the symmetry in the distribution at about $\alpha = 0.5$. This symmetry is introduced by the inverting nature of CMOS logic gates. When there is a net whose duty cycle is α, the inverting logic that is driven by the net can be found nearby and which gives a duty cycle of $1-\alpha$. The second observation is that there are many wires (indicated using dark color in the figure) whose duty cycles are at about $\alpha = 0.5$ and whose activities are relatively high. Most of these nets are found inside the ALU. In addition, we observe that there are a large number of wires that are inactive — either at $\alpha \sim 0$ or $\alpha \sim 1$. Most of these wires did not change their values at all during the application runtime. The paths that include such inactive wires and gates tend to suffer from large delay degradation, and possibly be a part of *invariant paths* [14]. In (5), a linear relationship is assumed in between the duty cycle and the frequency. The relationship represents the above symmetric property about $\alpha = 0.5$ and serves as relatively good approximation as indicated by dashed lines. When the applications are compared, fft requires longer runtime and more number of high activity wires are found. Hence, as we will see later, the frequency dependence should become larger for fft than for cordic.

In order to evaluate actual activity in the circuit, distribution of the duty cycles for all the wires is plotted for fft and multiple applications in Fig. 5. The most of the wires are inactive, and 17.8% of the wires are evaluated to be in $\alpha > 0.99$ or $\alpha < 0.01$ in the case of fft. Running the mixture of various applications do not change the situation very much, but the ratio of inactive wires is reduced to 13.3% in the case of multiple applications. As we will see later, these wires having mostly DC stress significantly increase aged path delay, and also the aged delay has only weak frequency dependence.

C. Frequency Dependency of Path Delay Degradation

The accuracy of Cond-1 and Cond-2 are examined using various workloads being the result of Cond-3 as the reference, as it is considered the most accurate estimation.

Firstly, differences of path delay degradation between Cond-1 and Cond-3 are compared in Fig. 7 for the fft and multiple applications. The worst path delay error of Cond-1 is found to be $err = -0.81\%$ in cordic, $err = -1.13\%$ in fft and $err = -1.31\%$ in multiple applications, respectively. Here, the worst path delay error, err, is defined as

$$err = (t_{\rm Cond-1} - t_{\rm Cond-3})/t_{\rm Cond-3}, \tag{7}$$

where $t_{\rm Cond-1}$ and $t_{\rm Cond-3}$ are the worst delay of Cond-1 and Cond-3 after degradation, respectively. Similarly, a difference of path delay degradation between Cond-2 and Cond-3 is shown in Fig. 8. The worst path delay error of Cond-2 is found to be $err = -0.35\%$ in cordic, $err = -0.95\%$ in fft and $err = -0.91\%$ in multiple applications, respectively. The error of Cond-2 is smaller than Cond-1 because (5) gives the reasonable estimation of the frequency. The aged worst path delay calculated by Cond-1, Cond-2, and Cond-3 and the errors of Cond-1 and Cond-2 are listed in Table IV with the initial path delay. The frequency dependence of path delay degradation becomes small because, along the worst path after degradation, there are many logic gates having DC stress input.

Next, in Fig. 9, path delay degradation of Cond-1 and Cond-3 is compared, removing the delay increase due to DC stressed transistor. By removing the DC stress, the delay degradation of the paths that were close to the worst delay becomes small. As shown in Fig. 5, the number of DC stress wires becomes smaller in multiple applications, which executes various programs, than running a single application. The situation of running multiple applications is considered more realistic, and in such situations, frequency dependence of path delay degradation became large. However, the contribution of frequency dependence is still small. From Table IV, the worst path delay decreases and the error of the worst path increases in the multiple applications. This result shows that the error of the worst path delay increases as the number of the DC-stressed wires decreases. From the above result, it is shown that the frequency dependency of the path delay

degradation is larger in executing multiple applications than a single application only. In addition, it is suggested that the error of the worst path caused by frequency dependency will decrease by using (5). Some researches [21] proposed path delay mitigation technique by decreasing DC stress paths, and frequency dependency of the worst path will be larger in mitigated circuits.

V. Conclusion

In this paper, the circuit degradation of a processor is quantitatively analyzed by considering stress probability and frequency based on measured data. As a result, it is found that frequency dependency of the worst path delay is not large since there are many DC stress components independent of frequency. However, frequency dependency of path delay increased when DC component decreases due to execution of multiple applications. When we use path delay mitigation technique by decreasing DC stress paths, frequency dependency of the worst path will be larger in mitigated circuits.

Acknowledgments

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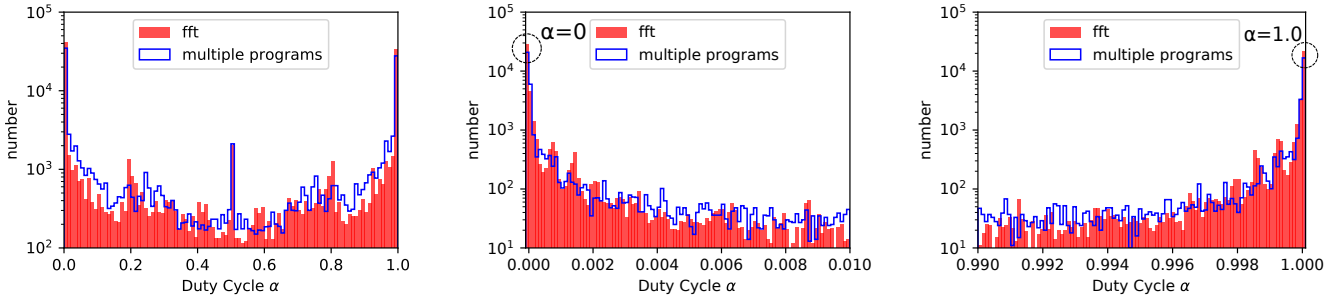
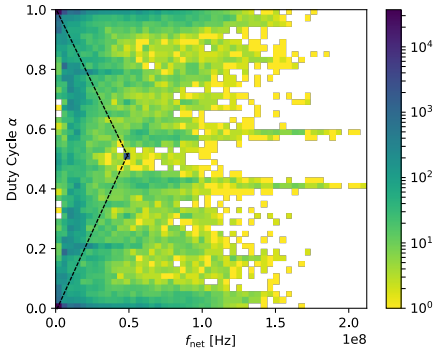
TABLE IV
WORST PATH DELAY, DELAY DEGRADATION, AND DELAY ERROR

Application	Initial (ns)	Cond-1 (ns)		Cond-2 (ns)		Cond-3 (ns)
cordic	4.905	6.078 (Δ1.173)	-0.81%	6.106 (Δ1.202)	-0.35%	6.128 (Δ1.223)
fft	4.905	6.192 (Δ1.287)	-1.13%	6.204 (Δ1.299)	-0.95%	6.263 (Δ1.358)
multiple applications	4.905	6.044 (Δ1.139)	-1.31%	6.069 (Δ1.164)	-0.91%	6.124 (Δ1.219)



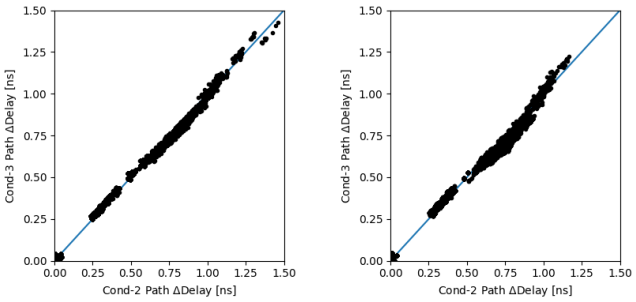
(a) All (b) Duty cycle smaller than 0.01 (c) Duty cycle larger than 0.99

Fig. 5. Path duty cycle histogram in single or multiple applications.



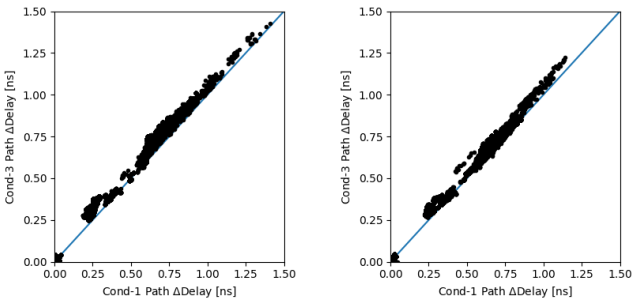
(a) fft

Fig. 6. Distribution of duty cycle and frequency with glitch.



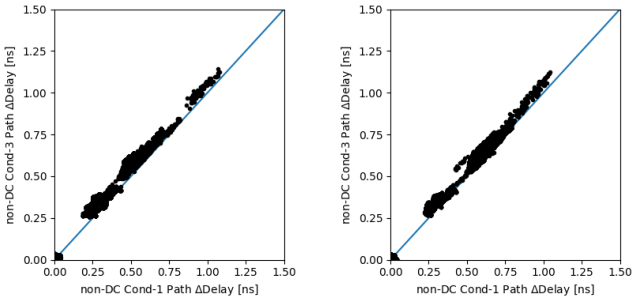
(a) fft (b) multiple applications

Fig. 8. Improvement by considering frequency operating line.



(a) fft (b) multiple applications

Fig. 7. Impact of frequency on path delay degradation.



(a) fft (b) multiple applications

Fig. 9. Path delay degradation without DC degradation.