Verification Methodology to Guarantee Low Routing Resistance to Well Taps

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Abstract

The proposed verification methodology enables designers to meet a maximum resistance specification for the well taps routing. Key strengths of the flow are: automatic identification of both well taps and VDD/VSS grid; comparison of the extracted resistance to a user defined specification value; review of results with a graphical interface; no marker layers to identify the extraction path.

Keywords

Verification, taps, routing, methodology, extraction, CAD, EDA, connectivity

1. Introduction

IC power distribution through metal routing is designed to deliver the required voltages and currents to the transistors to enable the functioning of an integrated circuit. Voltage drop (IR) and electro-migration (EM) are primary design parameters in the design of metal routing from power supplies to the drain/source of active transistors. The IR and the EM rules are well defined in product definition kits (PDK), with verification flows established in the industry [1].

Another type of routing covers the connection of CMOS wells to the power grid: VSS grid to the p-taps of the p-substrate or p-wells, and VDD grid to the n-taps of the n-wells. A PDK usually provides good guidance on how to implement tap layout in the front end of the line (FEOL) active silicon layers, including mandatory metal_1 strapping. However, the metal routing parameters are not well defined for the tap connections to the VDD and the VSS grid, in the back end of the line (BEOL) metal layers. This gap in the verification methodology leaves designers with the freedom to design metal routing with the only requirement that it passes LVS continuity checks. High resistance tap metal routing can weaken Electrostatic Discharge (ESD) immunity and lead to ESD qualification failures [2], as well as functional issues since the output impedance of a MOS transistor is a function of substrate resistance (Rsub). This resistance includes the metal routing to well tap [3].

As the IC industry has followed Moore's Law to advanced technology nodes, there has been a trend of increasing metal layer count coupled with reduced interconnect metal cross-sections. Metal congestion and longer routing paths have made it more difficult to design low routing resistances to the well taps, especially for custom analog, and I/O designs. While experienced designers usually enforce robust tap metal routing as a good design practice, there are no formal methodology or industry standard tools offered in the PDKs.

To resolve those challenges before tape-out, we propose a verification flow that allows the designers to define and check pass/fail criteria for BEOL metal tap routing resistance. This methodology has been successfully implemented for Xilinx 20nm UltraScale™ and 16nm FinFET UltraScale+™ MPSoC products.

2. Motivation Case Study

A. Taps for Internal Nodes to Enhance ESD Protection:

For the ESD discharge path, parameters of BEOL metal tap routing resistance are usually well defined to ensure IR drops < 1V, and to ensure both metal-width and number-of-vias are sufficient in any segment of the path to comply with the ESD current density specification [4].

Occasionally, we have observed failures at internal nodes during ESD qualification with respect to a standard Charge Device Model (CDM) test. The CDM strength of these internal nodes was significantly improved with increased density of p-substrate taps [5]. Design rules were introduced to require specific cells to be surrounded by P+ guard rings as shown in Fig. 1. Design rule checker (DRC) codes were developed to identify all such cells that must be surrounded by P+ tap guard-rings. However, despite the aforementioned cells being completely guard-ringed, it was found experimentally that some 20nm products passed 200V CDM specification, while others, with identical ESD design, failed.

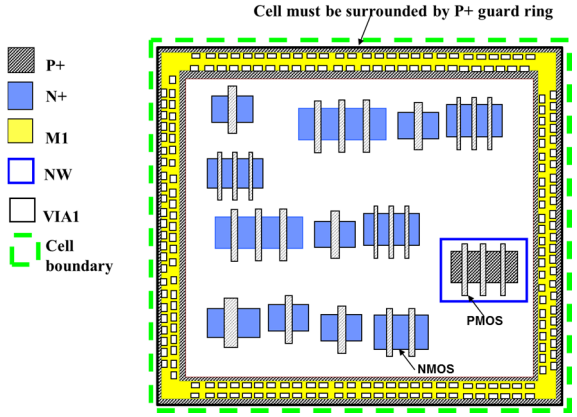

Figure 1: Well tap placement rule requires that the cell must be surrounded by P+ guard ring.

B. CDM Weakness and Routing Resistance of Taps:

For the products that failed a 200V CDM test, failure analysis (FA) showed multiple hot spots at internal nodes (see Fig. 2). Physical FA of these hotspots revealed nmos gate oxide damage exactly at the hot spot locations. With all p-substrate guard rings in place, we made a hypothesis that the observed variation in CDM-ESD immunity may be correlated to the variation in BEOL metal tap routing resistance. No resistance specification was set in the PDK, and the resistance values were not verified prior to completion of the design and product tape-out.

Following observation of the CDM weakness, manual estimation of the BEOL tap routing resistance from the substrate p-taps to the ground grid in the area of the hot spot

was then made; yielding values in the range of 10s of Ωs. Based on this we adopted a mitigation solution to reduce p-tap BEOL metal routing resistance. The target routing resistance was set a priori at R ≤ 5Ω. After making design modifications to meet this new R requirement, the product passed the 200V CDM specification.

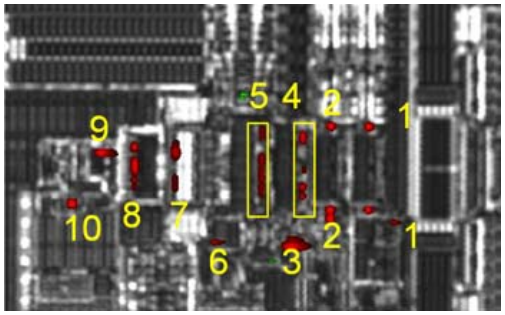

Figure 2: Multiple hot spots related to gate oxide damage observed at the nmos of internal nodes.

This work confirmed the importance of enforcing BEOL metal tap routing resistance to a specific maximum value. For next generation products, it was determined from this that a formal verification methodology should be implemented to enforce this new specification. At that time no industry standard design tool could support the evaluation of routing resistance to the well taps. Hence we have developed a new methodology and verification flow, as described in this paper.

3. Verification Flow

Commercially available EDA extraction tools can extract IR drop for active devices, but do not address the BEOL metal tap routing resistance. Some tools are able to perform point-to-point R extraction, but require manual probing and marking for each point of destination. The user is required to have in-depth knowledge of the VSS and VDD grid which is usually very large and complex. That makes such a largely manual methodology inefficient and prone to human error.

The proposed verification flow [6] was developed to address these shortcomings of commercial EDA tools. Our integrated flow allows the user to verify specific routing resistance specifications ("R-rule") for both P+ tap rings on p-substrate/p-well, or N+ tap rings on N-well.

The flow developed utilizes industry standard tools to perform a series of tasks that starts with 2 inputs: (i) the design layout GDS file and (ii) the design CDL netlist. These two input files are used to verify layout vs. schematic (LVS). A Boolean checker equations are developed and added to the LVS deck to identify tap rings. The identified taps may or may not be continuous (see Fig. 3a, b). For a ring that is formed by fragmented diffusions, the R-rule can be verified for each piece of the diffusion segment (Fig. 3b).

The LVS verification flow enables identification of the VSS or VDD ports and the associated P+ (or N+) taps for follow-up analysis. This flow can identify the VSS or VDD ports at any specified metal layer (e.g. at metal_6 or at metal_10). Each tap ring that is tied to either VSS or VDD ports is identified as a destination point. It is important to note that active devices tied to the VDD or VSS ports are not the focus of this verification. Therefore, these nodes are ignored during this flow. Elimination of the active devices in our flow significantly simplifies the verification task and expedites the verification run-times.

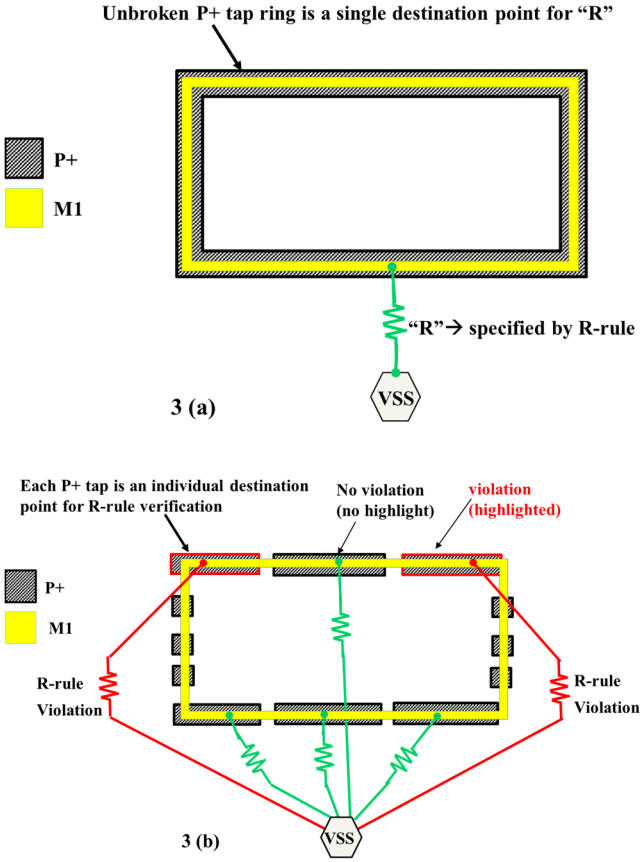

Figure 3: VSS NET to P+ tap ring R extraction for (a) P+ ring with continuous diffusion (b) P+ ring with broken diffusions.

At the next stage, the processed design data is pipelined into a parasitic extraction tool. Then a static resistance analysis (SRA) tool is used to analyze the extracted effective resistance of each VSS or VDD network. Finally, a report is generated as a text file. A flow-chart of our "R" verification process is shown in Figure 4.

For the P+ tap metal routing resistance, the extraction path starts at the VSS port. Each VSS network is extracted with a resistance of the grid to represent the physical network. The tool extracts metal resistance based on the process technology file. The extracted information is represented in the form of a netlist. The SRA collapses the grid into a single resistance to represent the effective "R" of a path from the VSS port to the P+ tap, as shown in Fig. 5. This process is repeated for all VSS ports to all P+ taps for the given design and a report is created.

By default, this report shows all VSS port to P+ tap paths that have resistances more than the specification value. The user has the flexibility to set this specification to any "R" value including zero Ω. A sample report for the VSS net is shown in Fig. 6. The same process is applicable to the N+ tap w.r.t. the VDD net.

Besides generating a complete text report, the verification flow creates a database (.db) file for displaying the violations directly on the layout. Any R-rule violations can be reviewed and debugged through commercially available graphical results viewing tools (see Fig 7).

To capture the total path resistance from VSS or VDD ports to the taps, it is important to complete the final verification at a level where the VSS or VDD routes have reached the C4 bumps or bonding pads. But, at that level, the design database is usually very large. If R-rule violations are identified late in the design flow (when the full IC database is assembled), it can be very difficult and costly in time to fix these, especially since a significant portion of the total metal routing resistance is likely to be coming from the higher resistivity lower metal layers. To address these challenges, the proposed flow allows users to run the verification at the lower metal levels once partial design databases are ready. Users can start their review of the extracted "R" as the layout progresses towards the higher levels of metals. This feature allows IC designers to fix any violations early in the design cycle and before they become very costly or impossible to address.

The entire verification flow is coded into a single script. Users can execute the entire process through a single command line to kick off the "R" analysis on a design block.

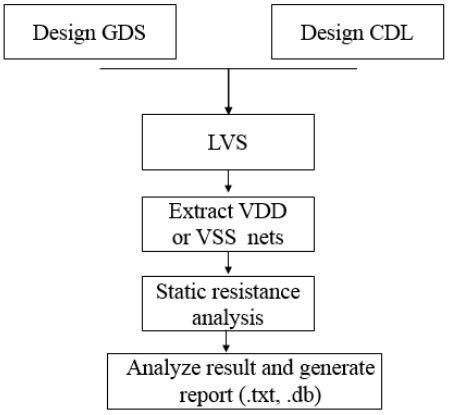

Figure 4: Flow-chart for the verification methodology

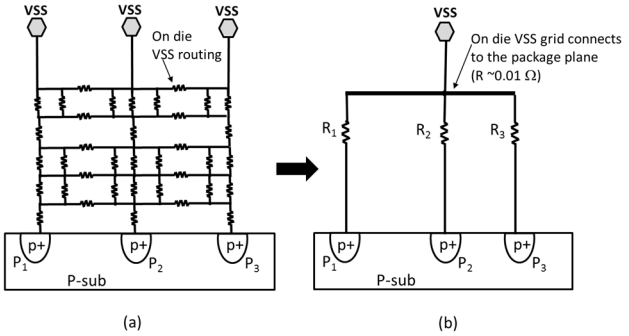

Figure 5: Illustration of the verification flow collapsing through the SRA: (a) ground grid for multiple ground path resistance into (b) a single resistance for each path from ground port to each p+ tap; the resistance at the VSS grid and package plane is negligible and ignored.

```
###One-ohm rule check Result###
#The following paths failed the maximum path resistance of 1 ohms set by user.
gnd(8.493:25.229) TO ld_x0:t1(4.233:0.631) resistance = 4.22 Ohms
gnd(8.493:25.229) TO ld_x1:t1(4.233:5.118) resistance = 4.64 Ohms
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Figure 6: Example violation report generated by the verification flow as a text file

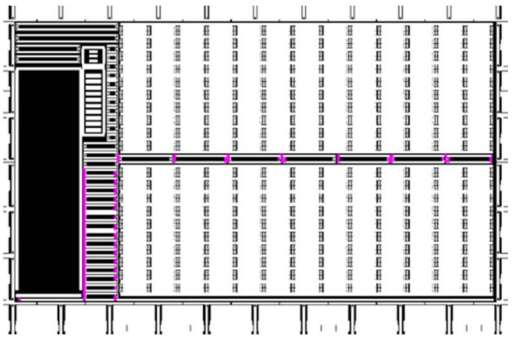

Figure 7: R-rule violations are highlighted on the layout GDS

4. Test Case Verification and Implementation

For an analog design, it is especially important to verify low routing resistance from the tap guard rings to the power grid. A realistic test-case layout scenario that was improved by our flow is illustrated in Fig 8. The VSS grid starts at the metal_6 for this test-case. The extracted resistance for the portion of the layout from the VSS grid to the C4 pad is very small (~0.01Ω), i.e. it meets R-rule by construction of the grid. Hence, this small resistance can be ignored for our verification purpose, i.e., it is safe to assign zero Ω for metal routing from metal_6 to the VSS C4 pad. Applying this simplification significantly shortens the runtime, and saves server memory utilization.

Now focus can be applied to resistance extraction for metal layers below the metal_6 grid. In this test case, the user defined pass/fail specification was set to 1 Ω. The flow identified and highlighted the exact location on the P+ tap routing that violated this specification. The flagged high resistive paths were then modified by adding metal and vias. Layout snapshots for the failed and passed designs for this test case are shown in Fig 9.

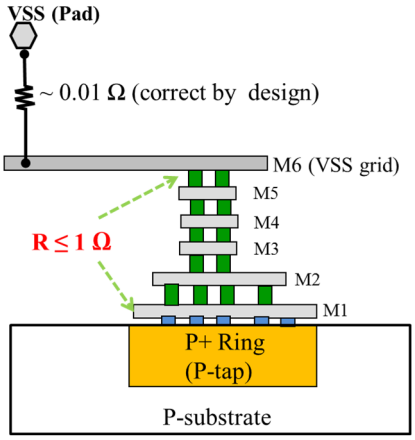

Figure 8: Allowed metal routing resistance for P+ ring to the metal_6 (M6) VSS grid (maximum): 1 Ω

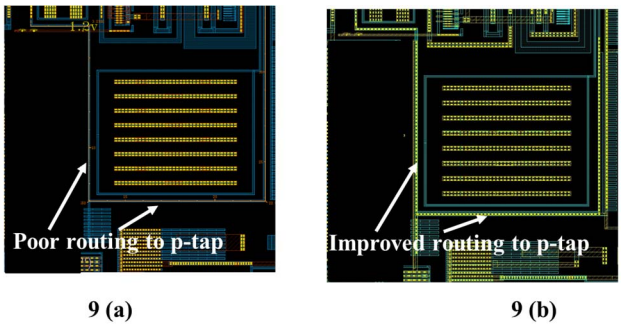

Figure 9: Layout snapshots for the failed and passed designs for test case (a) R-rule failed (b) R-rule passed

5. Discussion

Commercial EDA tools extract resistance by processing the entire design. It is inefficient to analyze raw data from a large design before re-processing the extracted data. Scripts may be used to filter the pre- and post- extracted data for further analysis. Our flow requires no script for pre- or post-processing of design data.

Another advantage is this flow does not require special marker layers to identify a net and a destination terminal. The flow relies on existing text terminal labels and net identifications. Interconnect connectivity is established through via and metal overlap, which is part of the standard design process.

We optimized two main areas of an existing extraction as follows:

(1) *Connectivity extraction* utilizes net dependent filtering. Any node that is not associated with the specified net is excluded during this process. An extracted path for the VSS terminal to a p+ tap is illustrated in Figure 10. Devices that are not part of path of interest are ignored.

(2) *Resistance extraction* is initiated only for the targeted networks. The terminal and net information allows any net that is violating the "R-rule" to be reported. Our analysis algorithm is designed to limit the search for path $R > R_{(max)}$ only.

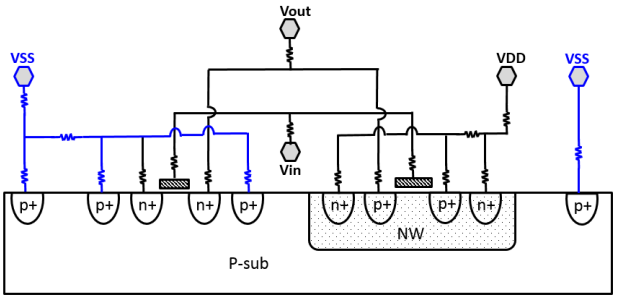

Figure 10: Connectivity extraction for the VSS net to the p+ well tap; the target path for extraction is highlighted in blue. Similar path selection is possible for the VDD net, or any other net of interest.

A dominant factor in the runtime of the extraction is the area of the search region [7]. Removal of devices and nets not related to well taps reduces the search. That cuts the size of the extracted data (.spf) file, and shortens the runtime.

The final report is reviewed through a standard graphical interface tool. This provides an interactive feedback for the users to review routing resistance. The tool highlights the "region of interest" that requires routing fix.

Our tool uses an industry standard extraction engine, which is already part of the product verification flow, thereby eliminating the need to acquire additional EDA tools. Our flow is seamlessly retrofitted with vendor tools without impacting other verification and sign-off processes.

This methodology can be utilized for different verification purposes beyond the scope of this work. For example, verification of the R and C of interconnect routing for single net, multi nets, point-to-point, and multipoint routing can utilize this methodology. A comparison of our methodology with a vendor tool is shown in the Table 1.

Table 1: Advantages of using our verification flow vs. a vendor tool.

Feature	**This Solution**	**Vendor Solution**
Ease of use	* Easy to learn * No extra training	* Tool dependent * Tool training
Integration	* Seamless with existing flow	* Tool specific
Run Time	* Minutes	* Hours
Extracted file size	* Small	* Large (~100X)
Visualization	* Violation specific * Localized	* Not violation specific * Non localized
Violation fix	* Real-time feedback	* Post processing of data needed

The "R" reported by this methodology is the total contribution from all the BEOL layers associated with a specific net and the destination terminal. Ability to review and analyze resistance of each contributing BEOL layer would further improve our flow and allow designers to do fix with lesser iterations.

In summary, our verification flow offers the following advantages:

1. Flow utilizes existing identifiers to find nets and destination terminals.
2. Accuracy is guaranteed since the flow uses an industry standard extraction engine.
3. Data reduction allows for a verification that is faster and easier to analyze.
4. Integration is seamless with existing verification flows.

6. Conclusion

The proposed verification methodology enables designers to meet resistance specification for the well taps routing. Test cases and extraction flow are discussed to demonstrate its efficiency. We believe that other application specific extractions can be developed based on the proposed approach.

7. References

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