Back-Bias Generator for Post-Fabrication Threshold Voltage Tuning Applications in 22nm FD-SOI Process

Arif Siddiqi, Navneet Jain, Mahbub Rashed
Design & Technology Co-Optimization (DTCO)
GLOBALFOUNDRIES INC.
Santa Clara, CA, 95054, USA
arif.siddiqi@globalfoundries.com

Abstract

This paper provides design and implementation of silicon-validated Back-Bias Generator (BBGEN) for Forward Back-Bias (FBB) operation of transistor devices in 22FDX Fully Depleted Silicon-On-Insulator (FD-SOI) process. The design has been used to drive multiple Ring Oscillators (RO) and silicon measurement shows signficant enhancement in maximum frequency (fmax) with the application of FBB. BBGEN consists of two independently controlled back-bias sections to provide FBB to both NMOS and PMOS devices. This architecture has also been implemented for device trimming applications to enhance the performance of slow devices towards typical performance by the application of Threshold Voltage (VT) tuning using FBB.

Keywords

CMOS, FD-SOI, FDX, forward back-bias, back-bias generator, device trimming, rail-to-rail unity gain buffer, DAC

1. Introduction

FD-SOI technology has been used for sometimes as an alternative to bulk planar technologies and reported to have several benefits in terms of Power, Performance and Area (PPA). Figure 1 shows the comparison of 22FDX technology with and without FBB with FinFET and Bulk Planar technologies. One of the main features of FD-SOI technology is the availability of substrate node that is accessible externally and can be used to tune device characteristics substantially such as threshold voltage (VT) after fabrication [1,2]. Regular bulk technologies may also potentially employ Deep NWELL (DNW) layer to achieve some variability but the amount of VT tuning as a design feature is very limited due to the possibility of reverse-biased parasitic substrate diodes getting forward-biased once the voltage difference goes above VT of substrate diode. For 22nm FD-SOI technology, the Buried Oxide (BOX) layer isolates the local substrate from other three nodes (drain, source and gate) and therefore can be tuned up to the device breakdown level without having any substrate diodes becoming forward-biased (Figure 2). This can potentially provide an extremely useful external tuning knob and opens up a whole new set of interesting circuit design techniques that may not be possible in regular bulk planar or FinFET technologies. This feature has many advantages that can be implemented globally on System-on-Chip (SOC) level or at a specific area; for example in case of device trimming, the back-bias enhancement can be used globally to force the devices fabricated in slow process case to typical case by tuning VT

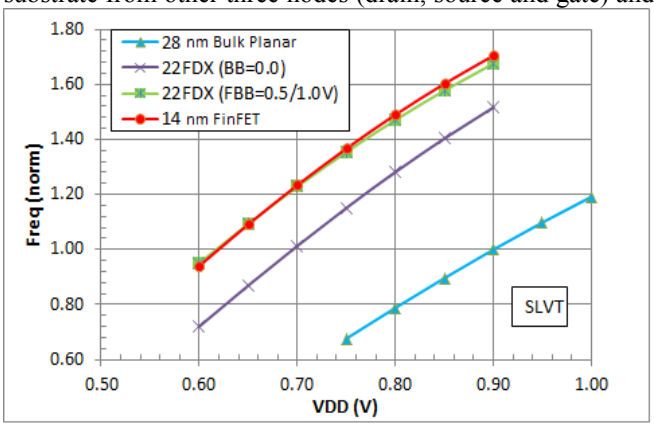

Figure 1: 22FDX Comparison with and without FBB

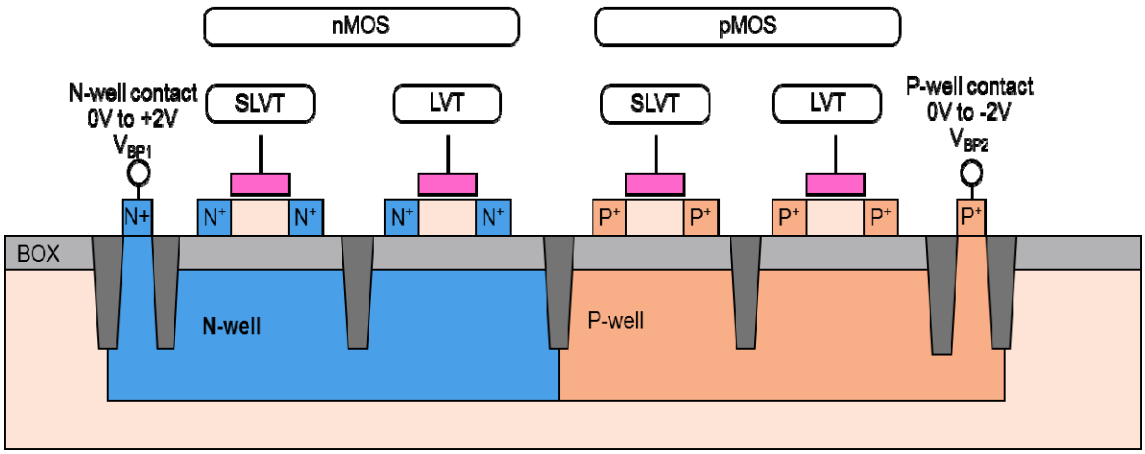

Figure 2: 22FDX Flipped-Well FET Cross-Section

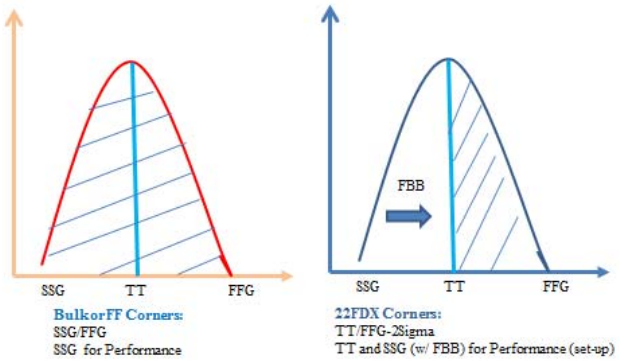

Figure 3: Device Trimming using FBB

of devices to bring it closer to the expected typical process VT. This may result in better trade-offs among PPA by not necessarily overdesigning the blocks as has been generally done to satisfy slow process corner case (Figure 3) In another application, this feature can also be used to reduce the overall power consumption by reducing leakage during inactive or power-down mode. It can also be used to enhance the performance of critical path devices selectively during high performance and speed sensitive applications.

This paper presents the design and implementation of Back-Bias Generator (BBGEN) that generates back-bias voltages for VT tuning applications. It consists of two independently controlled back-bias sections to provide both positive and negative back-bias operations for NMOS and PMOS devices respectively. Both sections carry 3-bit Digital-to-Analog Converter (DAC) followed by unity-gain buffers to drive capacitive load. Both DACs provide 7 linear settings for back-bias operation. Negative BBGEN (N-BBGEN) carry a 4-stage Negative Charge Pump (N-CP) to generate negative voltage that is used as a negative low supply level to drive negative level-shifters (NLS), Negative DAC (NDAC) and unity-gain rail-to-rail buffer. The implementation can be used to drive up to 20nF of estimated substrate/well capacitive load with up to 30uA of well leakage. BBGEN is used to drive three 41-stage Ring Oscillators (RO) and silicon-based measurements show RO frequency increasing linearly for each DAC update and overall 35% fmax improvement for up to 1.8V (-1.8V) of applied FBB voltage.

In Section 2, proposed architecture is explained, implementation details are provided in Section 3and silicon measurement results are shown in Section 4 while Section 5 provides conclusion.

2. Proposed Architecture

Figure 4 shows the top-level block diagram of the BBGEN architecture. BBGEN requires two supply voltages 0.8V core voltage supply and 1.8V I/O supply. The internal control logic and 100MHz CP Clock (CLK) signals are derived from 0.8V supply and level-shifted to either 0 – 1.8V or 0 – (-1.8V) voltage swing levels for internal operation. The current drawn by 0.8V supply is less than 1% of the total current consumption and most of the current is drawn from 1.8V supply. As mentioned earlier, BBGEN consists of two sections, P-BBGEN and N-BBGEN. P-BBGEN generates NMOS back-bias voltage by taking 1.8V I/O voltage supply and 3-bit PDAC provides 7 linear steps; ~257mV per PDAC update and rail-to-rail unity gain buffer drives back-bias voltage of NMOS N-Well (NW) bias grid.

N-BBGEN comprises of similar front-end architecture but running in 0 to (-1.8V) supply voltage domain requiring

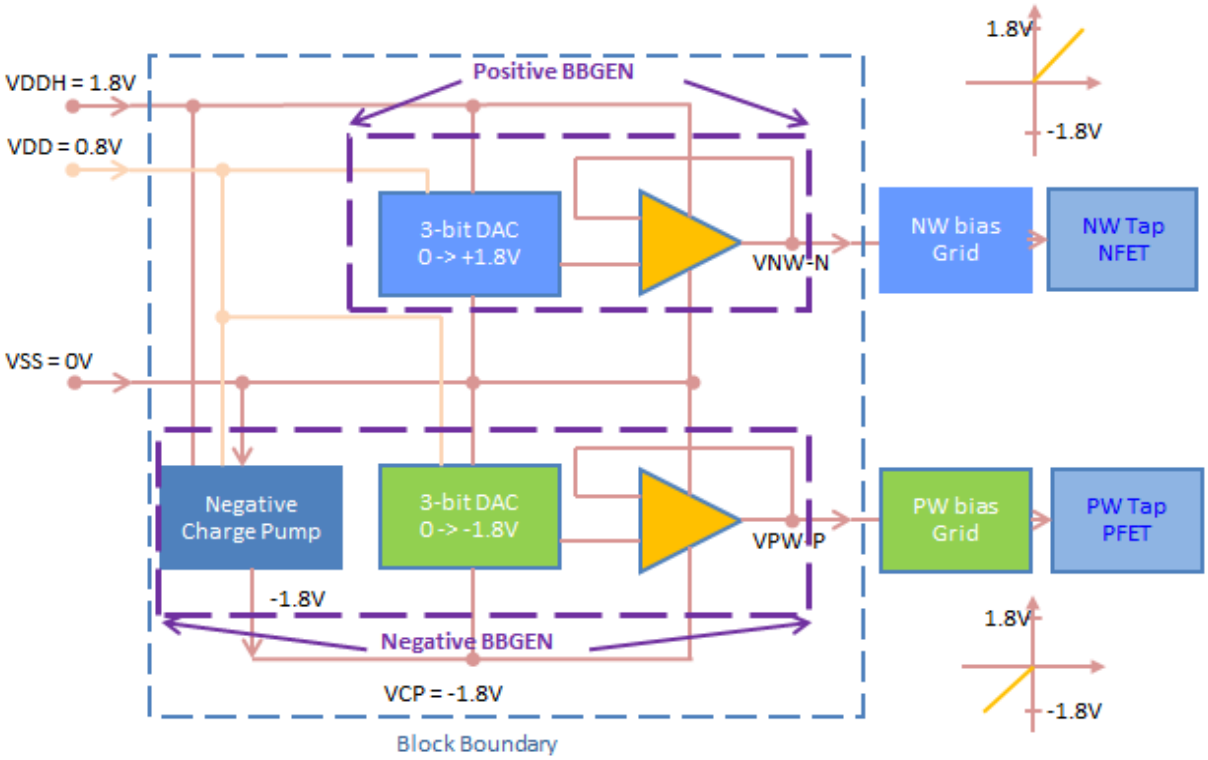

Figure 4: BBGEN Top-Level Block Diagram

Negative Level Shifters (NLS) and Negative Charge Pump (N-CP) that generates -1.8V as the low supply level. It also generates the internal current drive for 3-bit NDAC and unity-gain buffer providing 7 linear steps; -257mV per each NDAC update driving negative back-bias voltage VPW-P of PMOS P-Well (PW) bias grid.

This architecture uses open-loop concept and doesn't need any feedback loop to regulate the output voltage. The output back-bias voltages VNW-N and VPW-P may vary around 10% over the whole DAC range but the impact is minimum as the 10% change in 1.8V supply voltage translates into less than 15mV overall VT variations i.e. even a relatively smaller Power Supply Rejection Ratio (PSRR) value due to resistor-string ladder based DAC architecture doesn't have significant impact on the overall VT tuning control. Another advantage of this architecture is that the actual output driver is unity gain buffer, designed to drive up to 20nF of well capacitive load (estimated 10-15 Million Logic Gates); not the CP output which generally is very sensitive to output load (both capacitive and current based load). Therefore, the impact of capacitive load variation, that can vary from tens of pF to up to 20nF, on the CP output is negligible. Also because of this design feature, the output capacitive load can be highly scalable and doesn't require a scaled BBGEN design for different capacitive load applications.

One more advantage of this architecture is that the output unity gain buffer acts as a low pass filter with less than 250 kHz corner bandwidth, resulting in the high frequency supply noise and 100 MHz CP clock feedthrough filtered out, providing a less than 1mV peak-to-peak voltage ripple on VPW-P back-bias output, without requiring an elaborate low-pass filtration process to limit the output voltage ripple.

3. Design Implementation

This section provides detailed design information and measurement results. As shown in Figure 4, BBGEN consists of two parts, P-BBGEN and N-BBGEN. Many of the blocks are common in both sections such as unity-gain buffer, 3- bit DAC, positive and negative level-shifters. The only additional block in N-BBGEN is the Negative CP that generates -1.8V. Following sub-sections provide design implementation of the major blocks

3.1. Negative Charge Pump (N-CP)

Charge Pump is an essentially a DC-DC converter that converts the input DC voltage to a DC voltage that can be multiple times higher than the input. It can also be used to generate negative DC voltage which is not readily available. CP usually consists of multiple stages depending on the required output DC voltage and amount of load needed to drive. Each CP stage consists of pumping capacitor and switches to charge and discharge the cap based on the input periodic signal (mostly clock). The most famous and the simplest form of CP circuit is based on Dickson architecture [3] (Figure 5) that replaces switches with forward biased diodes with alternate non overlapping clock edges driving the consecutive CP stages. A modified Dickson CP version replaces actual diodes with MOS diodes [4,5]. This topology has one major drawback; threshold voltage VT of the diode causes the reduction of CP output voltage by a factor of (N+1)*VT where N is the number of stages. This design can easily be modified to generate negative voltage by rearranging diodes and clock signals; however the voltage gain and the current driving capacity through each stage is limited requiring the use of bigger on-chip capacitors which may not be possible in most cases.

Another interesting topology that has been used to generate high positive voltage is called Latched CP or Voltage Doubler architecture. It is usually designed using standard bulk planar CMOS technologies and quite suitable for high frequency operation, requiring only 2 non-overlapping clock phases [4,6]. Another advantage of this topology is that it is highly symmetrical and can also be used to generate negative voltage just by connecting input node of the first stage to VSS instead of VDD. In addition, to get the same voltage gain as in double CP configuration, each capacitor needs to be only one half the size if designed in a single CP style [4]. In this implementation, a modified version of Latched CP architecture is used to generate negative -1.8V with 100MHz input clock. Figure 6 shows one of the four identical stages, known as Charge Transfer Block (CTB). As this design is implemented in FD-SOI technology where local substrate node is isolated because of the BOX layer, the body-effect is not a concern and local substrate nodes for both PMOS and NMOS devices can be connected to their default VSS connection without incurring any loss in efficiency as opposed to connecting to transistor source which may be required if implemented in regular bulk planar CMOS technology to achieve better efficiency [6]. Alternate Polarity Metal-Oxide-Metal (APMOM) capacitors are used in place of more area efficient NMOS caps (NCAP) which not only provide capacitance independent of input voltage variations but also don't contain reversed-biased substrate parasitic diodes that may become forward-biased once the voltage on the bottom plate goes more negative than the VT of the NCAP causing a latch-up scenario. Both NMOS and PMOS devices are sized as a trade-off between required RC time-constant and the voltage gain through each stage. This design requires four CTB stages to provide enough driving current for internal NDAC and unity-gain buffer (almost 100uA typical) while keeping CP voltage at -1.8V. The charge pump (N-CP) can

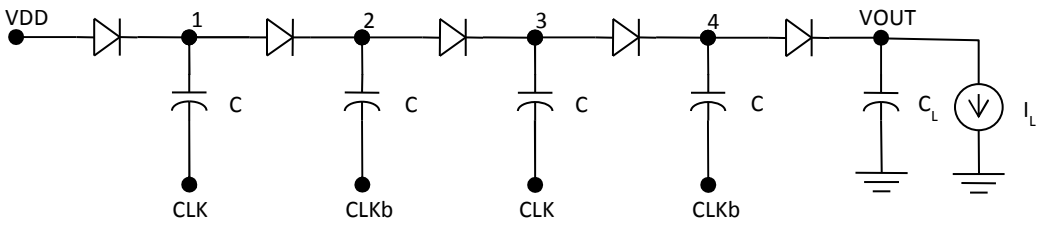

Figure 5: Conventional Dickson CP

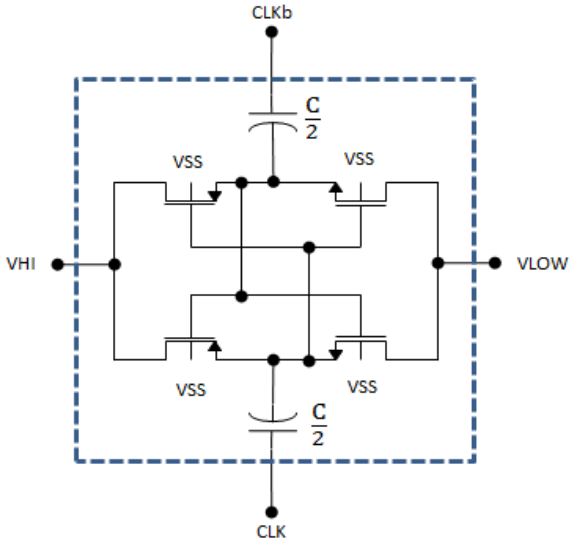

Figure 6: N-CP Charge Transfer Block (CTB)

drive up to 20nF of capacitive load from PW Bias Grid, which can also include up to 30uA of additional well leakage current.

3.2. DAC and Unity Gain Buffer

As mentioned earlier, BBGEN consists of two sections, P-BBGEN and N-BBGEN both carrying identical 3-bit DAC and unity-gain buffer to drive the output. DAC is designed using resistor-string ladder network with transmission gate switches providing guaranteed monotonicity and linear operation. This feature is very useful when BBGEN is used to drive the block whose back-bias voltage is dynamically updated based on the performance or process monitoring feedback loop to achieve certain performance level.

Unity gain buffer is designed using Operational Transconductance Amplifier (OTA) with complementary folded cascode input stage driven by class AB output stage. That way the designed unity-gain buffer can work for both input and output rail-to-rail signals over Process, Voltage and Temperature (PVT) variations. The unity-gain frequency of OTA is designed to be around 10 MHz with on-chip compensation APMOM capacitor so that the high frequency noise emanating from 100MHz clock feedthrough and power supply noise can be filtered out. This results in output voltage ripple on the back-bias output voltage to be less than 1mV peak-to-peak.

4. Silicon Measurement Results

In order to validate the performance and FBB functionality, three 41 stage ROs are designed whose back-bias nodes VPW-P and VNW-N are driven by the back-bias voltages generated by BBGEN. Each RO consists of delay cells based on Inverter, NAND and NOR gates respectively. A 1024 frequency divider is used at the RO outputs to facilitate silicon measurements. The BBGEN is used to provide Forward Back-Bias (FBB) to RO delay cell's transistors PMOS and NMOS back-bias nodes i.e. for PMOS, back-bias VPW-P is varied from 0V to -1.8V when the NDAC code is swept from 0 to 7 resulting in PMOS transistors VT to reduce incrementally, subsequently speeding up the RO output frequency. Similarly for NMOS devices, back-bias VNW-N is varied from 0V to 1.8V by sweeping PDAC code from 0 to 7 resulting in VT of NMOS devices to become increasingly smaller and eventually speeding up the RO frequency. Figures 7-8 show the silicon measurement results of BBGEN back-bias outputs VNW-N and VPW-P when 3-bit DAC code is swept from 0 to 7 under typical voltage and temperature conditions. The non-monotonicity in VPW-P back-bias voltage and then eventually in RO Frequency response from DAC code 6 to 7 is due to the unexpected excess current drawn from charge pump by an internal current bleeder circuit causing the N-CP output voltage to drop. This issue has been resolved in the updated design and a more monotonic response for the future versions is expected. Figure 9 shows the measurement results of total BBGEN internal current IDDH variations for the same conditions. Figures 10-12 show the normalized measured frequency plots of three ROs when 3-bit DAC is swept from 0 to 7. The silicon measurement shows the BBGEN performing well by linearly increasing the RO frequency over the DAC range. Figure 13 shows the top-level layout snapshot of BBGEN and three ROs, including 25 pin wafer probe pads used for silicon measurements. Figure 14 & 15 show the Die Micro-Photographs. Table 1 provides the typical specs and features of BBGEN while Table 2 shows the comparison of designed N-CP with the reference designs reported in recent literature.

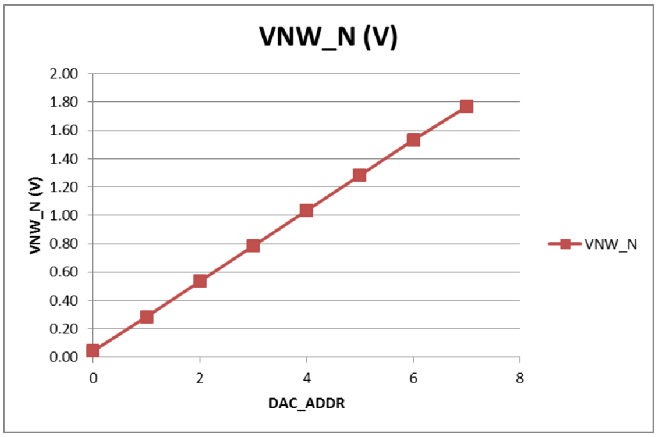

Figure 7: VNW-N Output for NMOS Back-Bias Grid

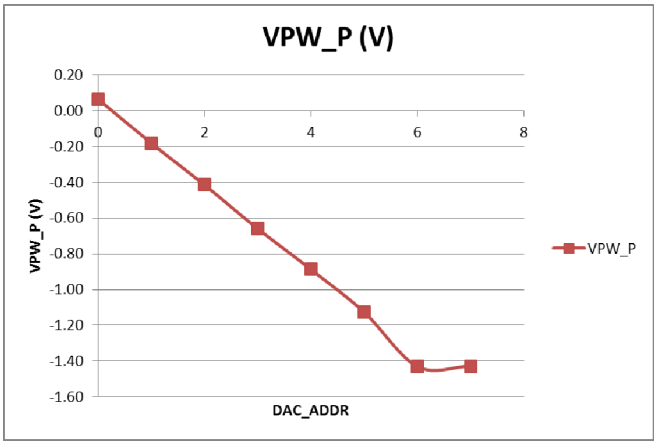

Figure 8: VPW-P Output for PMOS Back-Bias Grid

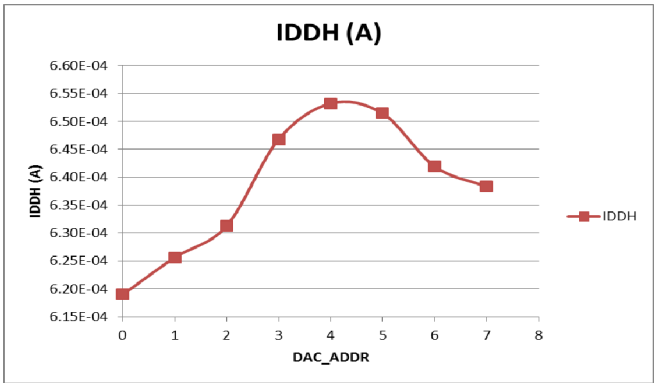

Figure 9: BBGEN Current Consumption (A)

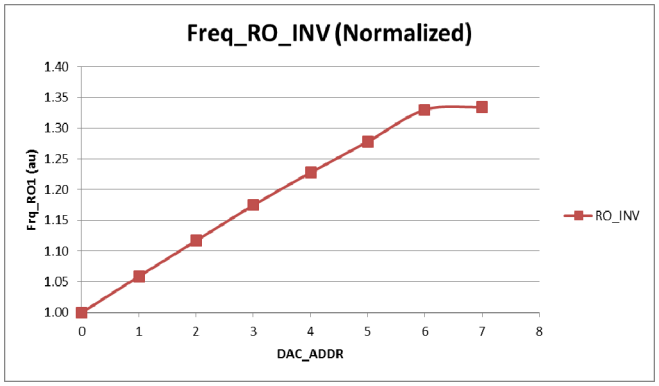

Figure 10: INV based RO Frequency Sweep for FBB changing from 0 to 1.8V (-1.8V)

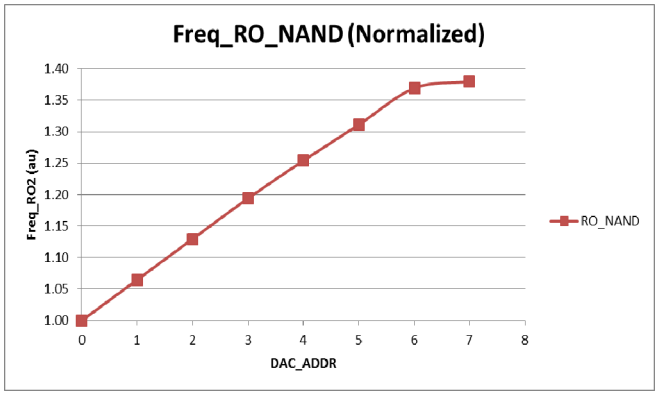

Figure 11: NAND based RO Frequency Sweep for FBB changing from 0 to 1.8V (-1.8V)

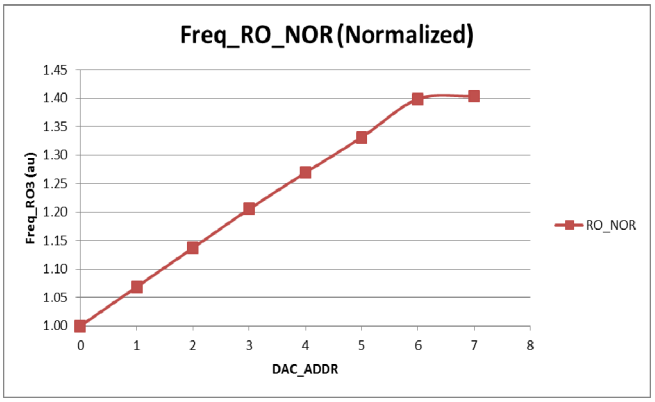

Figure 12: NOR based RO Frequency Sweep for FBB changing from 0 to 1.8V (-1.8V)

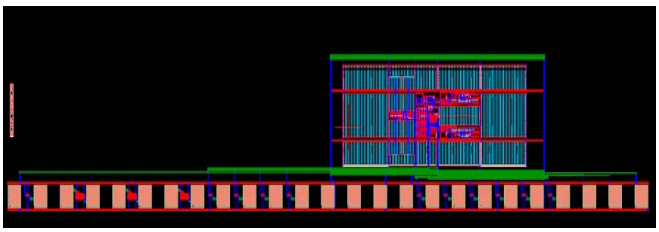

Figure 13: BBGEN and RO Top-Level Layout (Including 25 pin wafer probe pads)

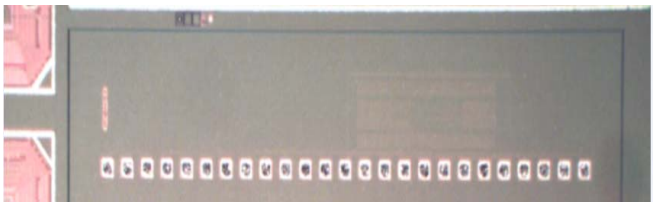

Figure 14: BBGEN and RO Die Micro-Photograph (Including 25 pin wafer probe pads)

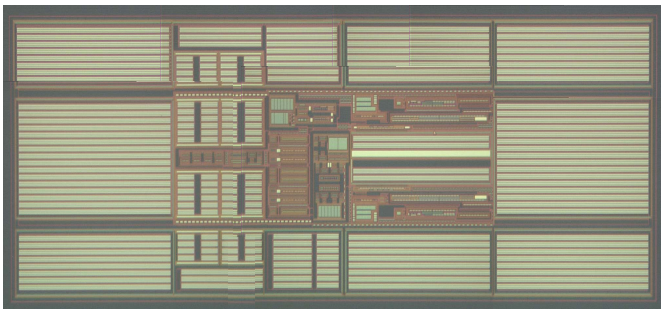

Figure 15: BBGEN Die Micro-Photograph

Table 1: BBGEN Typical Specs and Features

Parameters	**Features**
Block Layout Area	507.2 x 163.5um^2 (0.083mm^2) (Including internal 100pF decap) 256 x 121um^2 (0.031mm^2) (Core area excluding internal decap)
Metal Layers	4 Layers (M1, M2, C1, C2)
3-bit DAC	INL < 0.2LSB, DNL < 0.2LSB
Max Load	Capacitance= 20nF (supports up to 10-15 M Logic gates based on maximum well leakage of 30uA)
Initial Startup time	~30us (for full level negative charge pump output)
Settling Time	~10us/dac update at 1nF load
Output Voltage Ripple	< 1mV (with 100pF Internal decap)
Input CLK Frequency	100MHz
Average Active Current	Ivddh = 634uA, Ivdd = 3.31uA @ 25C, vdd=800mV, vddh = 1.8V
Power Down Leakage Current	Ivddh_lkg = 1.23nA, Ivdd_lkg = 87.8nA @ 25C, vdd = 800mV, vddh = 1.8V
Supply Voltage	800mV, 1.8V

Table 2: BBGEN Charge Pump Comparison with References

Charge Pump Parameter	This work	Ref [7]	Ref[6]	Ref[8]
CP Area (um^2)	5,041	NA	NA	30K
Metal Layers	4	NA	6	3
CP Stages	4	7	5	5
Process	22nm FD-SOI	0.15um CMOS	0.18um CMOS	0.8um 5V/HV CMOS/ DMOS
CP Output Voltage (V)	-1.8	-6.0	5.0	20
CP Type	Latch based	Dickson	Latch based	Latch based
Number of Clock Phases	2	4	2	2
Max Current Load (uA)	100	NA	400	25
Max Cap Load (nF)	20	0.3	0.03	0.028
Cap/Stage (pF)	2	6.6	5	NA
Initial Startup time (us)	30	40	0.5	250
Output Voltage Ripple (mV)	< 1	>100	400	400
Input CLK Frequency (MHz)	100	8	100	10
Current Consumption (uA)	655	NA	NA	NA
Supply Voltage (V)	1.8	1.5	1.8	5

5. Conclusion

In this work, a BBGEN architecture has been presented that is used to drive back-bias nodes of SOC as a whole or specific blocks inside SOC for performance enhancement and device trimming applications in 22nm FD-SOI technology. Silicon measurement results show 33-40% RO fmax improvement with the application of 1.8V (-1.8V) Forward Back-Bias. Comparison with the recent literature shows significant advantages with this implementation and showing less than 1mV output voltage ripple with 10pF capacitive test load and 100uA internal current load. Also capacitor per charge pump stage is less than half while the current load is comparable and specified maximum capacitve load is order of magnitude bigger than the comparison. Another main advantage of this implementation is that the capacitive load is highly scalable from a few pF to up to 20nF without requiring any change in the design.

6. Acknowledgements

We like to acknowledge Global Foundries management for supporting this project. We like to thank Shibly Ahmed for providing us with PPA comparison plots between different nodes. We also wish to thank Helmut Prengel for measurement support, Peter Vinh and Siang Fatt for layout work. We would also like to particularly thanks Juhan Kim for his technology insights and spending valuable time in long technical discussions to have the best in class physical design methodology.

7. References

[1] Cathelin, A. “RF/analog and mixed-signal design techniques in FD-SOI technology”, 2017 IEEE Custom Integrated Circuits Conference (CICC), pp.1 – 53

[2] H.-K. Lim and J. G. Fossum, “Threshold voltage of thin-film Silicon-on-Insulator (SOI) MOSFET’s,” IEEE Transactions on Electron Devices, vol. 30, no. 10, pp. 1244-1251, 1983

[3] J. Dickson, “On-chip high-voltage generation MNOS integrated circuits using an improved voltage multiplier technique,” IEEE J. Solid-State Circuits, vol. SC-11, no. 3, pp. 374–378, June 1976

[4] G. Palumbo, D. Pappalardo, “Charge Pump Circuits: An Overview on Design Strategies and Topologies”, IEEE Circuits and Systems Magazine, First Quarter 2010, pp. 31-45

[5] J. Witters, G. Groeseneken, and H. Maes, “Analysis and modeling of on-chip high-voltage generator circuits for use in EEPROM circuits,” IEEE J. Solid-State Circuits, vol. 24, no. 5, pp. 1372–1380, Oct. 1989.

[6] R. Pelliconi. D. Ieui. A. Baroni, M. Pasotti. P. Rolandi. "Power efficient Charge Pump in Deep Submicron Standard CMOS Technology’, IEEE J. Solid-State Circuits, vol. 38, no. 6, pp. 1068–1071, June. 2003.

[7] T. Yamazoe. H. Ishida. Y. Nihongi, , "A Charge Pump that Generates Positive and Negative High Voltages with Low Power-supply Voltage and Low Power Consumption for Non-Volatile Memories’, 2009 IEEE International Symposium on Circuits and Systems, Year 2009, pp. 988–991.

[8] J. Richard, Y. Savaria, "High Voltage Charge Pump Using Standard CMOS Technology’, The 2nd IEEE Northeast Workshop on Circuits and Systems, NEWCAS 2004, pp. 317–320.