An Automated Design Flow for Synthesis of Optimal Multi-layer Multi-shape PCB Coils for Inductive Sensing Applications

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Abstract

This paper presents an automated flow to quickly design and layout an optimal multi-layer square, hexagonal, octagonal spiral printed circuit board (PCB) coils for inductive sensing applications. The flow takes into account several constraints including via connections in the center of the coil well ahead in the calculations for minimum inner diameter in order avoid any iteration later. Step-by-step instructions on how to find the optimal solution for a given optimization criteria e.g. coil area, coil performance parameter, application performance parameters are presented including trade-off between area vs layers and area vs coil fill ratio. Next, the paper discusses the algorithm to generate the multi-layer multi-shape coil in order to layout the coil on a PCB using computer aided design tools. An online design tool is developed based on flow proposed in this paper for inductive sensing applications and results from the tool are discussed and generated PCB coil layout to five popular PCB CAD tools is presented. The online design tool has reduced the PCB coil design time to a fraction of a minute and is being actively used by hundreds of designers worldwide.

Keywords

Liner Inductive Sensing, Coil, PCB, EDA, online design tool, optimization

1. Introduction

Inductors form integral part of circuit design in system level applications. In most cases printed trace inductors (on board) are preferred to discrete solenoidal inductor components. It becomes very critical to design coils on printed circuit board (PCB) that meet the desired system specifications, within the limitations of available space on board, and at the same time complying with the PCB manufacturing constraints. Designing a PCB coil manually by taking in to account above consideration and optimizing it for given number of PCB layers and/or various shapes like circular, square etc. is a non-trivial task. Zeroing down on an optimal solution for a given system level application requires significant amount of engineering expertise as well as multiple iterations and therefore is very time consuming.
PCB layout engineer not only need to know the accurate relationship of physical dimensions of coil to coil performance parameters, starting from calculations of diameters and trace widths to the self and mutual inductances but also need to know about hidden parasitics. Although a set of equations to calculate the inductance from coil geometry have been established, applying these to the problem at hand requires significant analysis. These equations do not directly include the geometries of the PCB coil in to consideration such as layer stack information. A detailed analysis of various geometrical parameters to performance parameters is required in order to design an optimal multi-layer multi shape PCB coil. In general multiple iterations are required to arrive at optimal solution. This is mainly because a well-defined tool, flow or methodology for designing multi-layer multi-shape PCB coils does not exist for system level applications.

PCB coil design methodologies reported in literature make use of simulated data to study the variation of inductance of the coil with physical parameters of the coil [1]. These methodologies require the simulations to be run every time the setup is changed, and several iterations for a given application. This is time consuming and error prone. Accurate expressions for planer spiral coils are discussed in [2-7]. These need to be extended to include stack layer details for multi-layer coils.

In this paper, an automated flow to efficiently design optimal multi-layer multi-shape PCB coils for system level applications is presented. The flow dynamically derives the relation between output parameters e.g. inductance and the input parameters e.g. coil geometry for given system level specification using well established mathematical model of PCB coil. Representing these relations graphically to PCB designer reduces number of iterations in arriving at correct input parameters for required output parameters and therefore enables much faster coil design as compared to conventional methods. Multiple solutions for the same design specification can now easily be found by varying different input parameters for required output parameters using trade-off plots.

The flow also takes in to account constraints like via connections in the center of the coil well ahead in the calculations for minimum inner diameter in order avoid any iteration later. Step-by-step instructions on how to find optimal solution for a given optimization criteria e.g. coil area, coil performance parameter, application performance parameters is presented including trade-off between area vs layers and area vs coil fill ratio. Next the paper discusses the algorithm to generate the coil in order to lay-out the coil on the PCB as well as a pseudo code to generate layout in PCB computer aided design tools. Inductive sensing application [8-9] is chosen to demonstrate the flow proposed in this paper. The PCB coil designer results from the tool are discussed and generated PCB coil layout to five popular PCB CAD tools is presented. The remainder of the paper is organized as follows. Section 2 describes the equations to design multilayer PCB coils. Section 3 presents an automated flow followed by discussion on optimization flow

in section 4. Section 5 explains the PCB layout generation. Results are discussed in section 6 and section 7 concludes the paper.

2. Multilayer Spiral PCB Coil Design

The inductance for a single layer planer spiral inductor is given by Mohan's equation [4]

$$L = [(\mu_0 N^2 D_{AVG} C_1)/2][\ln(C_2/\rho) + C_3\rho + C_4\rho^2] \quad (1)$$

where,

L is the total inductance

μ_0 is the permeability of free space, $4\pi \times 10^{-7}$

N is the number of turns of the coil

D_{avg} is the average diameter = $(D_{out} + D_{in})/2$

C_1, C_2, C_3, C_4 are layout dependent factors based on the geometry of the coil (for a circle, the following values are appropriate: C_1=1.0, C_2=2.46, C_3=0, C_4=0.2. The C coefficients for other shapes may be found in [4])

ρ is $(D_{out} - D_{in})/(D_{out} + D_{in})$, and represents the fill ratio of the inductor – small values of ρ correspond to hollow inductors ($D_{out} \approx D_{in}$), while large values correspond to ($D_{out} >> D_{in}$). Different coil shapes are shown in Figure 1 and coil parameters are listed in Table 1.

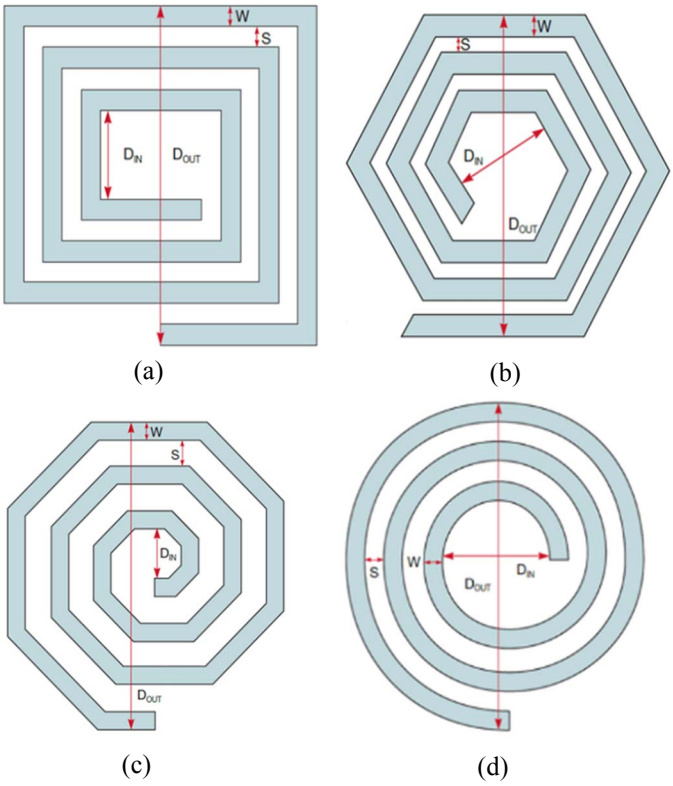

Figure 1: PCB coils (a) square, (b) hexagonal, (c) octagonal, and (d) circular.

The inductance of a two-layer coil (assuming current flow direction adds flux) is given by,

$$L_{TOT} = L_1 + L_2 + 2 * K_c * \sqrt{L_1 * L_2} \quad (2)$$

where K_c is coupling coefficient and given by [2]

$$K_C = \frac{1.5625N^2}{(0.184x^3 - 0.525x^2 + 1.038x + 1.001)(1.67N^2 - 5.84N + 65)} \quad (3)$$

where x is distance in millimeters between the inductors on two PCB layers. With multi-layer coils, there are more coupling factors. For 3 layers, there would be three coupling factors: K_{C12}, K_{C23} and K_{C13}. For 4 layers, there would be six coupling factors: K_{C12}, K_{C13}, K_{C14}, K_{C23}, K_{C24} and K_{C34} and so on. Equation (2) can be easily extended to calculate inductance of these multi-layer coils.

Table 1: PCB coil parameters

Symbol	Parameter	Units
Electrical parameters		
L	Total inductance	H
R_S	DC Resistance	Ω
C_P	Capacitance (parasitic)	F
Physical parameters		
D_{OUT}	Outer diameter of inductor	mm/ mils
M	Number of PCB Layers	-
N	Turns per layer	-
W	Trace width	mm/ mils
S	Trace spacing	Mm/mils
X_{ij}	PCB Layer Stack	mm/mils
t	Copper thickness	Oz-Cu/mils
Geometric parameters of coil		
r	Coil fill ratio	-
D_{AVG}	Average diameter	mm/mils
ρ	Geometric mean diameter	mm/mils
ρ_{cu}	Copper Resistivity	1.68×10^{-8} Ωm
l	Coil length per layer	mm/mils
Performance parameters of the application		
Q	Q factor	
F	Resonance frequency	Hz
X_R	Resonance impedance	Ω
Circuit components		
C_T	Tank capacitance	F

The Series resistance for M layer circular coil can be given by, [1]

$$R_s = \frac{K_f M * 2 * \pi * \rho_{cu}}{W * t}[D_{OUT} * N - N^2 * (W + S)] \quad (4)$$

where,

K_f is a factor which takes in to account skin depth and is given by

$$K_f = \frac{t}{\delta\left(1 - e^{-\frac{t}{\delta}}\right)}; \text{ and skin depth } \delta = \sqrt{\frac{\rho}{\pi f \mu_0 \mu_r}} \quad (5)$$

ρ is the resistivity of the conductor in Ω.m

f is the frequency in Hertz

μ_r is the relative magnetic permeability of the conductor

The parasitic capacitance C_p for a multilayer coil can be calculated as given in [1]. The self-resonant frequency of the coil is given by,

$$f_{SRF} = \frac{1}{2\pi\sqrt{LC_p}} \quad (6)$$

The equations for square spiral coil are used from [1, 13]. The detailed derivation of equation used in the tool can found in [11].

3. Automated Flow for Designing Multilayer Spiral PCB Coils

Figure 2 presents an automated flow for designing multilayer PCB. The detailed calculations are provided in previous work [11] and implementation is accessible at [12]. The total inductance of a multi-layer coil is dependent on a number of parameters. Few of the physical parameters are fixed by the manufacturing process. Based on largely used variables in the design, a tradeoff matrix between the physical parameters is shown in Table 2 [11]. In addition to these dependencies, one can plot tradeoff graph with external component values such as tank capacitance.

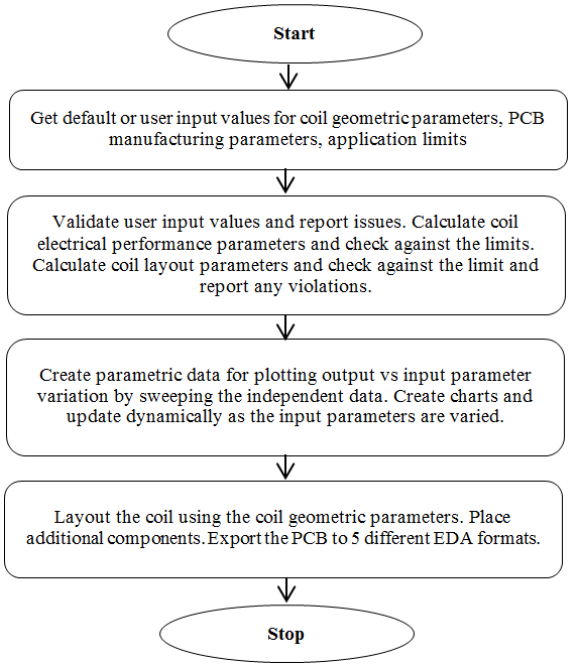

Figure 2: An automated flow for designing multilayer PCB coils.

Table 2: Tradeoff matrix for optimizing PCB coil

Tradeoff matrix	Outer diameter	Number of PCB layers	Coil fill ratio	Trace width	Trace spacing
Outer diameter (Area)	-	✓	✓	✓	✓
Number of PCB layers	✓	-	✓	✓	✓
Coil fill ratio	✓	✓	-	✓	✓
Trace width	✓	✓	✓	-	✓
Trace spacing	✓	✓	✓	✓	-

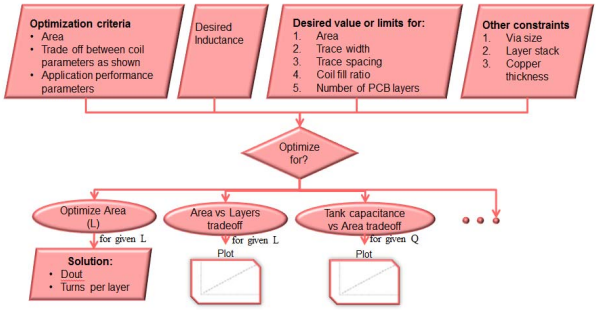

Figure 3: Flow for optimizing coil design for given parameter constraints.

4. Multilayer Spiral PCB Coil Optimization

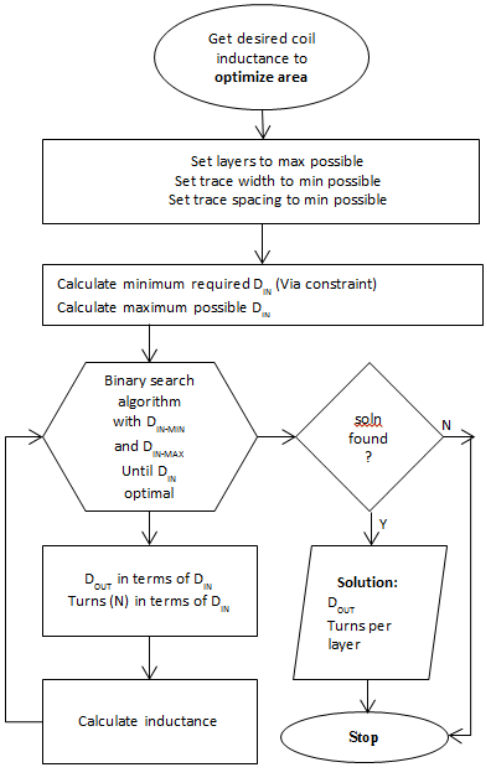

Figure 4: Algorithm to optimize area for a given parameter (inductance in this flow).

In order to optimize the coil design, turns per layers in terms of D_{IN} is given by

$$N = \frac{D_{IN}\left(\frac{1}{r}-1\right)+S-W}{2*(W+S)} \quad \text{where } r = \frac{D_{OUT}}{D_{IN}} \quad (7)$$

Minimum required D_{IN} takes into account the vias to be placed at the center of the coil for connections, is given by

$$D_{IN-MIN} = \frac{N}{2}D_{VIA} + \left(\frac{N}{2}-1\right)S_{VV} + 2S_{VM} \quad (8)$$

Where D_{VIA} = Diameter of a via,

S_{VV}= Via to Via spacing,
and S_{VT}= Via to Trace spacing

Maximum possible D_{IN} limited by max area available:

$$D_{IN-MAX} = rD_{OUT-MAX} \quad (9)$$

In order to optimize coil design for a given parameter an algorithm as shown in Figure 3, and Figure 4 is developed. The algorithm is used in finding design tradeoff between other parameters such as area vs layers and area vs coil fill ratio as shown in Figure 5.

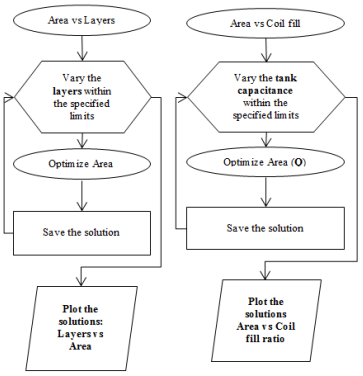

Figure 5: Flow for plotting area vs layers and coil fill ratio

5. Laying out a PCB Coil

Figure 6 shows top level flow to generate the layout of PCB coil and details are provided in [10]. The pseudocode to generate tracks as shown in Figure 7 is given below:

Notations

$\theta \rightarrow Track\ subtend\ Angle$
$R_r \rightarrow Radius\ increment\ per\ turn$
$R_T \rightarrow Radius\ increment\ per\ track$
$W \rightarrow Trace\ width$
$S \rightarrow Trace\ spacing$
$R_O \rightarrow Offset\ radius$
$\theta_O \rightarrow Offset\ angle$
$x1, y1, x2, y2 \rightarrow Track\ coordinates$
$N_T \rightarrow Tracks\ per\ turn$
$N \rightarrow Turns\ per\ layer$
$M \rightarrow Number\ of\ PCB\ layers$
$Shape \rightarrow circular, square, hexagonal, octagonal$

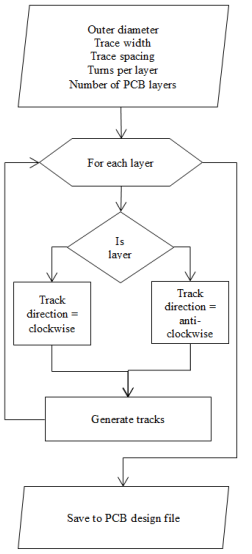

Figure 6: Flow for laying out the coil

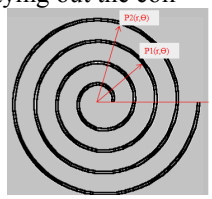

Figure 7: Points on a spiral using polar co.

```
func GenCoil(DesignSpecs)
N_T ← EvalTracksPerTurn(shape)
// 4, 6, 8 and 24 based on shape
θ ← SetSubtendAngle(N_T)
R_T ← EvalRadiusIncrRate()
R_O ← EvalOffsetRadius()
θ_O ← EvalOffsetAngle()
  for Layer: 1 → M
  θ = SetSubtendAng(SpirlDir)
    for I: N * N_T → 0
      x1 = [I.R_T + R_O] cos(I.θ)
      y1 = [I.R_T + R_O] sin(I.θ)
      x2 = [(I − 1)R_T + R_O]cos((I − 1)θ)
      y2 = [(I − 1)R_T + R_O] sin((I − 1)θ)
      CreateRect(x1, y1, x2, y2, W, Layer);
    end for
  end for
end func
```

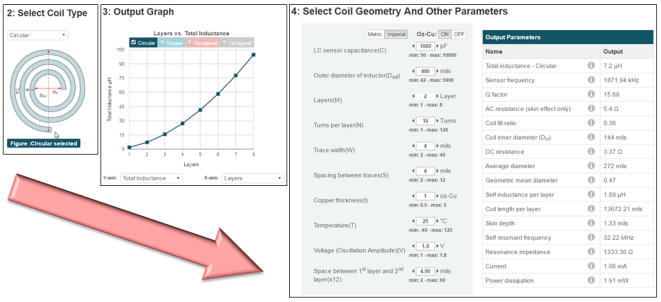

Figure 8: An online tool for designing multilayer PCB coils.

6. Results and Discussion

The flow presented in this paper has been implemented as an online design tool [12] as shown in Figure 8. First a coil shape is selected and next the coil geometries are selected. The tool instantly generates plot for various input and output parameters as well as calculates the current output parameters. Plots help designers to quickly arrive at the optimal coil design [14]. Figure 9 shows a plot between inductance vs PCB layers generated by online coil designer tool. The plot shows that L increases as M increases and follows eqn. (2) for multi-layer spiral PCB coils. Fig 10 shows a plot of D_{out} vs M generated for three different L values for circular spiral coil to tradeoff between area vs layers for desired inductance. For inductive sensing application [10] a circular sensor coil needs to be designed such that the sensor frequency is 1 MHz,

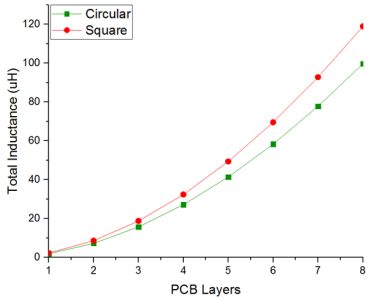

Figure 9: Plot of L vs. M for D_{out} =10mm, r=0.36, $W = S = x_{12} = x_{23} = x_{34} = x_{45} = x_{56} = x_{67} = x_{78} = 4mils, \rho_{cu} = 1\ oz - Cu$

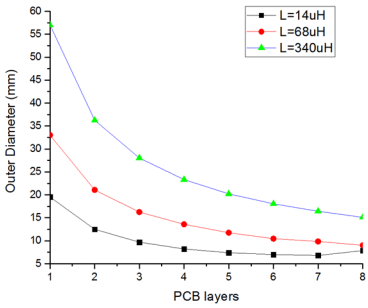

Figure 10: Plot of D_{out} vs. M for r=0.3-0.4, $W = S = x_{12} = x_{23} = x_{34} = x_{45} = x_{56} = x_{67} = x_{78} =$

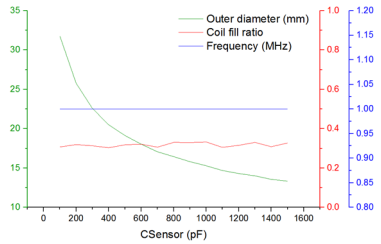

Figure 11: Plot of D_{out} vs. $Csensor$ for r=0.3-0.4, $W = S = x_{12} = x_{23} = x_{34} = x_{45} = x_{56} = x_{67} = x_{78} = 4mils, \rho_{cu} = 1\ oz - Cu$, and $Fsensor$ =1MHz

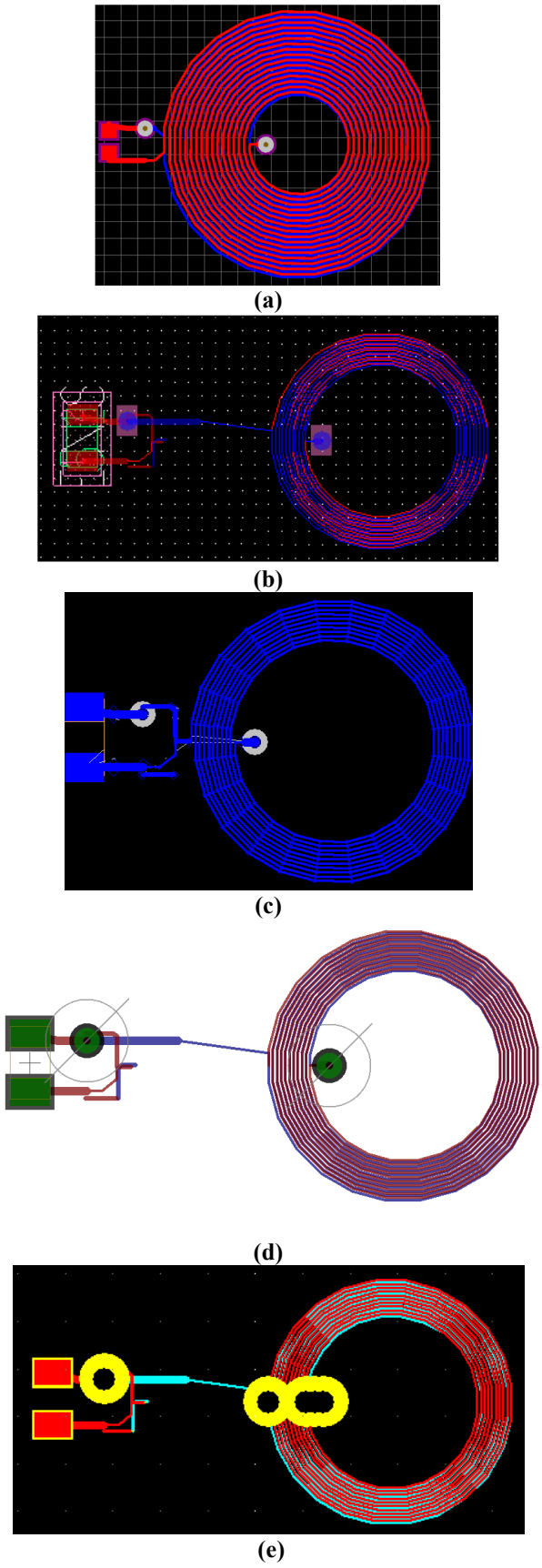

Figure 12: Generated two layer circular spiral PCB coil layout to a) Altium Designer b) Cadence Allegro c) Mentor PADS PCB d) CadSoft EAGLE PCB e) DesignSpark PCB

coil fill ratio is between 0.3-0.4. Figure 11 shows the tradeoff plot between D_{out} vs. sensor capacitance while keeping the fill ratio r within desired range generated using online tool. Once the desired coil has been designed the PCB layout can be exported to five different popular CAD tools by simply clicking on the export button in the online coil designer tool. Figure 12 shows the layout exported from online coil designer tool to various PCB CAD tools. Figure 12(a) shows a different coil compared to other coils due to different set of inputs provided to online coil designer tool to export this coil. Figure 13 shows the manufactured PCB coil for inductive sensing application. The online coil designer tool has been actively used by hundreds of designers worldwide every month for designing sensor coil for inductive sensing applications. The online coil designer tool quickly provides a multi-layer PCB coil design and layout which can be optimized for custom sensing applications.

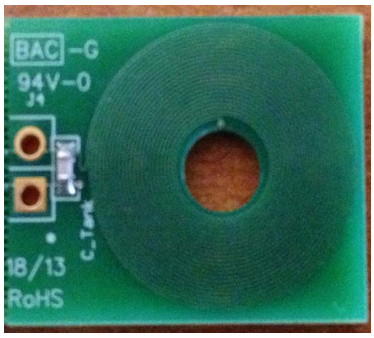

Figure 13: Manufactured PCB Coil for inductive sensing application.

7. Conclusion

An automated design tool for synthesis of optimal multi-layer multi-shape PCB coils in efficient way for inductive sensing applications has been presented. The methodology to generate the tradeoff plots, which helps the designer to optimize the coil as per the requirements, is discussed. A flow to automatically generate the PCB coil as well as pseudo code is presented. Finally the results from online coil designer tool are discussed. The instant generation of parametric plots for given input condition enables easier performance analysis over wide range of solutions. The proposed tool has reduced the design cycle time of sensor coil for inductive sensing applications to a fraction of a minute.

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